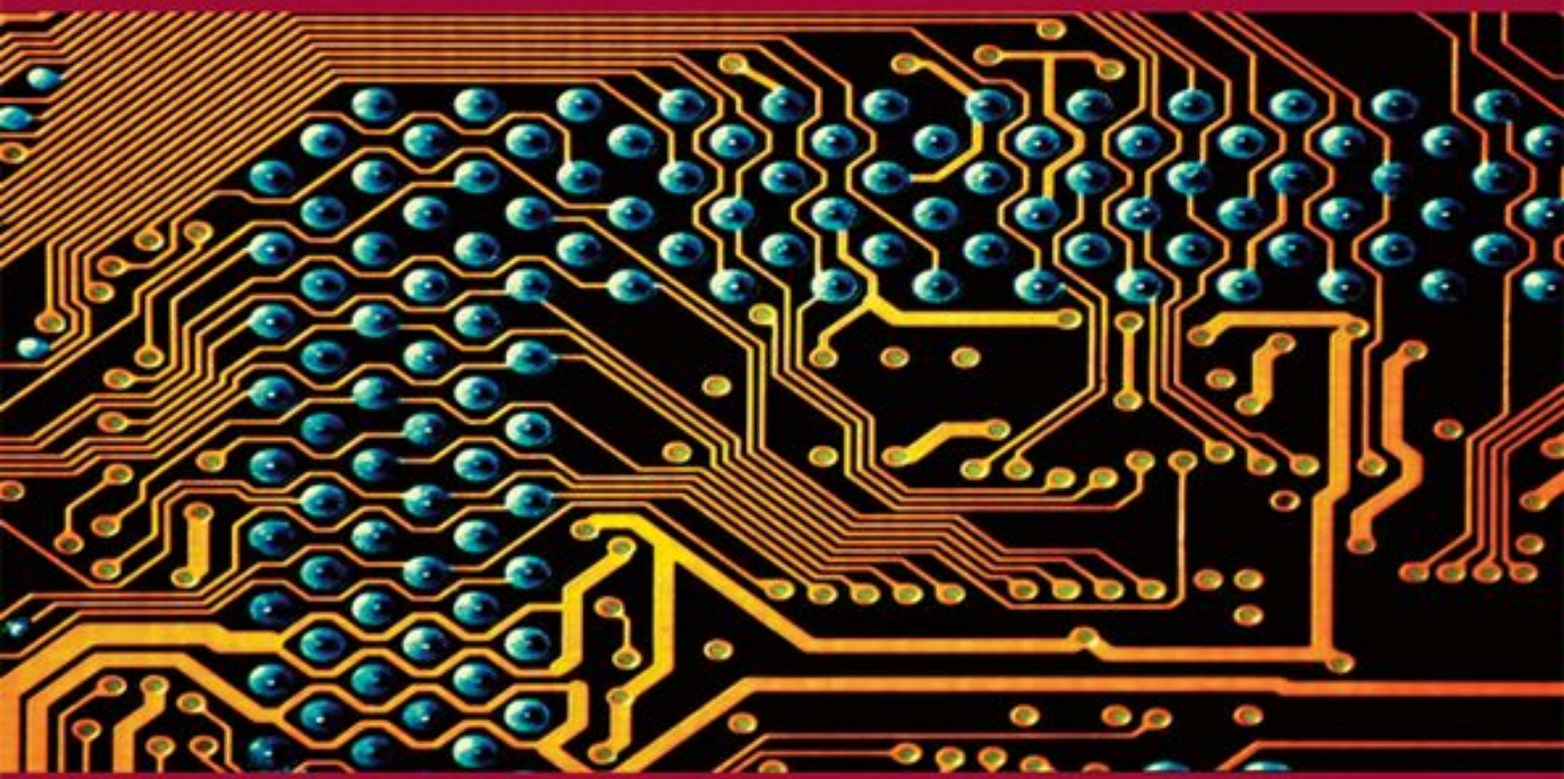

Power Electronics Semiconductor Devices

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Table of Contents

Preface

Electrical consumption, especially direct or variable frequency currents, has strongly increased over 50 years in industry. This situation explains the growth of power electronics.

At the beginning, when rectifiers replaced DC machines, only diodes and thyristors were used. Then power transistors appeared and enabled the extension of smaller power applications for domestic use. New research topics were developed around converters and power devices. For all these years, circuit specialists used available components but did not try to improve them; a lot of progress in device manufacturing proceeded from microelectronic tecnology.

At the beginning of the 21st century it appeared necessary to bring component researchers and circuit specialists closer together to create a global conception approach.

For over 15 years, French industrialists and academics have combined their efforts in the GIRCEP (Groupement Industriel et de Recherche sur les Composants Electrniques de Puissance) to develop, with the help of CNRS (Centre National de Recherche Scientifique – France), research programs in power electronics. Power Electronics Semiconductor Devices is a product of this work.

The first and second chapters are devoted to up-to-date switches (MOSFET and IGBT). Their properties and limitations are presented by P. Aloisi.

In Chapter 3, D. Chatroux and J.L. Schanen explain how to increase current or voltage with serial or parallel associations of elementary components.

M.L. Locatelli and D. Planson present a prospective study on new silicone carbide devices in Chapter 4. Possible performance improvements are shown as well as the technological difficulties linked to the production and process of the material.

Chapter 5 is devoted to a passive component essential for static converters; power capacitors working at high frequency. The authors are A. Béroual, S. Guillemet and Th. Lebey.

Power electronics must use conductors that allow the movement of large currents with a parasitic inductance as low as possible. A model for a good design of these conductors is described by E. Clavel, F. Costa, C. Gauthier, A. Guéna, J. Roudet and JL. Schanen in Chapter 6.

The operation of converters is often explained by the swiching cell concept defined by H. Foch [FOC88] in the 1980s. The right understanding of its operation and fine modeling are shown in Chapter 7, written by J. Roudet and JL. Schanen.

In Chapter 8, thermal aspects relating to the use of power electronic devices are developed by C. Perret and R. Perret with the help of J.M. Dorkel. The main problems related to cooling and examples of modeling are described.

Finally, in Chapter 9, P. Austin, M. Breil and JL. Sanchez show the value of integration on silicon for power electronic modules. From industrial achievements and laboratory prototypes they provide progressive ideas that can lead to a profound evolution of power electronics.

The book lacks at least one chapter: one which deals with magnetic components for power electronics. Several recent studies have been developed in laboratories; interested readers may consult [KER03] and [LAO04] for further information on current developments.

This book on power electronic devices represents a summary of research carried out in French and international laboratories in the early years of the 21st century.

Robert Perret

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[FOC88] FOCH H. and al, "Electronique de puissance", *Les Techniques de l'Ingénieur*, D3150 to D3163.

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[LAO04] LAOUAMRI K., KERADEC J.-P., FERRIEUX J.-P., BARBAROUX J., "Design and identification of an equivalent circuit for a LCT component. Inventory and representation of losses", *IEEE Transactions on Instrumentation and Measurements,* vol 53 no. 5, p.1409-1417, 2004.

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Chapter 1

Power MOSFET Transistors

1.1. Introduction

Before 1930, and thus a long time before the origins of the semiconductor transistor, J.E. Lilienfield was granted a patent for an electrostatic effect device allowing a current control like a MOSFET function. Thanks to planar technology, MM Khang and Atalla discovered in June 1960 the metal oxide semiconductor (MOS) structure, shown in Figure 1.1. This immediately provided the possibility of building:

– integrated circuits;

– large input impedance amplifier circuits;

– high frequency amplifiers.

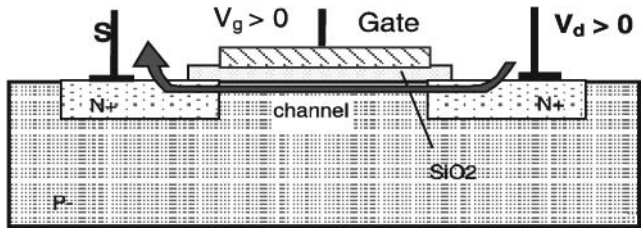


Figure 1.1. *Theoretical structure of a planar MOS*

Chapter written by Pierre ALOÏSI.

However, this planar structure is not able to simultaneously meet the following demands by power applications:

– high voltage operation,

– high current control.

Various research groups tried to improve this technology. The first trials to obtain a high voltage power MOSFET were based on improvements to lateral structures; see Figure 1.2. Due to the technological limitations of lateral structures for electrical field and current density, it was obvious that the vertical structure was the correct technology.

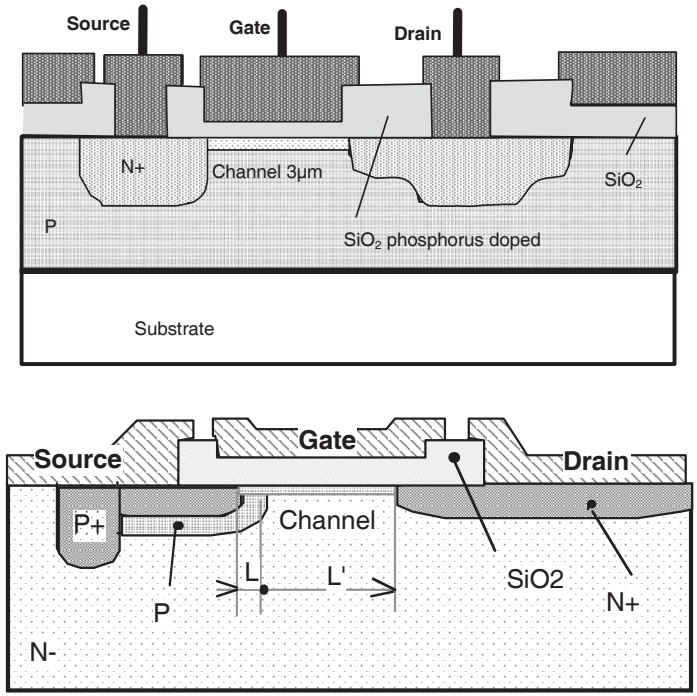


Figure 1.2. *DAWSON and lateral DMOS structures*

Removing the drain electrode from the silicon surface, the current density can be increased and the electrical field of the device is now independent of the channel length.

The first vertical structure was built around a V groove, or a truncated V, etched into the silicon using an anisotropic chemical, as seen in Figure 1.3a for the VVMOS and Figure 1.3b for the VUMOS. However, due to the high electric field at the point of the V or truncated V, this technology was replaced by a new VDMOS technology, with a double diffused channel vertical structure, as seen in Figure 1.4.

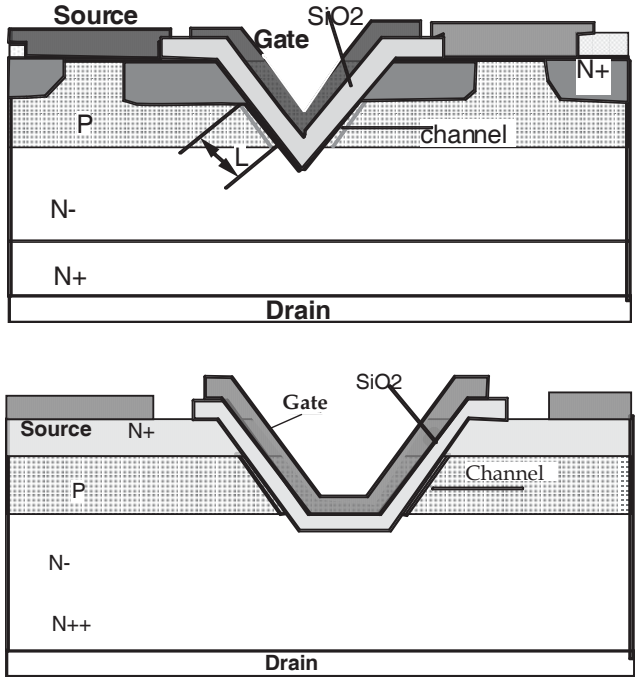


Figure 1.3. *VVMOS and VUMOS*

This vertical structure allows us to build the gate over the drift zone N-. This way, the die is also metallized, as well as the field plate, and enables a better thermal resistance.

Using a simple diffusion, including several masks, the polysilicon gate is built in order to make the source windows self-align, and to find a better compromise between the blocking voltage V_{dss} and the ON resistance R_{dson}.

The drawbacks are a higher interconnection capacitance and a bigger resistance for gate access, which increases the switching times and decreases the frequency performance.

The first designer of this P device was Yoshida from Hitachi in 1976, followed in 1979 by International Rectifier with the N-channel HEXFET, Siemens with the SIPMOS and Motorola with the TMOS.

Today, the VDMOS structure remains just about the same as the initial device, with a few adjustments.

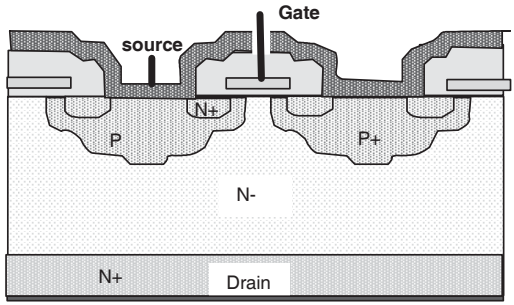


Figure 1.4. *VDMOS structure*

MOSFETs are unipolar devices where current transportation is carried out by majority carriers (electrons or holes). Thus, the expected current modulation from stored charges – which is the main phenomenon of a bipolar device – does not occur. Therefore, switching speeds are very fast and independent of the temperature. They are limited only by internal capacitances, which are charged and discharged when the device is turned on and off. The temperature coefficient of the internal resistance, R_{dson}, is positive: this leads to an easy paralleling. While bipolar transistors are driven by quite a large base current, the high input impedance of MOSFET allows a low energy gate drive. MOSFETs have a very good robustness during overloads, and the lack of secondary breakdown allows a large safe operating area. However, all of these good characteristics are in contrast with the large internal resistance of medium and high voltage devices.

Technological progress has allowed a large market for MOSFETs, mainly in low voltage segments of the market such as the automotive or telecoms industry. New technologies, such as “Superjunction”, increased the possibilities for medium voltage segments like the domestic market (240 V AC), thanks to internal resistances in the range of 0.3 Ω in 500 V devices, encapsulated in standard epoxy packages.

1.2. Power MOSFET technologies

1.2.1. *Diffusion process*

VDMOS structure is made with a lot of cells. Each of them is like a tiny independent parallel connected MOSFET.

The process of making them starts with a N+ substrate (doped at 10^{19} cm^{-3}), which is the drain. Then an epitaxial layer is grown (doped from 10^{14} cm^{-3} to 10^{16} cm^{-3}), which becomes the drift region where each cell is produced. For that, three diffused layers are produced: a P well (doped at 10^{16} cm^{-3}), then a P+ for the channel (doping 10^{18} cm^{-3}) and two N+ (doping 10^{19} cm^{-3}) for the source. To make a P-channel MOSFET, change all P and N regions to their opposites. The gate starts with an oxide that is very well controlled in thickness (around 100 nm) over which a polycrystalline silicon is laid down. The gate is over two P adjacent cells (channels) with the N- drift region in between, at the end a new oxide is deposited in order to insulate the gate from the source metallization, this becomes a link between all the cells and recovers all the device; only a gate pad is produced inside. The cell shape can be square or hexagonal, as seen in Figure 1.5.

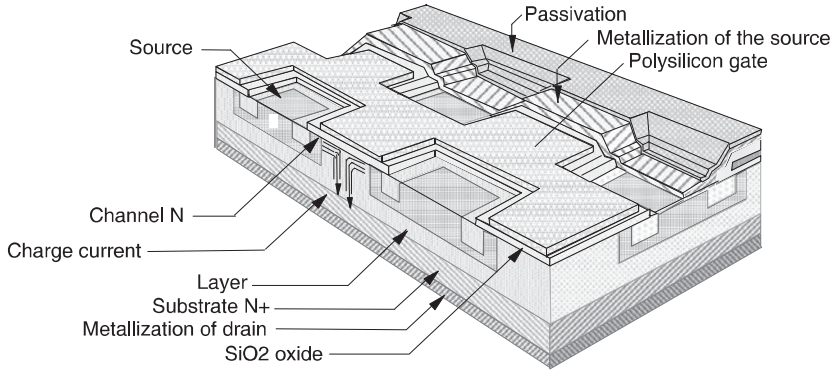


Figure 1.5. *Cellular MOSFET*

The main process steps are carried out as follows (see Figure 1.6):

– an epitaxial layer is grown on a 300 μm thick N+ wafer. Its thickness depends on the MOS voltage;

– a thick silicon dioxide SiO_2 is deposited over the die in which cell windows are opened to diffuse the P well and N+ source;

– etching and P+ channel implantation;

– thick oxide is removed except for the periphery, gate oxide is grown and polycrystalline silicon is deposited for gate metallization;

– gate oxide and polysilicon gate are etched to open cell windows. Boron for the P well is implanted and driven to make all the well. Thick oxide is grown on the die;

– cells window is again opened on the oxide and N+ sources are diffused;

– polysilicon gate is insulated by a SiO_2 deposition, the gate pad is opened for connection;

– source metallization over the die, contact pads for source and gate are opened;

– oxide is spread over the die for insulation. Metallization of drain back side occurs.

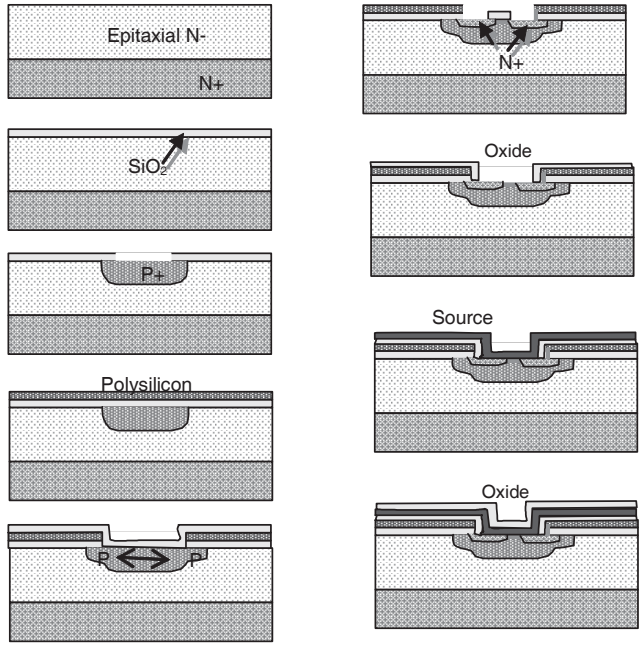


Figure 1.6. *Power MOSFET process*

1.2.2. *Physical and structural MOS parameters*

1.2.2.1. *Vertical structure*

If we examine the vertical structure of a MOSFET in more detail, we notice that it is made up of a N+N-PN+ parasitic bipolar transistor, in which the collector, emitter and base are formed by the drain, source and P channel. In order to avoid any parasitic transistor being turned on, base and emitter are short-circuited by the source metallization, but it remains a parasitic bipolar diode where the drain is the anode and the source is the cathode (see Figure 1.7), so the power MOSFET cannot sustain any reverse voltage.

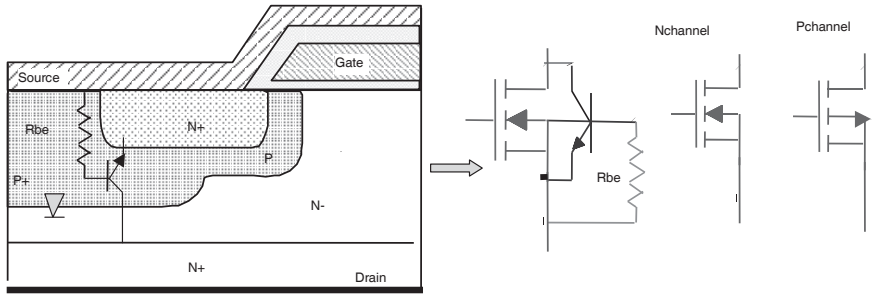
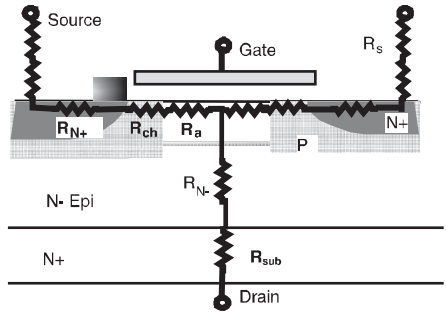


Figure 1.7. *Parasitic bipolar transistor and symbols*

1.2.2.2. *Upper side technological choices*

Power MOSFET is divided into two parts: the N- drift zone which sustains the electric field and the upper part including the gate, source and channel. This part controls the switching times of the power MOSFET. This part is very important for the internal resistance of a low voltage power MOSFET; see Figure 1.8. The main technological choices for the cells are the geometry and size; it will be the same for the P-well, the channel, the gate and the source.



R_{DSon}		
	VDS = 30V	VDS = 600V
RS	7%	0.5%
RN+	6%	0.5%
Rch	28%	1.5%
Ra	23%	0.5%
RN-	29%	96.5%
Rsub	7%	0.5%

Figure 1.8. *MOSFET internal resistance distribution*

1.2.2.2.1. Geometry of the cells

The rule for the channel resistance is very well known

$$R = pL/A$$

where ρ is the material resistivity, L is the channel length and A is the channel section. As the channel depth is constant, the channel resistance is governed by channel length and channel width. Thus for the same die size, channel resistance is lower when cells are optimal in terms of minimum channel length L and maximum perimeter Z = 4R; see Figure 1.9.

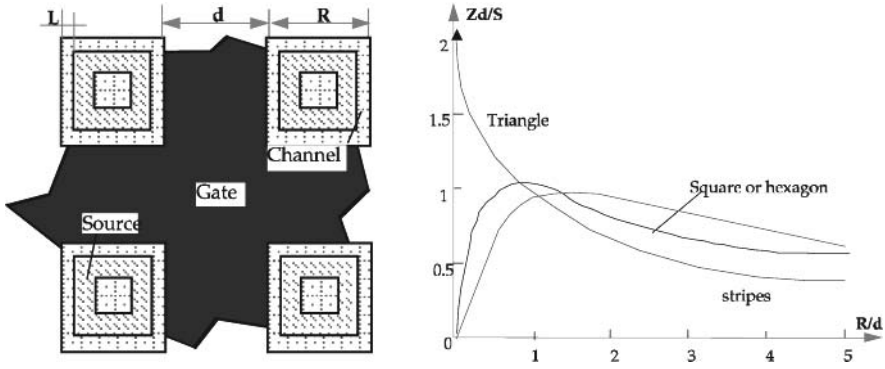


Figure 1.9. *Optimal shape of cells*

Figure 1.9 shows quality factor versus cell size; that optimal shape of the cell is given when R = d, source width = distance between two cells. Cell density is also an important parameter for lower channel resistance; this explains why the challenge for a low voltage power MOSFET is the maximum number of cells per surface unit. For medium and high voltage devices the number of cells per surface unit is not so important because the part of channel resistance in the R_{dson} is very low, and on the other hand, in high voltage devices the distance between two cells must be sufficient in order to avoid any JFET parasitic element.

1.2.2.2.2. P well choice

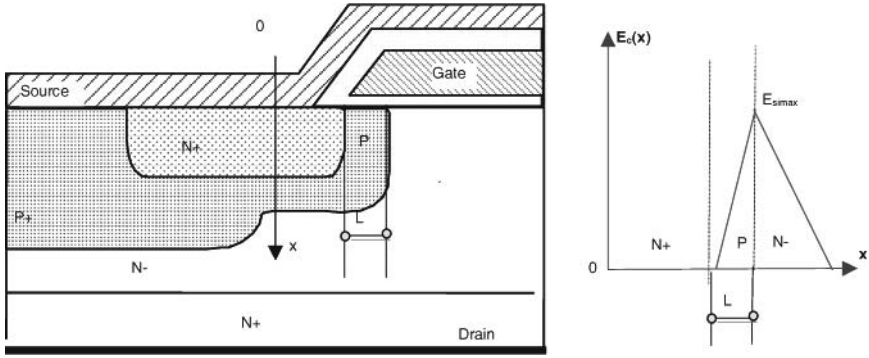


Figure 1.10. *Drain-source punch through*

When a voltage is applied between the drain and the source, a space charge $E_c(x)$ is spread out between the N- drain and P channel; see Figure 1.10. Thus, the doping level in the well must be high enough in order to avoid any field at the N+P source-well junction, if not, a punch through will come at this junction, For example, if a uniform doping is made inside the P well, a minimum channel length L is designed for the critical field E_{simax}.

$$L_{\min} > \frac{\varepsilon_{Si} E_{Si\max}}{qN_A}$$

P doping of the well can be increased in order to reduce the channel length, to reduce channel resistance. However, this increases the threshold voltage, and the voltage level of drive may be too high for the existing integrated drivers.

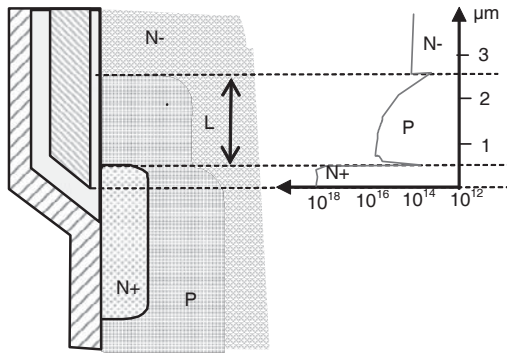


Figure 1.11. *Well doping profile*

From a practical point of view, channel length is defined by lateral doping drives of N+ source and P channel. This way, very short channels may be obtained. At the beginning, length L was around 10 µm; nowadays, length L is less than 1 µm. Normally, the doping level of N+ is much higher than the P level of the well, and punch through is automatically avoided; see the doping profile in Figure 1.11.

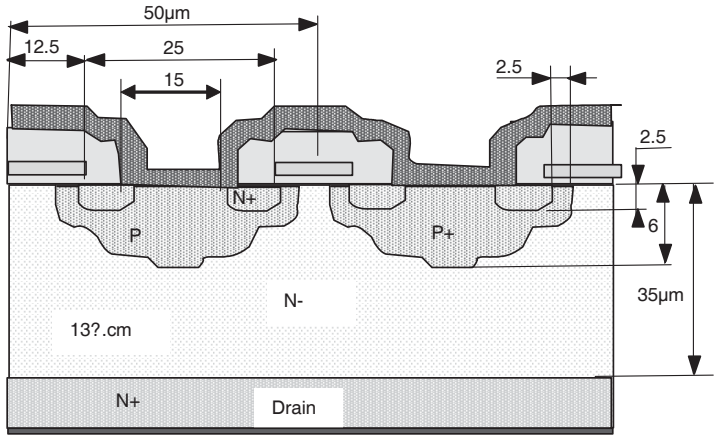


Figure 1.12. *400 V, 5 A MOSFET size*

As an example, Figure 1.12 shows the dimensions of a medium voltage power MOSFET, with 25 µm square cells, and a 35 µm N- drift zone, with a resistivity of 13 Ω.cm, in order to sustain a 400 V blocking voltage.

1.2.2.2.3. Gate realization

Gate characteristics must include:

– a low access resistance,

– a low leakage current,

– a great stability versus time,

– a high breakdown voltage,

– a low input capacitance.

The gate must also be easy to make.

The first gates were made of aluminum. This material has a lot of the desired qualities, except the fact that it sometimes contains particles of sodium, which in turn could create reliability problems.

Another possibility was to use molybdenum for gate manufacturing, but its cost is quite high.

Final choices remain monocrystalline silicon, but it is too resistive and expensive, and polycrystalline silicon, which is less resistive than monocrystalline,

but its resistance remains 3,000 times higher than that of aluminum, and 50 times higher than that of molybdenum. However, this resistance has no significance for the switching times of a current power MOSFET, and a gate may be N+ doped, during source diffusion, in order to be very well controlled.

Gate oxide thickness d_{ox} determines not only the maximum gate voltage but also the switching times by its capacitance. Maximum gate voltage is given by:

$$V_{GSmax} = d_{ox}. E_{oxmax}$$

where E_{oxmax} is the oxide maximum electric field, around 750 V/µm.

For a 75 V maximum gate voltage, a 100 nm oxide thickness is sufficient. Gate oxide capacitance per square centimeter, versus its thickness, is given by:

$$C_{ox} = \varepsilon_{ox}/d_{ox}$$

where ε_{ox} is the oxide permeability, which is $\varepsilon_{si}/3$ (around 3.5 10^{-13} F/cm). Cox is reduced when dox increases. Thus, a capacitance per square centimeter from 35 nF to 3.5 nF may be obtained for a gate thickness from 100 nm to 1 µm. Oxide capacitance is the main part of the MOSFET gate-source capacitance C_{gs}, and it may be obtained using:

$$C_{GS} = A_{ox}. \varepsilon_{ox} /d_{ox}$$

where A_{ox} is the oxide covered area, which may be between 50% and 80% of the die area. For example, C_{gs} per silicon square centimeter varies between 17.5 nF and 28 nF for d_{ox} = 100 nm and between 1.75 nF and 2.8 nF for d_{ox} = 1 µm, according to the oxide coverage. To decrease the input capacitance, d_{ox} must be increased, but a thick oxide leads to a large threshold gate voltage, while V_{th} is proportional to d_{ox}. Additionally, channel transconductance is decreased. A typical d_{ox} that is currently used is around 100 nm.

1.2.2.2.4. Source choice

The doping level of the N+ source is matched in order to control the channel length. This is also important for access resistance. Source metallization allows an easy paralleling of cells and an overall die coverage for good temperature spreading.

1.2.2.3. *Sustaining static drain source voltage V_{DSS}*

1.2.2.3.1. Drift region N-

V_{DSS} is proportional to the N- region thickness. For a given V_{DSS}, an optimization process is conducted between N- doping level and N- thickness, W_v. Avalanche, ionization and multiplying effects must also be taken into account. For voltage strength, a N- MOSFET structure is similar to a P+N-N+ diode structure. Figure 1.13 shows the electric field inside a MOSFET when it is polarized by a maximum drain-source voltage VDSS. In other words, when the electric field rises, the silicon critical field $E_{simax} = E_{Cmax}$.

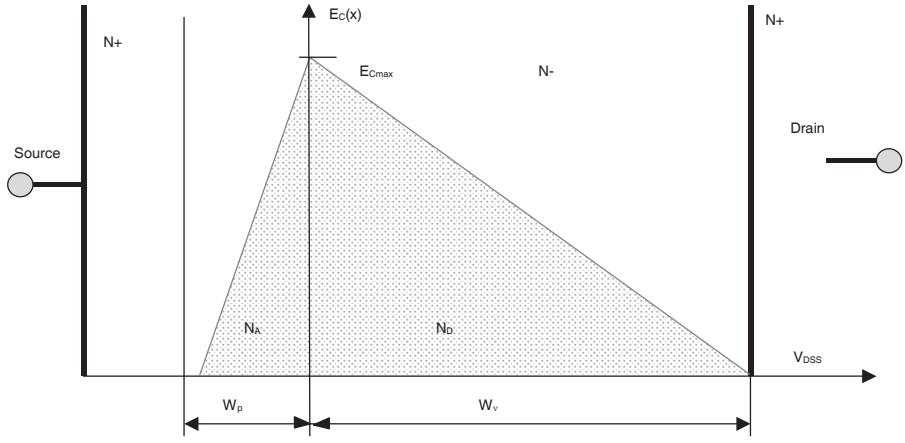


Figure 1.13. *Electric field inside the MOSFET drift region N-*

If the doping concentration inside the N- layer is constant, the electric field decreases linearly from the PN- junction to the N-N+ drain. Assuming an "abrupt junction", electric field $E_C(x)$, thickness of the W_{ZD} zone and the applied voltage V_{app} are linked together by the following equations:

$$E_C(x) = \frac{2V_{app}}{W_{ZD}^2}(W_{ZD} - x)$$

and $$W_{ZD} = \left(\frac{2\varepsilon_{si}.V_{app}}{qN^-}\right)^{1/2} = \left(\frac{1.3\cdot 10^7 V_{app}}{N^-}\right)^{1/2}$$

When the critical field is affected, silicon breakdown appears. At this time, the electron and hole ionization integral is equal to one, and carriers are produced by atom ionization in the space charge area. The current is increased by avalanche multiplication, M_p and M_n factors diverge to infinity:

$$1-\frac{1}{M_p}=\int_0^{W_{ZD}}\alpha_p \exp\left(-\int_0^x(\alpha_p-\alpha_n)dx'\right)dx=1$$

$$1-\frac{1}{M_n}=\int_0^{W_{ZD}}\alpha_n \exp\left(-\int_0^x(\alpha_n-\alpha_p)dx'\right)dx=1$$

where αp and αn are the ionization coefficients for holes and electrons, which vary exponentially with the electric field. They are given by the following equations:

$$\alpha_n = a.\exp(-b/E) \qquad \text{and} \qquad \alpha_p = 0.344\ a.\ \exp(-b/E)$$

where $a = 1.6.10^6$ (cm^{-1}) and $b = 1.65.10^6$ ($V.cm^{-1}$). Analytical integration of the two equations is very difficult, and solutions are found numerically. In order to obtain an analytical expression for the breakdown voltage, two simplifying hypotheses may be used. The first assumes equal ionization coefficients. Thus:

$\alpha_n = \alpha_p = \alpha_i$ (Mn = Mp =M) and α_i may be analytically expressed.

The second simplifying hypothesis uses the same multiplication terms for the preceding equations. Analytical expression for α_i is difficult and may be approximated by:

$$\alpha_I = 3.3\cdot10^{35}E(x)^7 \qquad (cm^{-1})$$

This equation is the best compromise for voltages over 400 V.

This way, the criterion for maximum voltage determination becomes:

$$1-\frac{1}{M}=\int_0^{W_{ZD}}\alpha_i dx=1$$

for $V_{app} = V_{DSS}$ and $W_{ZD} = W_\nu$

Thus: $\alpha_i = 4.2.10^{-33} \frac{V_{DSS}^{7}}{W_\nu^{14}} (W_\nu - x)^7$

and V_{DSS} is given by:

$$V_{DSS} = 5.5.10^4 \, W_\nu^{6/7}$$

Breakdown can now be obtained versus doping level N_D and N- thickness W_ν:

$$V_{DSS} = 4.26 \; 0.10^{13} \, N_D^{-3/4}$$

$$W_\nu = 2.94. \; 10^{-2} \, V_{DSS}^{7/6}$$

Thus, silicon resistance per unit area in the W_ν drift zone is:

$$R_\nu = 8.2.10^{-9} \, V_{DSS}^{2.5}$$

For example, if N_D doping level is $5.10^{14} cm^{-3}$, V_{DSS} could be around 400 V with a drift zone thickness of 32 µm. Then, silicon resistance per unit area is: $0.026 \; \Omega.cm^2$.

For a doping level $N_D = 10^{14} \; cm^{-3}$, V_{DSS} rises to 1,350 V with a thickness of 130 µm, and silicon resistance per unit area is $0.55 \; \Omega.cm^{-2}$.

In the previous analysis, the drift zone is completely empty when the E_{simax} electric field is raised. For the same maximum voltage, drift zone thickness may be reduced in a different way: the "punch-through" technique consists of doping the drift zone in such a way that the maximum electric field is lower than the critical E_{simax} field limit, when the drift zone is completely empty. In this case, the space charge spreads in the N+ drain, and the voltage is maximum when the critical field is raised (see Figure 1.14). If the ratio between maximum field and minimum field is expressed by a variable such as:

$$E_{Cm} / E_{CM} = 1 - \alpha$$

Then, the voltage at $E_{CM} = E_{simax}$ is:

$$V_{dsopt} = 0.5(E_{CM} + E_{cm}) W_{vopt} = 0.5(2 - \alpha) \, E_{simax} \, W_{vopt}$$

If the target for V_{DSSopt} is the value without the "punch-through" technique (α = 1), the following condition is requested:

$$V_{DSopt} = 0.5(2 - \alpha)E_{simax}.\ W_{vopt} = V_{DSS} = 0.5\ E_{simax}.\ W_{v}$$

This leads to: $W_{vopt} = W_{v}/(2 - \alpha)$

The electric field slopes during avalanche with and without the "punch-through" technique are:

$$\frac{E_{Si\max}}{W_{v}} = \frac{qN_{D}}{\varepsilon_{Si}} \quad \text{and} \quad \frac{\alpha E_{Si\max}}{W_{vopt}} = \frac{qN_{Dopt}}{\varepsilon_{Si}}$$

From these equations, the following characteristics are obtained:

$$N_{Dopt} = \alpha(2 - \alpha)N_{D} \quad (cm^{-3})$$

$$V_{DSSopt} = 5.5.10^{14}\ [(2 - \alpha)W_{vopt}]^{6/7} \quad (V)$$

$$V_{DSSopt} = 4.26 \cdot 10^{13} \left[\alpha(2-\alpha)\right]^{3/4} N_{vopt}^{-3/4} \quad (V)$$

$$W_{vopt} = 2.94 \cdot 10^{-2} \frac{1}{2-\alpha} V_{vopt}^{7/6} \quad (\mu m)$$

$$R_{vopt}^{*} = 8.2 \cdot 10^{-9} \frac{1}{\alpha(2-\alpha)^{2}} V_{DSSopt}^{2.5} \quad (\Omega.cm2)$$

Designers generally use α = 0.75. For example, for a 400 V device, the N- area is 26 µm deep with a doping of $4.7.10^{14}$ cm^{-3}, resistance per unit area is: 0.022 $\Omega.cm^{-2}$, leading to a 18% saving compared to the case without the punch-through technique.

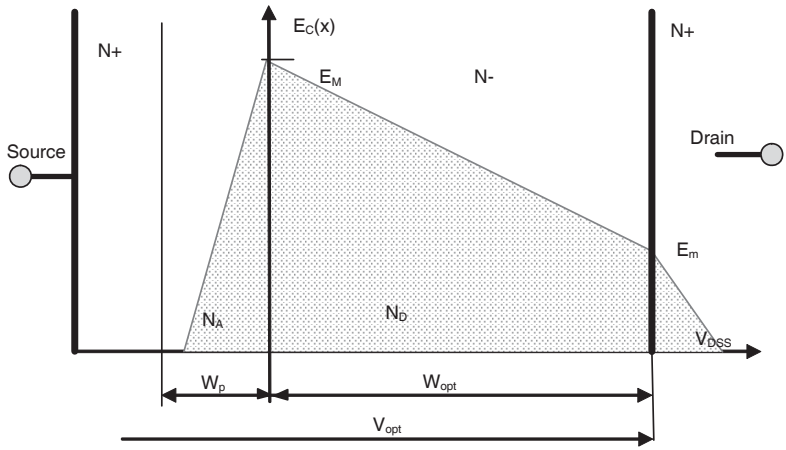


Figure 1.14. *"Punch through" electric field inside the N- MOSFET drift region*

1.2.2.3.2. Gate oxide and drift zone N- interface

When the MOSFET is blocked, the gate is connected to ground or negatively polarized. Drain source voltage and possibly the negative gate voltage are spread out between the drift zone and the gate oxide. In the case where no charges are stored in the gate oxide and in the gate silicon oxide interface, Figure 1.15 shows the electric field in the oxide and in the drift zone. In the silicon oxide interface we obtain:

$$\varepsilon_{ox}.E_{Cox} = \varepsilon_{si.}\, E_{CN}$$

When the field $E_{Cox} = 3E_{CN-}$ raises the critical value for silicon, the previous equality $E_{CN-} = E_{simax}$ becomes:

$$\varepsilon_{ox}.E_{Cox} = \varepsilon_{si.}\, E_{simax}$$

which gives:

$$E_{Cox} = 3\, E_{simax}$$

As there is a ratio of three between the dielectric constants of the two materials ($\varepsilon_{si}/\varepsilon_{ox} = 3$), the critical field of the oxide ($7.5.\ 10^6$ V/cm) is higher than the critical field in silicon, and the ratio E_{oxmax}/E_{simax} may be between 9 and 30 for a doping between 5.10^{17} cm^{-3} and 10^{14} cm^{-3}. This is much higher than 3. Therefore, breakdown

occurs only in silicon. With a doping level of $1.6.10^{14}$ cm^{-3}, and for a sustaining voltage around 1,000 V, the maximum electric field is $E_{simax} = 2.5.10^5$ V/cm when a 1,000 V voltage is applied between drain and source. Voltage inside the oxide is:

$$\Delta V_{ox}\ E_{oxmax}.d_{ox} = 3E_{simax}.d_{ox}$$

This is a 7.5 V voltage (d_{ox} = 100 nm, V_{GSmax} = 75 V).

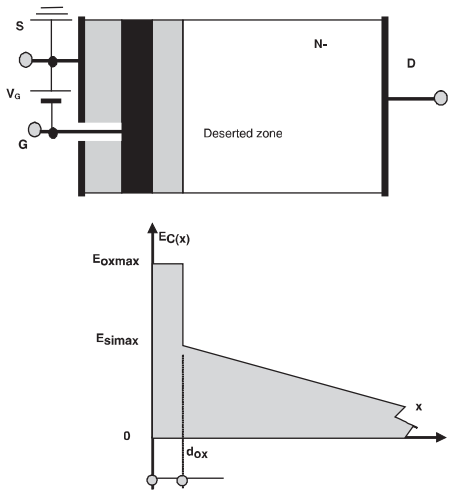


Figure 1.15. *Interface between gate oxide and deserted N- zone*

In the conduction state, before switch-off, the N- region under the gate oxide is a neutral region (rather than an accumulation region). When the voltage increases during switch-off, this neutral region becomes a space charge region. The two space charges at the PN- junction should be interpenetrated before the V_D voltage goes beyond the value of:

$$E_{oxmax.}\ d_{ox} \quad \text{(see Figure 1.16).}$$

This phenomenon is called the "gate shielding effect". Thus, a maximum distance appears between two wells: d_{max}. For example, for a junction 5 µm deep and an oxide thickness of 100 nm, d_{ox} becomes 34 µm for $N_D = 2.10^{14}$ cm^{-3} and 25 µm for $N_D = 4.10^{14}$ cm^{-3}.

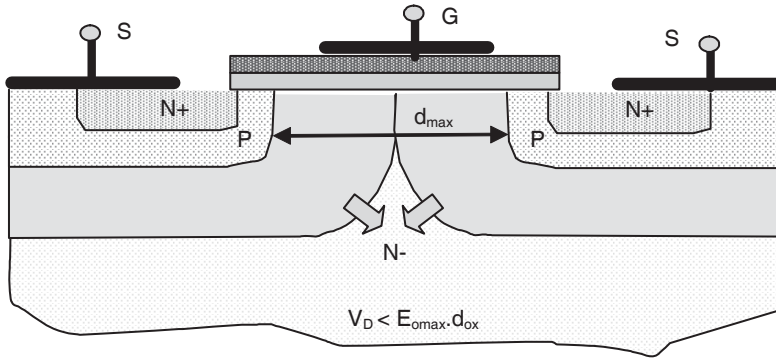


Figure 1.16. *Gate shielding effect*

1.2.2.3.3. Peripheral sustaining voltage

The silicon critical field is around 20 V/cm, thus a 1,000 V voltage may be sustained by a silicon thickness of 100 µm. However, at the atmospheric pressure, the air breakdown field is around ten times less. Therefore, a 500 µm distance in the air is requested to sustain this voltage, and the surrounding silicon must be large enough in order to keep the breakdown inside the silicon. Thus, in a silicon MOSFET, techniques such as “field plate”, “guard ring”, “pocket”, etc. are used; see Figure 1.17.

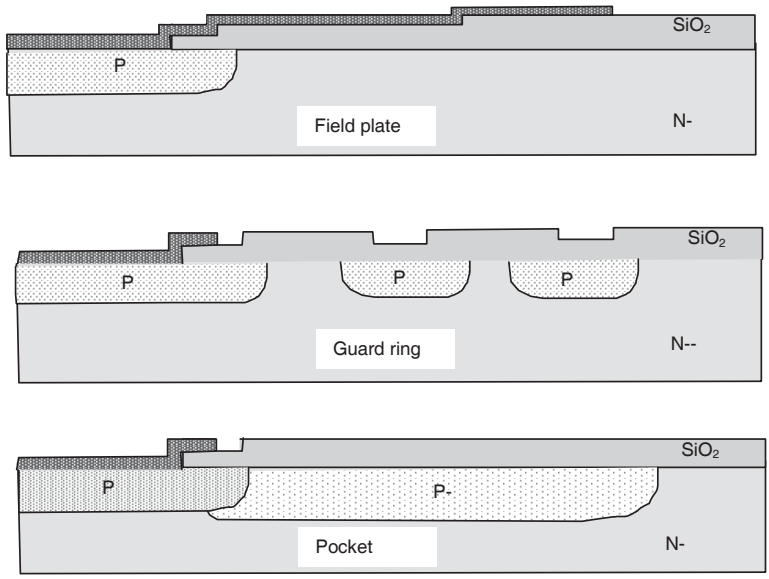


Figure 1.17. *Peripherals examples*

1.2.3. *Permanent sustaining current*

In the power device, the permanent sustaining current is mainly thermally limited. The drain-source current density is the same as the channel current density. The latter, with an adequate gate voltage, is generally much larger than the nominal values given by the manufacturer. During permanent operation, charge in the channel is given by:

$$Q_{ns} = \Delta V_{ox}\ L.2.\ \varepsilon_{ox}/d_{ox}$$

This gives the channel resistance:

$$R_{channel} = \frac{L^2}{\mu_{ns} Q_{ns}} = \frac{d_{ox} L}{\mu_{ns} \Delta V_{ox} Z \varepsilon_{ox}}$$

A channel may include the following characteristics: length: 2 µm, width: 10 m per cm^2, square cells of 10 µm, oxide thickness: 100 nm, channel resistance: $R_{channel}$: $9.5.10^{-4}\ \Omega.cm^{-2}$. This makes a current density of 525 $A.cm^{-2}$, if a 0.5 V voltage drop in the channel is acceptable. This value is much higher than current densities well known by power electricians ($\leq$100 $A.cm^{-2}$ for a low voltage MOSFET and around 50 $A.cm^{-2}$ for a power MOSFET over 600 V). Figure 1.18 shows a power MOSFET in a non-insulated package, such as a TO220. Losses in the die increase with

temperature and the thermal flux flows in the direction from die to die bonding, thermal spreading layer and package environment, a heat sink for example. Losses in the on state are:

$$P = R_{dson}.I^2_{DS}$$

The die temperature is given by

$$T_j = P\,(R_{th(si)} + R_{th(sol)} + R_{th(hs)}) + T_{sur}$$

where $R_{th(si)}$, $R_{th(sol)}$ and $R_{th(hs)}$ are the three sheet thermal resistances, which are given by the following equations:

– for silicon: R_{th} (si) = d(si) /σ_{th}(si).A(si)), thus 0.036°C/W per square centimeter, with a thickness d_{si} = 300 µm and $\sigma_{th(si)}$ = 0.83W/°C.cm;

– for soldering: R_{th} (sol) = d(sol) /σ_{th}(sol).A(sol) thus 0.03°C/W per square centimeter, for a thickness d_{sol} = 100µm and $S_{sol} = S_{si}(\sigma_{th(sol)})$ = 0.33 W/°C.cm for lead;

– for thermal spreading layer: R_{th} (TSL) = d(TSL) /σ_{th}(TSL).√A(TSL), thus 0.036°C/W per square centimeter, for a thickness d(TSL) = 2 mm A(TSL) = 2Si and σ_{th}(TSL) = 3.9 W/°C.cm for copper.

The amount of the three resistances is called "junction to case thermal resistance":

$$R_{th(j\text{-}c)} = R_{th(si)} + R_{th(sol)} + R_{th(TSL)}$$

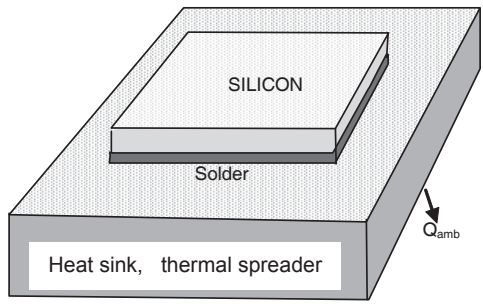


Figure 1.18. *Power MOSFET die stack*

We can see that for one square centimeter of silicon, the thermal limit is around 0.1°C/W. For a power MOSFET with a voltage over 400 V, we can accept an internal resistance R_{Dson} quite the same as that of the drift zone, $\tilde{R_v}$. The continuous current per square centimeter of silicon becomes:

$$J_{DS} = \sqrt{\frac{T_j - T_{env}}{R_{th(j-c)} R_{Dson}}} = \sqrt{\frac{T_j - T_{env}}{R_{th(j-c)} 8,2.10^{-9} V_{DSS}^{2.5}}}$$

with $R_{th(jh-c)}$ in °C/W and R_{DSon} in $\Omega.cm^{-2}$.

If the maximum temperature of silicon is T_j = 150°C, and if the ambient temperature is T_{amb} = 50°C, current density cannot be over 144 $A.cm^{-2}$, for a 500 V power MOSFET, and 60 $A.cm^{-2}$ for a 1,000 V power MOSFET. This calculated value of thermal resistance Rth(j-c) is always under the true value due to some defects in the links of the three layers. Now, electric insulation between silicon and external elements is always requested in power electronics. This insulation increases the thermal resistance, the previous values for the overall thermal resistance are always optimistic and the current density cannot be over 60 $A.cm^{-2}$ for a 500 V power MOSFET, and 20 $A.cm^{-2}$ for a 1,000 V device.

As the source connection of a power MOSFET is made of aluminum wires, the diameter and the number of these wires also make a continuous current density limitation. The semiconductor industry uses 250 µm diameter aluminum wires, for a maximum current of 10 A.

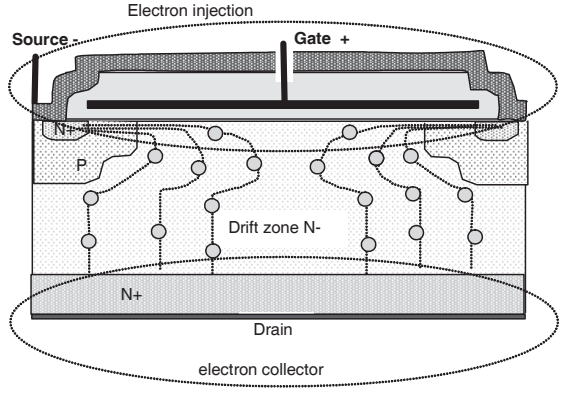


Figure 1.19. *Power MOSFET operation principle*

1.3. Mechanism of power MOSFET operation

1.3.1. *Basic principle*

As power MOSFETs are unipolar devices, only one carrier type operates: electrons for N-type power MOSFETs, and holes for P-type power MOSFETs. Electron injection is performed by N+ source and channel is driven by the gate. When $V_{DS} > 0$, injected electrons move through the drift zone and raise the N+ zone and the drain. When the gate stops the electron injection, it turns off the MOSFET. Figure 1.19 shows this principle. Thus, the channel is the main part of the power MOSFET drive.

1.3.2. *Electron injection*

Channel studies were undertaken early in the development of power MOSFET. Today, its mechanism is very well known. When the gate-source voltage is greater than a V_{th} value (a minimum value which creates a channel inversion), free electrons rise to the silicon surface in the P-well, called the inverting channel. This inversion modulates the channel resistivity. When V_{GS} is high, resistivity decreases. Figure 1.20 shows two possible operations. The voltage between channel ends is V(L).

First, saturation operation occurs when: $V_{GS} - V_{th} >> V(L)$, as depicted in Figure 1.20(a).

This is the channel state when the power MOSFET is conducting. The equation for this case is:

$$I_{Cchannel} = \frac{Z}{L}\mu_{ns}\frac{\varepsilon_{ox}}{d_{ox}}(V_{GS} - V_{th})V(L) - \frac{1}{2}V(L)^2$$

where μ_{ns} is the electron mobility at the silicon surface.

The threshold voltage is approximated by:

$$V_{th} = \phi_{ms} + 2\phi_{Fi} + \frac{d_{ox}}{\varepsilon_{ox}}\sqrt{4qN_A\varepsilon_{Si}\phi_{Fi}}$$

where Φ_{ms} is the difference between the metal and the semiconductor working functions, N_A is the channel doping, Φ_{Fi} is the distance between the Fermi level and the intrinsic semiconductor Fermi level, which is:

$$\Phi_{Fi} = U_T.\text{Log } N_A/ni$$

where U_T is a thermo dynamic unit (26 mV at 25°C).

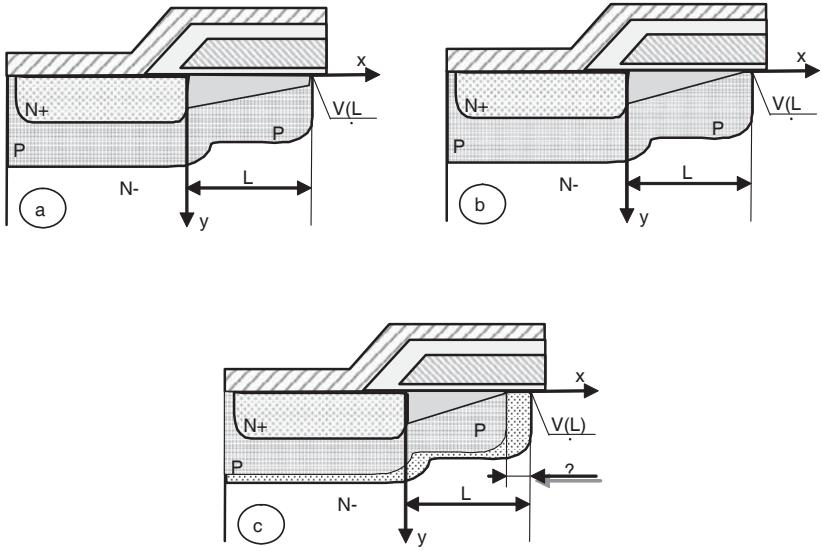


Figure 1.20. *Electron injection:*
(a) saturated operation; (b) beginning of pinch off;
(c) desaturated operation

We can see that the threshold voltage V_{th} increases with the channel doping, but also with the gate oxide thickness.

First, desaturation operation occurs when: $V_{GS} - V_{th} < V(L)$, depicted in Figure 1.20(c).

Starting from a conduction state with an I_D current in the channel, if gate source voltage slowly decreases, the charge density in the channel decreases and the channel resistance increases, in turn increasing the voltage drop in the channel. When the channel inversion leads to the disappearance of the channel ends, we obtain a channel pinch off (see Figure 1.20(b)). If the gate voltage is even more reduced, pinch off moves towards the source, and a deserted region, or space charge, is settled at the channel ends. This is the desaturation operation. Channel voltage is quite equal to the space charge ΔL. If the channel doping is not important, and if the gate oxide thickness is thin, the pinch off voltage is: $V(L) = V_{channel} = V_{GS} - V_{th}$.

After the channel pinch off, channel electron flux only depends upon the gate voltage V_{GS}. This maximum current is:

$$I_{channel} = \frac{Z}{2L}\mu_{ns}\frac{\varepsilon_{ox}}{d_{ox}}(V_{GS} - V_{th})^2$$

If ΔL/L is not negligible, as in the case of a short channel, the channel current is a function of voltage V/(L) in the form of:

$$I_{channel} = \frac{Z}{2L}\mu_{ns}\frac{\varepsilon_{ox}}{d_{ox}}(V_{GS} - V_{th})^2 \cdot \frac{L}{L - \Delta L}$$

where $\frac{Z}{L}\mu_{ns}\frac{\varepsilon_{ox}}{d_{ox}}$ is usually represented by K_p, the transconductance parameter.

1.3.3. *Static operation*

This operation may be the ON state or the OFF state. The ON state is the conduction of an I_D current, which is not channel driven, but imposed by the load. So, the number of electrons at input is equal to the number of electrons at drain output. If the requested charge density for the current is small compared to the doping density, $J_D/qv_n << N_D$, the drift zone is like a R_D resistance, and the power MOSFET shows a V_{DS} drop in voltage (see Figure 1.21). If the drain N+ and the source N+ resistances are neglected:

$$V_{DS} = I_D . R_{DSon} = I_D . (R_n + R_a + R_{channel})$$

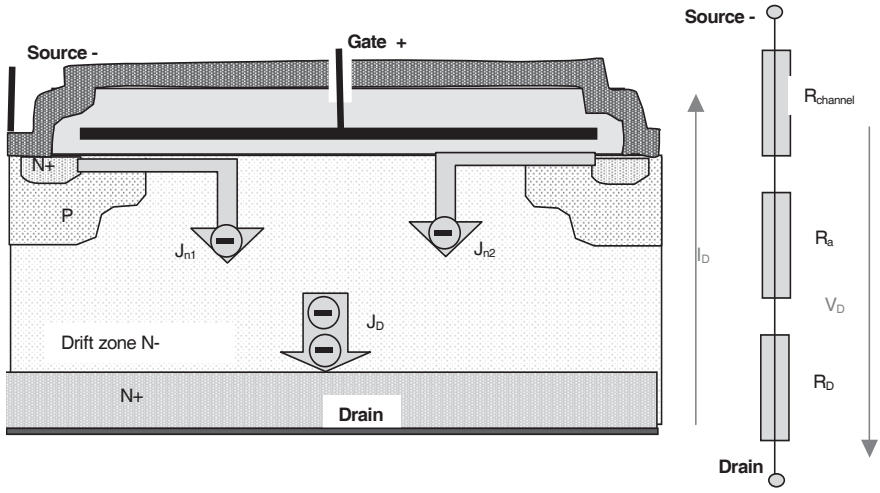


Figure 1.21. *Conduction operation:* $J_{D1} + J_{D2} = J_D$

Channel resistance depends upon the physical characteristics of the material used, on channel geometry and also on gate voltage. The relationship may be written as:

$$R_{channel} \approx \left[\frac{Z}{L} \mu_{ns} \frac{\varepsilon_{ox}}{d_{ox}} (V_{GS} - V_{th}) \right]^{-1}$$

Access resistance, R_a, and drift zone resistance, R_v, are two phenomena able to change their theoretical values. This is achieved by narrowing the access region and restricting current lines at the drift region entry. We can see, as shown in Figure 1.22, that electrons, after running in the channel close to the silicon surface, turn at 19 degrees in the drift zone. The sum of the voltage drop, in the channel, in the lateral region (weak, thanks to the accumulated region), and in the access region, build up a space charge in the access zone, and, consequently, the pathway for electrons is narrowed. After that, electrons are injected into the drift zone and go out through the drain. We can see that the current pass at the entry level of the drift zone, is narrower than at the output level. Due to these two parasitic effects, the effective resistances R_a and R_v increase up to 20%.

This R_a resistance may be written as:

$$R_a = \lambda \cdot \frac{1}{q\mu_n N_D} \frac{2h}{Zd}$$

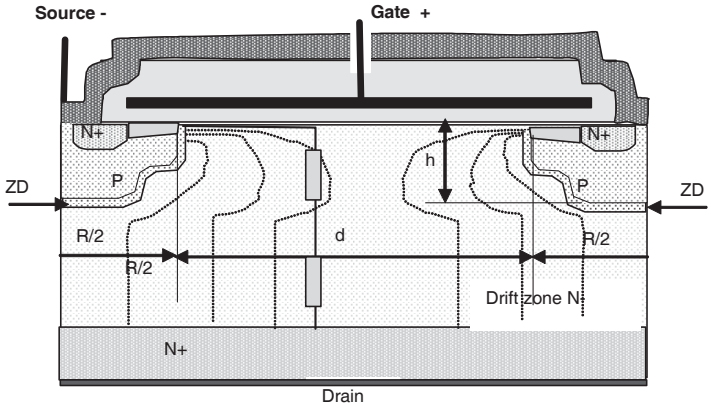


Figure 1.22. *Resistances R_a and R_v increase due to the narrowing pathway*

This may be considered as an N- silicon bar with a cross-section Zd/2, a length h and a doping level N_D increased by a factor λ according to cell geometry and gate voltage. This factor is greater than one, and increases when the doping level increases, and decreases with P+ depth and gate voltage V_{GS}.

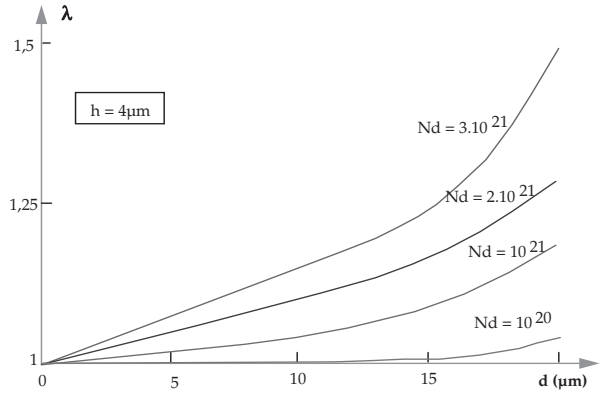
Thus, λ is high for a low voltage power MOSFET, and λ is close to one for a high voltage power MOSFET (as shown in Figure 1.23(a)).

The drift zone resistance is:

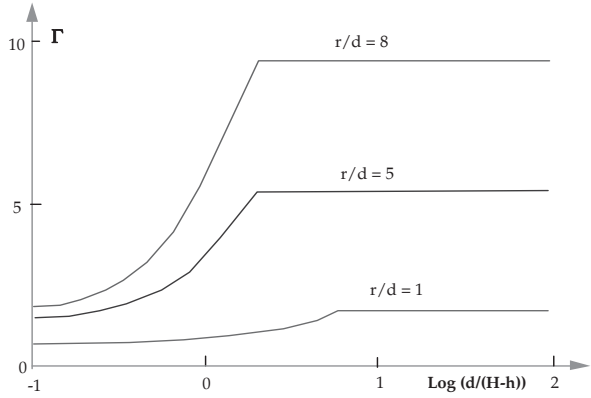
$$R_{vV} = W_v / q\, \mu_n\, N_D\, A(si)$$

The actual value for this resistance is given by: $R_v = \Gamma . R_{vV}$

The Γ factor represents the geometrical factors. It is larger for a low voltage power MOSFET, according to Figure 1.23(b).



(a)



(b)

Figure 1.23(a) and (b). *Resistances Ra and R_v versus geometrical factors*

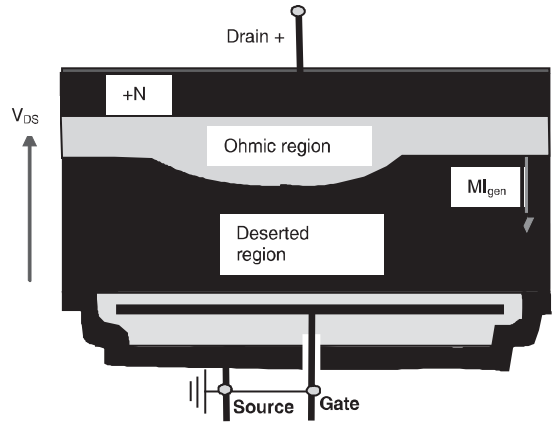
In the OFF state, the external power circuit imposes a supply voltage between the drain and source of the MOSFET. Drift zone N- includes two regions: a deserted space charge region W_{ZD}, which sustains the voltage, and a resistive region, which is the remaining part of the drift region without a field, depicted in Figure 1.24(a).

Very few mobile carriers ($p << n << n_i$) are located in the deserted space. The field generates some electron-hole pairs, and consequently a generative current. This is the main part of the leakage current of the MOSFET when the die temperature

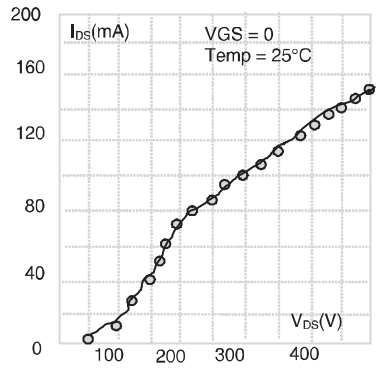
remains under about 170°C. If the generative electron-hole pair is represented by a generative rate τ_{gen}, the leakage current is:

$$J_D \text{ leakage} = q.n_i W_{ZD}/\tau_{gen}$$

Leakage increases with the applied voltage, through space charge W_{ZD}, and increases with temperature through the intrinsic concentration n_i, which is closely related to temperature. Figure 1.24(b) shows the leakage current versus the applied voltage.



(a)



(b)

Figure 1.24(a) and (b). *Blocked MOSFET, leakage current versus V_{DS}*

1.3.4. *Dynamic operation*

The dynamic operation's main function is to commutate the power electronics system. Power MOSFETs are much faster than bipolar transistors, where a conductivity modulation takes place. Only a very small quantity of charges are involved, corresponding to the establishment and discharge of the space charge in the drift region. Consequently, the dynamic operation is only dominated by capacitive effects, as seen in Figure 1.25. Two types of capacities are included: constant capacities and the non-linear capacities. Constant capacities are: C_{oxm}, due to oxide and source metallization; C_{oxd}, the access capacity; C_{oxp}, the channel capacity; and C_{oxs}, the P+ source capacity.

The three last capacities can be easily calculated using the following equations:

$$C_{oxd} = 0.5\ L_{acc}.Z.\varepsilon_{ox}/d_{ox},\ C_{oxp} = 0.5\ L.Z.\varepsilon_{ox}/d_{ox} \text{ and } C_{oxs} = L_{rec}.Z.\varepsilon_{ox}/d_{ox}$$

where L_{rec} is the gate length over the source N+.

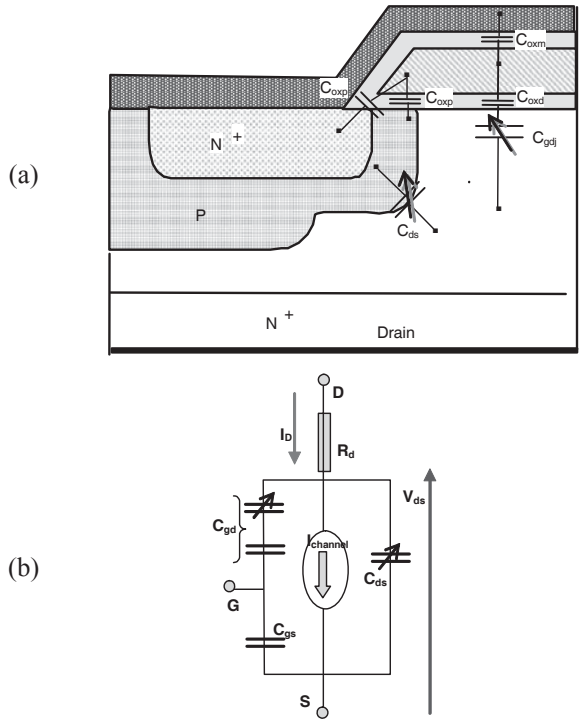


Figure 1.25. *(a) Various internal capacities and (b) equivalent circuit*

The drift zone is divided into two regions: the space charge region, and the ohmic region. The non-linear capacities highlight the space charge variation: C_{gdj} for the access deserted area L_{acc}, and C_{dsj} for the P+N- L_{ds} deserted area. The non-linear capacities are described by the following equations:

$$C_{gdj} = \frac{1}{2} L_{acc} \sqrt{\frac{q\varepsilon_{si} N_D}{2V_{ZD(acc)}}} \quad \text{and} \quad C_{dsj} = \frac{1}{2} L_{ds} \sqrt{\frac{q\varepsilon_{si} N_D}{2V_{ZD(ds)}}}$$

where $V_{ZD(acc)}$ and $V_{ZD(ds)}$ are the space charge voltages in the L_{acc} and L_{ds} parts of drift region N-. They are equivalent to:

$$V_{ZD(acc)} = V_{DS} - I_D . R_{acc} - V_{GS} \quad \text{and}$$

$$V_{ZD\,(ds)} = V_{DS} - I_D . R_{ds} + \Phi\Phi_{PN}$$

where Φ_{PN} is related to the P+N junction in thermo dynamic equilibrium.

Due to the difference between input and output currents in silicon, the power MOSFET involves an enlargement or a narrowing of the space charge in this silicon. Thus, there is a differrence between the $I_{channel}$ current in the channel, and the I_D current imposed by the load.

When the drain current is larger than the channel current, $\Delta I_N = I_D - I_{channel} > 0$, more electrons are released from the drain than are input by the channel. Thus, an enlargement of space charge occurs and V_{DS} increases.

Now, when $\Delta I_N = I_D - I_{channel} < 0$, more electrons come from the channel input than are released by the drains output. Thus, a narrowing of space charge occurs and V_{DS} decreases. The following formula describes these phenomena:

$$I_D - I_{channel} = C_{gdj} . dV_{ZD(acc)}/dt + C_{dsj} . dV_{ZD(ds)}/dt$$

The overall gate-source capacitance is quasi-constant and equal to:

$$C_{gs} = C_{oxm} + C_{oxp} + C_{oxs}.$$

The drain-source capacitance C_{ds} is only related to the space charge in the drift region and in the P+N junction. It is obviously non-linear. The gate-drain capacitance is made by a series association of capacitances: $C_{gd} = C_{gdj} . C_{oxd}/(C_{gdj} + C_{oxd})$. The neutral (or ohmic) region of the drift region is divided in two parts, L_{acc} and L_{ds}, represented by two resistances, R_{acc} and R_{ds}, according to Figure 1.25.

In the channel, for behavioral studies, a quasi-stationary approach is sufficient in the dynamic case. The channel current versus time is given by:

$$I_{channel}(t) = 0 \qquad V_{gs} - V_{th} \leq 0$$

$$I_{channel}(t) = \frac{Z}{L}\mu_{ns}\frac{\varepsilon_{ox}}{d_{ox}}(V_{GS}(t) - V_{th})V(L,t) - \frac{1}{2}V(L,t)^2 \qquad V_{gs} - V_{th} > V(L,t)$$

$$I_{channel}(t) = \frac{Z}{2L}\mu_{ns}\frac{\varepsilon_{ox}}{d_{ox}}(V_{GS}(t) - V_{th})^2 \qquad V_{gs} - V_{th} \leq V(L,t)$$

The channel voltage drop, $V_{channel}(t)$, is close to V(L,t) before pinch off. It remains constant and equal to V_{gs} (t) – V_{th} after pinch-off, because the deserted region of the drift zone sustains the main part of the voltage $V_{DS}(t)$.

Neglecting bi-dimensional effects, such as dissimilarities of the two parts of the neutral region ($R_{acc} = R_{ds} = R_d$), neglecting the access region, the parasitic elements like N+N-PN+ transistor and the anti-parallel diode, the equivalent circuit representing the dynamic operation of power MOSFET is depicted in Figure 1.25(b).

In this simplified schematic, the voltage V(L,t) becomes V_{DS} for the channel voltage, when it is under $V_{GS}(t) - V_{th}$. The resistance R_d in $\Omega.cm^{-2}$ is given by:

$$R_d = \frac{1}{q\mu_n N_D} \cdot (W_V - \sqrt{\frac{2\varepsilon_{Si}V_{DS}}{qN_D}})$$

Most of the data sheets give the input capacitance C_{iss}, the output capacitance C_{oss} and the transfer capacitance C_{rss}.

They are measured by a guarded capacitor measurement device, versus voltage V_{ds}, at 1MHz. The guard is made in order to avoid any interference from the other two capacitances, when one capacitance is being tested, as shown in Figure 1.26.

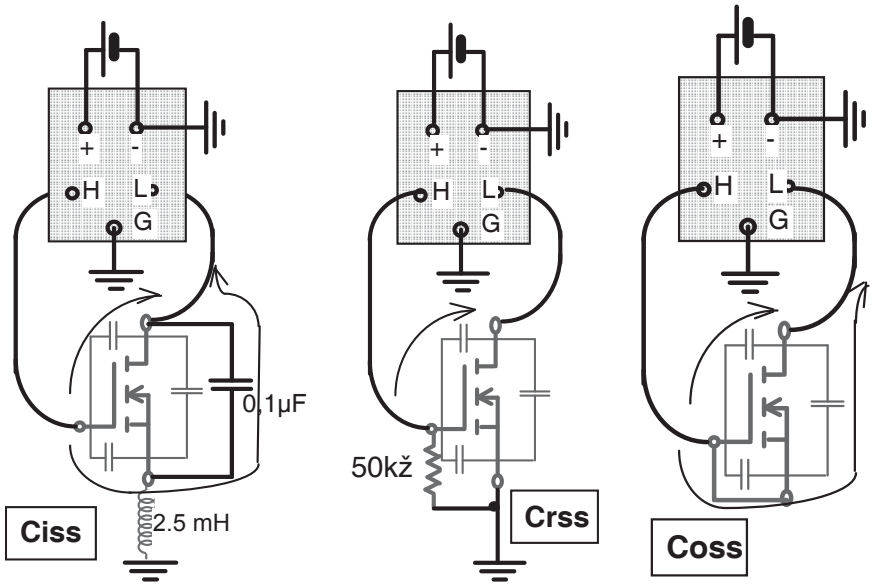


Figure 1.26. *Measuring MOSFET capacitance*

From these measured capacitances, the three capacitances of the equivalent circuit may be calculated as:

$$C_{gd} = C_{rss}, \qquad C_{gs} = C_{iss} - C_{rss} \qquad \text{and} \qquad C_{ds} = C_{oss} - C_{rss}$$

Figure 1.27 shows the capacitances versus V_{ds} for a 400 V, 14 A power MOSFET. We can see that the C_{gs} capacity is constant, while the C_{gd} and C_{ds} capacitances are strongly related to V_{DS}.

If $V_{DS} \approx V^*_{DS}$ is accepted, the following equation can be derived from the equivalent circuit (shown in Figure 1.25(b)):

$$(C_{ds} + C_{gd}).(dV_{DS}/ dt) - C_{gd}\,(dV_{GS}/ dt) = I_D - I_{channel}$$

$$\text{and} \quad (C_{gs} + C_{gd}).(dV_{GS}/ dt) = C_{gd}\,(dV_{DS}/ dt) + i_g$$

These two equations give a simplified one-dimensional model of a power MOSFET in a dynamic regime. More complicated equivalent circuits exist, but this one is suitable for most switching circuit operations.

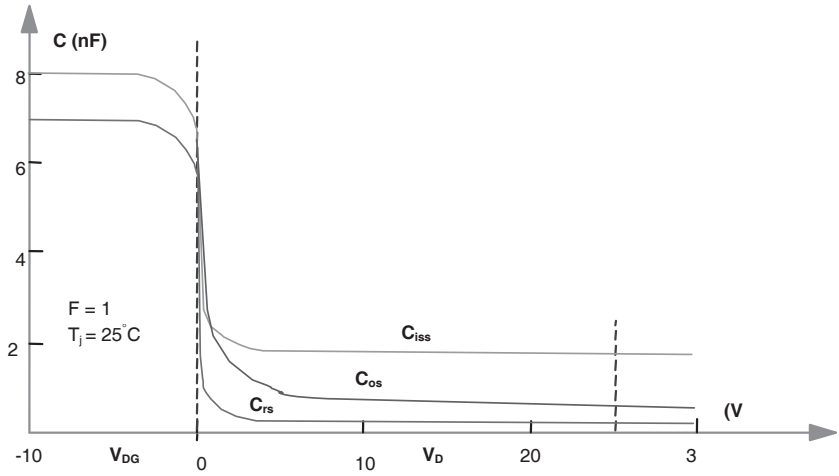


Figure 1.27. *Capacitances versus drain voltage V_{ds}, for a 400 V, 14 A, power MOSFET*

1.4. Power MOSFET main characteristics

Figure 1.28 shows a 500 V, 7 A, 8 Ω MOSFET, where output characteristic $V_D = f(I_D)$, versus gate voltage V_{GS}.

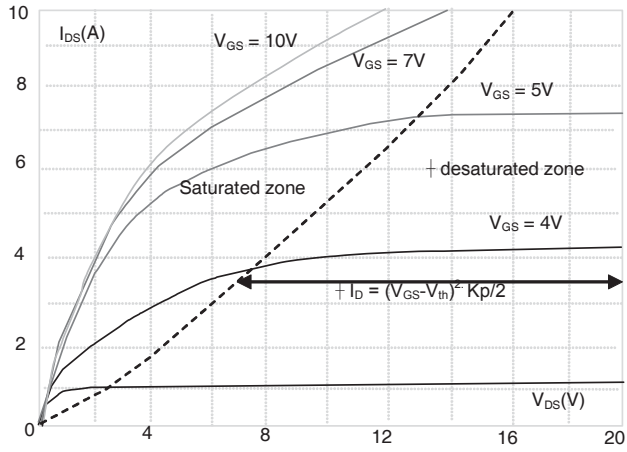


Figure 1.28. *Output characteristic of 500 V, 7 A, 8 Ω power MOSFET*

This chart shows two operating zones: a saturated or resistive zone and an active or linear zone, separated by a dotted line, which corresponds to the maximum current given by the channel, according to the gate voltage V_{gs}.

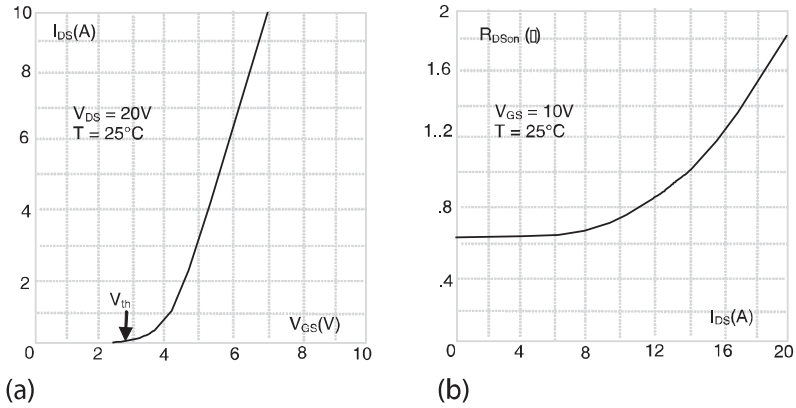


Figure 1.29. *Transfer characteristics and $R_{DSON} = f(I_D)$ for a 500 V, 7 A, 8 Ω MOSFET*

Figure 1.29(a) shows the transfer characteristics I_{DS} versus V_{GS} in the linear zone, with a constant V_{DS} and over V_{GS}-V_{th}. Figure 1.29(b) shows the internal resistance V_{DS}/I_{DS} in the saturated zone, with a constant voltage drive greater than V_{th}. Figure 1.30 depicts the gate charge for a constant drain current.

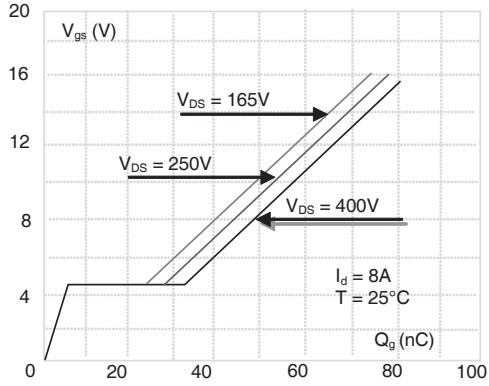


Figure 1.30. *Gate charge of a 500 V, 7 A, 8 Ω power MOSFET*

1.5. Switching cycle with an inductive load

Switching with an inductive load is very common in power electronics.

Figure 1.31(a) shows a power circuit where the inductive load is represented by a perfect current source in parallel with a free-wheeling diode D_{FW}, and driven by a power MOSFET. The gate charge is driven by a perfect voltage source $+V_g$ or $-V_g$, through a resistance R_g. The MOSFET equivalent circuit is given in Figure 1.31b. Figure 1.32 shows various waveforms and Figure 1.33 explains the various phases.

1.5.1. *Switch-on study*

1.5.1.1. *Delay time at switch-on*

At time t = 0, the drive signal $V_{GG}(t)$ changes from zero or a negative voltage to a positive voltage $+V_{GG}$. The gate is charged from the beginning, as indicated by the following exponential function:

$$V_{GS}(t) = V_{GG}\left[1 - 2e^{-\frac{t}{R_g(C_{gs}+C_{gd})}}\right] \approx V_{GG}\left[1 - 2e^{-\frac{t}{R_g C_{gs}}}\right] < V_{th}$$

The gate current $i_g(t)$ decreases from an initial value $2V_{GG}/R_g$. This current $i_g(t)$ includes two parts: the main part charges C_{gs}, and a negligible other part, compared to the first one, discharges C_{gd}. The drain current $I_D(t)$ is zero until the gate voltage $V_{GS}(t)$ raises the threshold voltage V_{th}. The supply voltage remains unchanged.

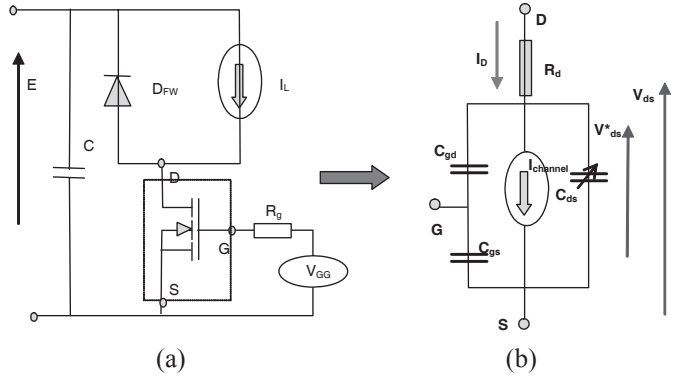


Figure 1.31. *Power circuit test and MOSFET equivalent circuit*

1.5.1.2. *Current rise time $t_{r(on)}$*

Drain current $I_D(t)$ starts when the threshold voltage V_{th} is rise. After that, $I_D(t)$ rises following the next law, when gate voltage $V_{GS}(t)$ increases:

$$I_D(t) = (V_{GS}(t) - V_{th})^2 \mu_{ns}.Z.\varepsilon_{ox}/ (2L.d_{ox})$$

Gate voltage $V_{GS}(t)$ increases in the same way as during the delay time:

$$V_{GS}(t) = V_{GG}\left[1 - 2e^{-\frac{t}{R_g(C_{gs}+C_{gd})}}\right] \approx V_{GG}\left[1 - 2e^{-\frac{t}{R_g C_{gs}}}\right] > V_{th}$$

Drain current increases until the current given by the circuit, $I_{ch} + I_{RM}$, rises. During this time, voltage $V_{DS}(t)$ remains at the same value E, and the voltage $V^*_{DS}(t)$ is almost $V_{DS}(t)$. Because the voltage drop inside R_d is tied, the drain current $I_D(t)$ is negligible. When the current I_D is equal to $I_{ch}+I_{RM}$, the following equation is given for the gate voltage $V_{GS}(t)$:

$$I_{ch} + I_{RM} = (V_{GS(Miller)on} - V_{th})^2 \mu_{ns}.Z.\varepsilon_{ox}/ (2L.d_{ox})$$

where $V_{GS(Miller)on}$ is Miller voltage at switch-on. Its value is high when $I_{CH} + I_{RM}$ is large.

1.5.1.3. *Voltage fall time $t_{v(on)}$*

When the load current $I_D(t)$ raises $I_{ch} + I_{RM}$, gate voltage still increases, and so $I_{channel}(t)$ tries to exceed the $I_D(t)$ value imposed by the load. A new relationship occurs between drain current and channel current: $\Delta I = I_{channel}(t) - I_D(t) > 0$. The C_{gd} and C_{ds} capacitances begin to discharge, and $V_{DS}(t)$ decreases. The fall in $V_{DS}(t)$ is given by the following equation:

$$\frac{dV_{DS}(t)}{dt} = \frac{-\Delta I + \frac{C_{gd}}{C_{gd}+C_{gs}} i_g}{C_{ds} + C_{gd} - \frac{C_{gd}^{\ 2}}{C_{gd}+C_{gs}}} \approx \frac{-\Delta I}{C_{ds}+C_{gd}}$$

Here the voltage drop inside R_d is neglected.

Capacitances C_{ds} and C_{gd} are weak at the beginning of the fall in $V_{DS}(t)$, so the initial speed of $dV_{DS}(t)/dt$ is very high, $V_{DS}(t)$ falls progressively, then the

capacitances are increasingly loaded, so the speed $V_{DS}(t)/dt$ becomes smaller and smaller.

When $V_{DS} = V_{GS} \approx 10V$, the capacitances increase substantially and dV_{DS}/dt is very small compared to the static conditions. In the end, gate current $i_g(t)$ is mainly used to charge the Miller capacitance C_{gd} while $V_{GS}(t)$ is quite constant. This phenomenon is called the "Miller effect". When $dV_{DS}(t)/dt = 0$, the Miller effect disappears and $V_{gs}(t)$ can increase up to V_{GG}. Thus:

$$V_{GS}(t) = V_{GG}\left[2e^{-\frac{t}{R_g(C_{gs}+C_{gd})}} - 1\right] > V_{GS(Miller)on}$$

1.5.2. *Switch-off study*

1.5.2.1. *Switch-off delay time $t_{d(off)}$*

Switch-off process is the reverse of the switch-on process. Drive voltage $V_{GG}(t)$ instantaneously goes from $+V_{GG}$ to a ground voltage $V_{GG} = 0$, or a negative voltage $-V_{GG}$. Gate voltage decreases as an exponential function given hereafter, and the gate current $i_g(t)$ increases from an initial value $-2V_{GG}/R_g$.

$$V_{GS}(t) = V_{GG}\left[2e^{-\frac{t}{R_g(C_{gs}+C_{gd})}} - 1\right] > V_{GS(Miller)off} > V_{th}$$

This delay phase occurs until the channel current $I_{channel}(t)$ is able to compensate the load current I_L. When the gate is discharged in such a way that the channel current cannot drive the load current, $V_{DS}(t)$ seriously increases, and so the switch-off delay time ends.

During this delay, the drain current is the load current $I_D(t) = I_L$, which also occurs in the conduction state.

If the gate voltage V_{GS} is defined, when $I_{channel} = I_L$, by $V_{GS(Miller)off}$, the following equation may be written:

$$I_{ch} = (V_{GS(Miller)on} - V_{th})^2 \mu_{ns}.Z.\varepsilon_{ox}/(2L.d_{ox})$$

where $V_{GS(Miller)off}$ represents the Miller voltage level at switch-off, as $V_{GS(Miller)on}$ for switch-on.

1.5.2.2. *Voltage rise time $t_{v(off)}$*

After the delay time, gate voltage tries to decrease, and $I_{channel}(t)$ has the tendency to be under the load current I_L. So, as for the switch-on, a potential inequality appears between $I_{channel}$ and the load current $I_L = I_D(t)$: $\Delta I = I_{channel}(t) - I_D(t) < 0$. C_{gd} and C_{ds} are discharged and V_{DS} can increase. The rate of increase is defined by:

$$\frac{dV_{DS}(t)}{dt} = \frac{-\Delta I + \frac{C_{gd}}{C_{gd}+C_{gs}} i_g}{C_{ds}+C_{gd}-\frac{C_{gd}{}^2}{C_{gd}+C_{gs}}} \approx \frac{-\Delta I}{C_{ds}+C_{gd}}$$

Note: the voltage drop inside R_d is neglected.

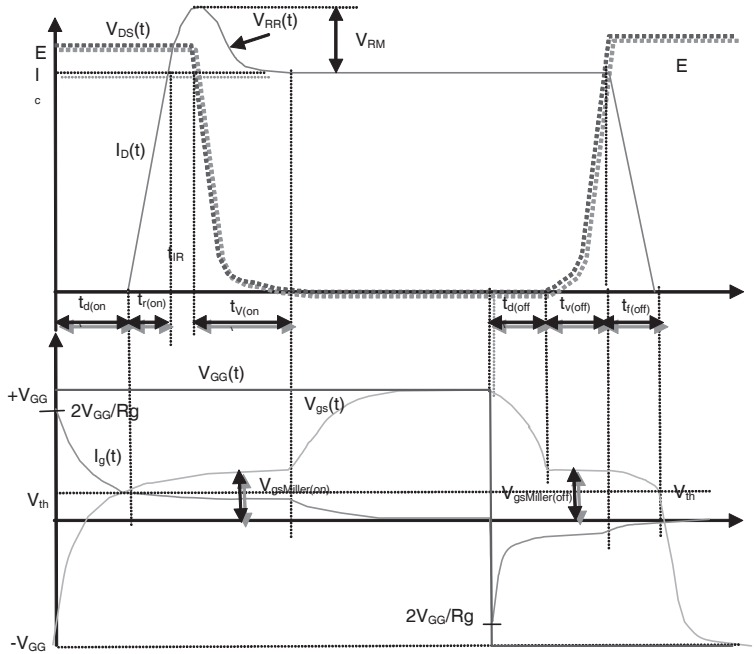


Figure 1.32. *Inductive load switching waveforms*

At the beginning of the V_{DS} voltage rise time, C_{gd} and C_{ds} are large and $dV_{DS}(t)/dt$ is a gradual increase in speed. When $V_{DS}(t)$ increases, capacitances become weaker and the $dV_{DS}(t)/dt$ becomes increasingly larger.

During this time, the C_{gs} discharge current is compensated for by the C_{gd} charge current, maintaining quite a stable V_{gs}: this same Miller effect occurs during switch-on.

The switch-off $t_{v(off)}$ voltage rise time stops when $V_{DS}(t) = E$, the supply voltage.

1.5.2.3. *Fall time current $t_{f(off)}$*

When $V_{DS}(t) = E$, $dV_{DS}(t)/dt = 0$, and the Miller effect disappears.

Thus, the gate can be normally discharged. The load current can now decrease until the gate voltage goes down to zero:

$$I_D(t) = I_{channel}(t) = (V_{GS}(t) - V_{th})^2 \mu_{ns}.Z.\varepsilon_{ox}/(2L.d_{ox})$$

$$V_{GS}(t) = V_{GG}\left[2e^{-\frac{t}{R_g(C_{gs}+C_{gd})}} - 1\right] < V_{GS(Miller)off}$$

Tables 1.1 and 1.2 sum up the various states of $V_{DS}(t)$, $I_{DS}(t)$ and $V_{GS}(t)$ during one switching cycle on inductive load.

For this analysis, the inductive parasitic effects were neglected. Parasitic inductances are not only in the power circuit, but also in the drive loop. Thus, the waveforms given by Figure 1.32 are slightly inaccurate.

Due to C_{gd}, the Miller effect is all the time in opposition to any gate voltage variation. At switch-on, V_{DS} decreases, dV_{DS}/dt is negative and a current, i_{CGD}, is extracted from the gate. At switch-off, V_{DS} increases and injects a current, i_{cgd}, into the gate.

If the gate current is very large, the Miller effect is quite negligible, and the V_{GS} "plateau" during switch-on and switch-off may disappear.

The equation for $dV_{DS}(t)/dt$ is still the same but $V_{GS}(t)$ varies during $t_{v(on)}$ and $t_{v(off)}$, according to the following laws:

$$(C_{gs} + C_{gd}).\, dV_{GS}/dt = C_{gd}.\, dV_{DS}/dt + i_g$$

$$\text{and} \qquad R_g.i_g + V_{GS} = V_{GG}$$

<table>
<tr><td colspan="4">SWITCH-ON</td></tr>
<tr><td rowspan="2">$t_{d(on)}$</td><td>$V_{DS}(t) = E$</td><td colspan="2">$I_D(t) = 0$</td></tr>
<tr><td colspan="3">$V_{GS}(t) = V_{GG}\left[1 - 2e^{-\frac{t}{R_g(C_{gs}+C_{gd})}}\right] \approx V_{GG}\left[1 - 2e^{-\frac{t}{R_g C_{gs}}}\right] < V_{th}$</td></tr>
<tr><td rowspan="2">$t_{r(on)}$</td><td>$V_{DS}(t) = E$</td><td colspan="2">$I_D(t) = \frac{Z}{2L}\mu_{ns}\frac{\varepsilon_{ox}}{d_{ox}}(V_{GS}(t) - V_{th})^2$</td></tr>
<tr><td colspan="3">$V_{GS}(t) = V_{GG}\left[1 - 2e^{-\frac{t}{R_g(C_{gs}+C_{gd})}}\right] \approx V_{GG}\left[1 - 2e^{-\frac{t}{R_g C_{gs}}}\right] > V_{th}$</td></tr>
<tr><td rowspan="2">$t_{V(on)}$</td><td colspan="3">$\frac{dV_{DS}(t)}{dt} = \frac{-\Delta I + \frac{C_{gd}}{C_{gd}+C_{gs}} i_g}{C_{ds} + C_{gd} - \frac{{C_{gd}}^2}{C_{gd}+C_{gs}}} \approx \frac{-\Delta I}{C_{ds}+C_{gd}}$</td></tr>
<tr><td>$I_D(t) = I_{Ch} + I_{RR}$</td><td colspan="2">$V_{GS} = V_{gs(Miller)on}$</td></tr>
<tr><td colspan="4">ON STATE</td></tr>
<tr><td></td><td>$V_{DS} = I_{Ch} \cdot R_{Dson}$
$= I_{Ch} \cdot (R_v + R_a + R_{channel})$</td><td>$I_D(t) = I_{Ch}$</td><td>$V_{GS} = +V_{GG}$</td></tr>
</table>

Table 1.1. *Various parameters variation during switch-on for an inductive load*

<table>
<tr><td colspan="4">SWITCH-OFF</td></tr>
<tr><td rowspan="2">$t_{d(off)}$</td><td colspan="2">$V_{DS} = I_{Ch} \cdot R_{Dson}$
$= I_{Ch} \cdot (R_v + R_a + R_{channel})$</td><td>$I_D(t) = I_{Ch}$</td></tr>
<tr><td colspan="3">$V_{GS}(t) = V_{GG}\left[2e^{-\frac{t}{R_g(C_{gs}+C_{gd})}} - 1\right] > V_{GS(Miller)off} > V_{th}$</td></tr>
<tr><td rowspan="2">$t_{V(off)}$</td><td colspan="3">$\frac{dV_{DS}(t)}{dt} = \frac{-\Delta I + \frac{C_{gd}}{C_{gd}+C_{gs}} i_g}{C_{ds} + C_{gd} - \frac{C_{gd}{}^2}{C_{gd}+C_{gs}}} \approx \frac{-\Delta I}{C_{ds}+C_{gd}}$</td></tr>
<tr><td colspan="2">$I_D(t) = I_{Ch}$</td><td>$V_{GS} = V_{gs(Miller)off}$</td></tr>
<tr><td rowspan="2">$t_{f(off)}$</td><td>$V_{DS}(t) = E$</td><td colspan="2">$I_D(t) = \frac{Z}{2L}\mu_{ns}\frac{\varepsilon_{ox}}{d_{ox}}(V_{GS}(t) - V_{th})^2$</td></tr>
<tr><td colspan="3">$V_{GS}(t) = V_{GG}\left[2e^{-\frac{t}{R_g(C_{gs}+C_{gd})}} - 1\right] < V_{GS(Miller)off}$</td></tr>
<tr><td colspan="4">SWITCH-OFF STATE</td></tr>
<tr><td colspan="2">$V_{DS}(t) = E$</td><td>$I_D(t) = 0$</td><td>$V_{GS} = -V_{GG}$</td></tr>
</table>

Table 1.2. *Various parameters variation during switch-off for an inductive load*

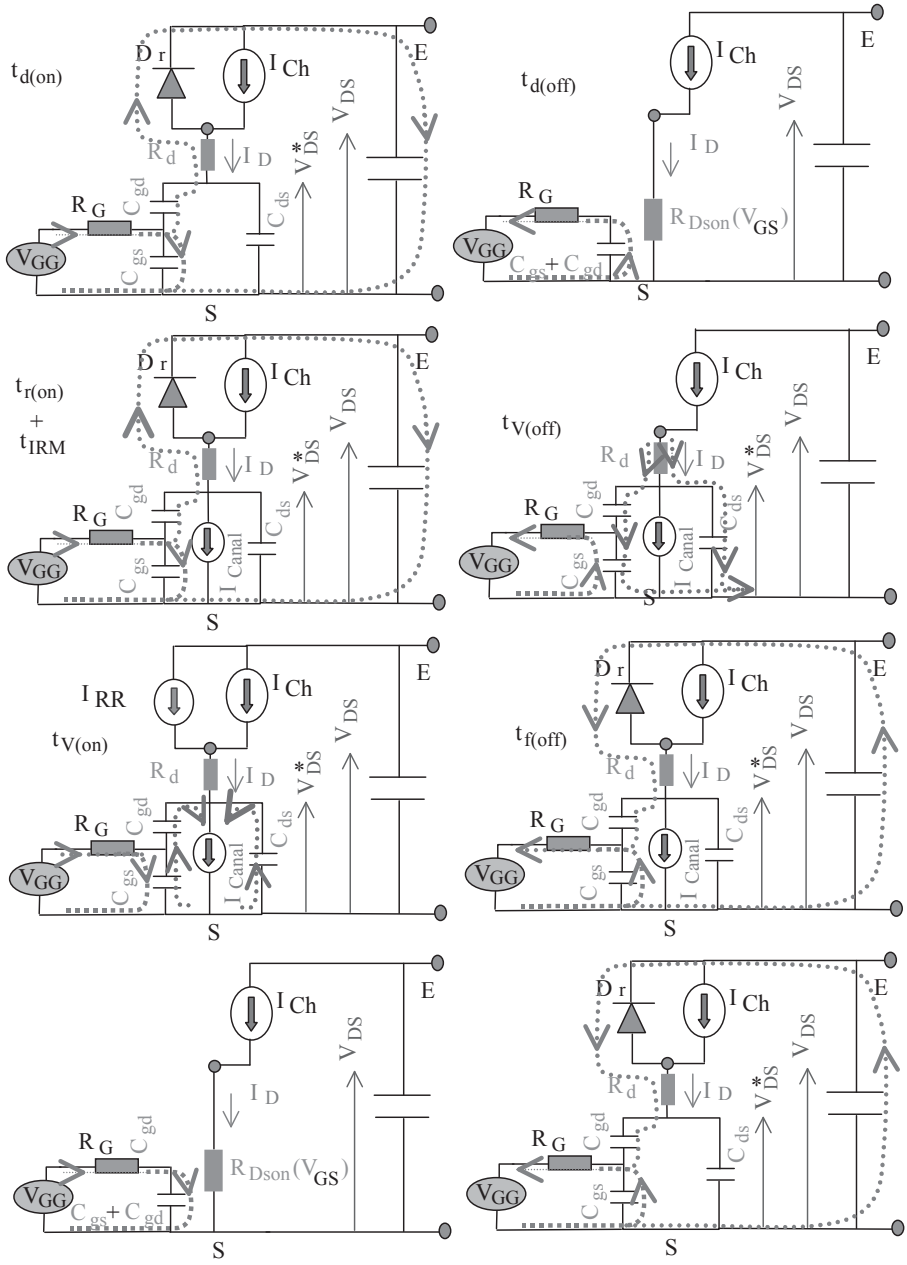


Figure 1.33. *Currents through capacitances Cgs, Cgd and Cds, during one switching cycle, on inductive load, with hard commutation*

1.6. Characteristic variations due to MOSFET temperature changes

The power electronics thermal aspects are of as much importance as the pure electrical aspects, mainly because electrical parameters change with temperature. In a power MOSFET, several parameters are sensitive to the die temperature:

– Kp transconductance, because the surface electrons mobility μ_{ns} decreases according to the following law:

$$\mu_n (T_j)/\mu_n(T_{jo}) = (T_j/T_{j0})^{-1.5}$$

– drift zone resistivity $\rho_v = 1/ q.\mu n.ND$. Due to the electron volume mobility reduction, μ_n increases with temperature according to:

$$\mu_n (T_j)/\mu_n(T_{jo}) = (T_j/T_{j0})^{-2.5}$$

– threshold voltage V_{th} decreases by 6 mV/°C, due to Fermi potential;

– power MOSFET in conduction is characterized by its internal resistance R_{DSon}, which is the sum of three resistances:

- channel resistance, R_{ch},
- access resistance, R_{acc}
- and drift zone resistance, R_v

For low voltage power MOSFET (<100 V), channel resistance, R_{ch} is the most important. Drift zone resistance, R_v is, however, of greater importance for medium and high voltage power MOSFETs (>400 V). Thus, the theoretical resistance R_{dson} versus temperature, from the mobility evolution, can be given by:

$$R_{DSon} (T_J) = R_{DSON}(T_{jo}) (T_j /T_{jo})^{\alpha}$$

where the temperature is given in Kelvin degrees, and where $\alpha = 1.5$ for low voltage MOSFET (<100 V) and $\alpha = 2.5$ for medium and high voltage power MOSFETs (>400 V).

The previous equation may also be written:

$$R_{DSon} (T_j) = R_{DSon} (25°C). (1+ \alpha. \Delta T/ 300)$$

where ΔT, in °C, is the increase of temperature from 25°C. This equation really shows the positive temperature coefficient of power MOSFETs.

Figure 1.34 shows characteristics versus temperature for a 500 V power MOSFET. We can see that between 25°C and 125°C, R_{DSon} doubles while V_{th} reduces by 25%.

For the transfer characteristic, two parameters are in opposition when temperature increases: decreases V_{th}, contrasting the rise of dI_D/dT_j. For the same V_{GS}, reduction of the transconductance parameter K_p has the opposite effect. Thus, dI_D/dT_{jh} includes two reverse behaviors in temperature, versus I_D current.

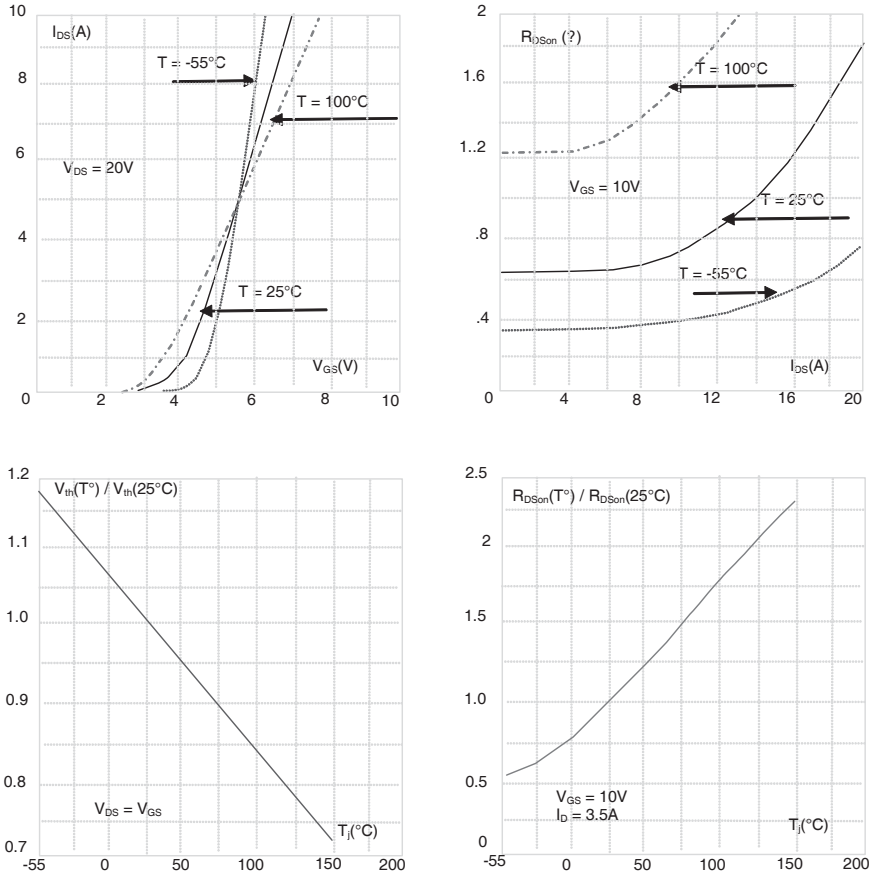


Figure 1.34. *500 V, 7 A, 8 Ω MOSFET characteristics versus temperature*

Switching characteristics show very few variations versus temperature, because V_{th} has a minimal reaction, and the power MOSFET capacitances are insensitive to

temperature. Variation speeds $dI_D(t)/dt$ and $dV_{DS}(t)/dt$ do slow down with temperature, because the parameter of transconductance Kp is reduced.

1.7. Over-constrained operations

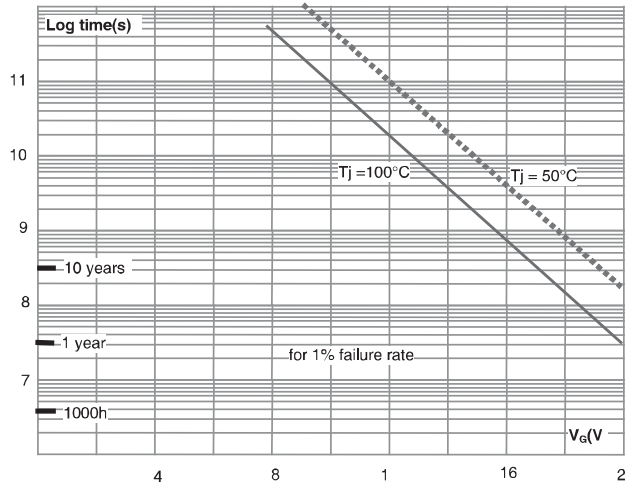


Figure 1.35. *MOS lifetime versus gate voltage V_{GS}*

1.7.1. *Overvoltage on the gate*

Despite a maximum gate voltage of 70 V for an oxide thickness of 100 nm, manufacturers specify a gate voltage V_{GS} limited to 20 V.

Two reasons justify this limitation. On the one hand, Figure 1.35 shows that power MOSFET lifetime decreases substantially when V_{GS} increases. On the other hand, V_{GS} over 20 V gives nothing more for the power MOSFET. So, an overvoltage protection must be set between the gate and the source.

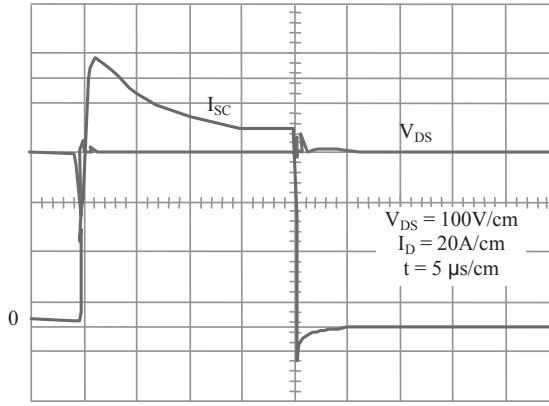


Figure 1.36. *Short circuit on a 500 V, 14 A, 0.4 Ω MOSFET*

1.7.2. *Over-current*

Short circuit is the most common and the most constraining overload, because the device must sustain both the supply voltage and a large drain current I_D in concert. If the current density in the die is considered uniform, and if the critical field in silicon is the cause of the failure, then the electric field is reversed in the N-N+ junction, and the theoretical current density versus short circuit voltage is given by:

$$J_D = q.N_D v_{ns} + v_{ns}.\varepsilon_{si}.E_{simax}^2/2V_{DS}$$

where v_{ns} is the saturation speed of the electrons (10^7cm/s).

If a doping level of $N_D = 4.10^{14}$ cm^{-3} is applied on a 500 V power MOSFET, the critical field E_{simax} is $2.7.10^5$ V/cm, and the critical current density is around 1745 A.cm^{-2} for a voltage of 70% of the maximum voltage (1415 A.cm^{-2} at 100% of V_{DSS}). This value is at least 30 times higher than the nominal current density, which is very far away from the normal short circuit current with a gate voltage under 20 V. So, from an electrical point of view, power MOSFETs can easily sustain a short circuit current with a gate voltage under 20 V, and a supply voltage equal to V_{DSmax}.

Figure 1.36 shows a short circuit with V_{GS} = 15 V for a 500 V, 14 A, 0.4 Ω power MOSFET, including two dies of 25.5 mm^2 each, combining to create 51 mm^2, and so a current density of 220 A.cm^{-2}.

The time the power MOSFET can sustain the short circuit current is only limited thermally. In Figure 1.36, we can see that the short circuit current decreases with time (or increase of temperature), because the channel current decreases with the surface mobility of electrons, which decreases with temperature.

With some simplifications, the approximate dissipated energy in silicon is:

P_{sc} = 350 V x 90 A = 31.5 kW, according to the thermal impedance chart specified for this device.

In Figure 1.37, the maximum temperature rise at the end of the short circuit is:

$$T_j = Z_{th}.P_{sc} + T_c = r(t).\ R_{th(j\text{-}c)}.P_{sc} + T_c = 0.01 \text{ x.7 x } 31.5.10^3 + 25 = 245.5°C,$$

which is not very far away from the critical temperature of silicon:

$$300°C \text{ for } N_D = 4.10^{14} cm^{-3}.$$

When the short circuit current duration is short (<50 µs), we can consider that the energy is adiabatically dissipated inside the small die. The volume of silicon involved corresponds to the space charge volume: W_{ZD} x S_{Si} where W_{ZD} is a function of the short circuit voltage, thus giving:

$$W_{ZD} = \sqrt{\frac{2\varepsilon_{si} V_{DS}}{qN_D}}$$

The maximum temperature in silicon may be estimated as a function of the dissipated energy W_j as shown below:

$$T_j = \frac{W_J}{k_{Si} W_{ZD} S_{Si}} + T_c \qquad \text{with} \qquad W_J = \int_0^{t_{cc}} I_D(t) V_{DS}(t) dt$$

where K_{SI} is the volume calorific capacity of silicon, around 1.767 J $°C^{-1}$. cm^{-3}.

With the previous MOSFET (S_{SI} = 51 mm^2, Z_{ZD} = 34 µm, W_j = 0.63 J), the short circuit current makes a temperature at the short circuit end of 231°C, which is the same as the previous result.

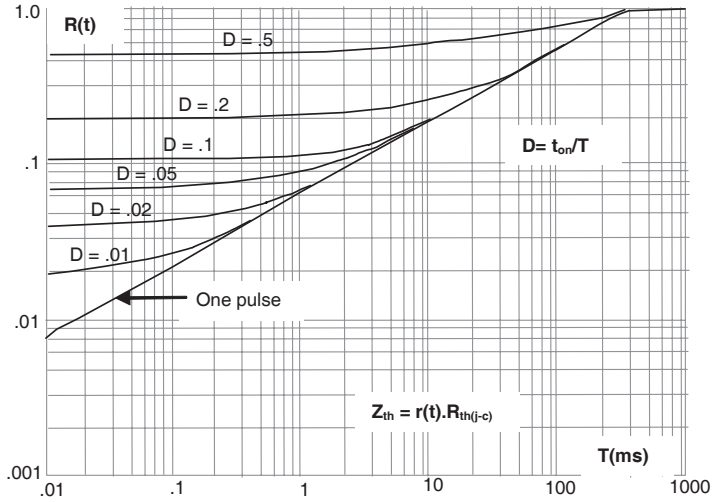


Figure 1.37. *Transient thermal resistance for 500 V, 14 A, 0.4 Ω MOSFET*

1.7.3. *Avalanche sustaining*

Avalanche occurs when the supply voltage connected on the device is over its maximum allowable voltage, which is generally slightly higher than the specified maximum voltage given in the data sheet, shown in Figure 1.38. From a physical point of view, avalanching means the beginning of a non-controlled process, which is more or less a failure activation.

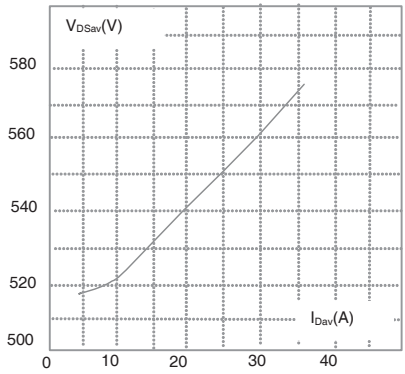


Figure 1.38. *Breakdown voltage versus drain current for a 500 V, 36 A, 0.13 Ω MOSFET*

Nevertheless, if the avalanching current remains under a value which does not lead to too great an increase of silicon temperature, this phenomenon may be reversible. The reason for this is the absence, in a power MOSFET, as a unipolar conduction device, of any second breakdown voltage. In other words, there are no hot spots.

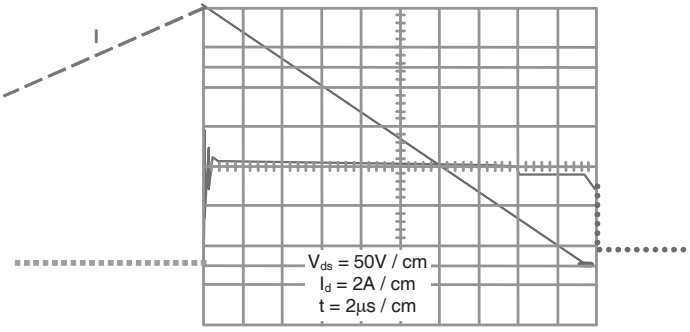


Figure 1.39. *Avalanche test on a 100 V, 12 A, 0.33 Ω MOSFET*

In the data sheets, the avalanche characteristic is shown as a maximum energy that the device is able to sustain at switch-off. The test is done with an inductance of few millihenries, without a free-wheeling diode, depicted in Figure 1.39. This figure shows the device can sustain an avalanche during 20 µs, with 12 A and 130 V, thus an energy of W = 0.016 J. Avalanche phenomenon is dangerous for power semiconductors due to possible lifetime degradation. So, this manufacturer's characteristic should be considered only as an accidental overvoltage strength.

1.7.4. *Use of the body diode*

Power MOSFETs have a structural body diode which may be used as a free-wheeling diode.

It should be interesting to use this diode in a lot of power applications, like ZCS (Zero Current Switch), in soft switching or in hard switching applications, where this diode can be used as a free-wheeling diode. Unfortunately, failures may occur and some limitations must be introduced.

Figure 1.40 shows the diode switch-off and the voltage application. Sometimes, when the speed of application of the supply voltage is over a few kV/µs, a failure appears inside the device. Even today, a true explanation for this phenomenon is still unknown. Maybe, the parasitic bipolar transistor inside the MOSFET is the cause of the failure, but some experiments do not seem in accordance with this explanation.

A large electric field, with a huge gradient, is applied inside the die: this leads to constraints applied on the peripheral of the die, and on the lithography. This could also play a role in explaining failure.

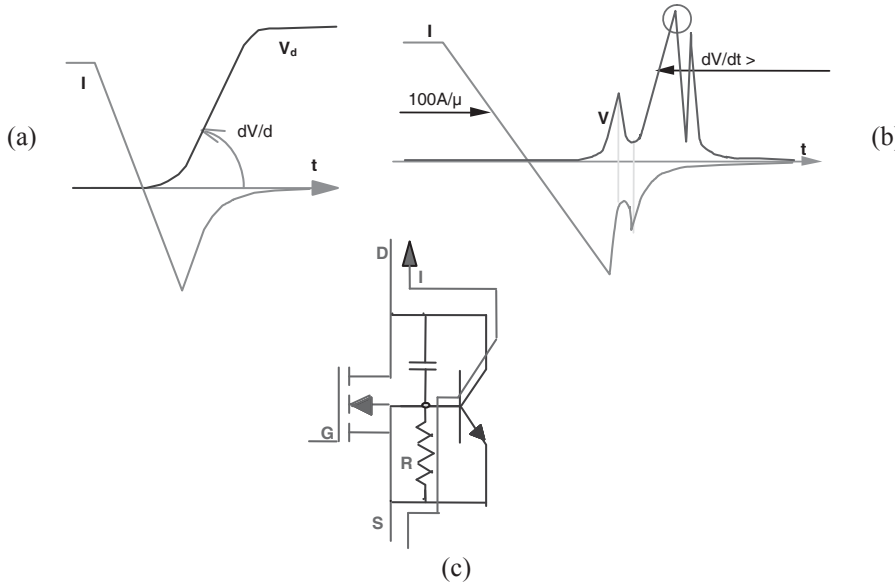


Figure 1.40. *Body diode recovery;*
(a) good recovery; (b) MOSFET fails; (c) parasitic bipolar transistor

1.7.5. *Safe operating areas*

If only the physics of silicon is considered, and if the maximum junction temperature is respected in the die, the theoretical current density is much higher than the load current, even in short circuit. So, in terms of current density in the device, the probability of failure is very low. Practically, due to technological aspects like current density dispersion between cells, packaging, and maximum temperature of various elements, allowable maximum current density is much lower. So, various safe operating graphs are specified in order to guarantee the device lifetime. Two of them are shown in Figure 1.41: the Forward Bias Safe Operating Area (FBSOA) and the Switching Safe Operating Area (SSOA). The same maximum pulsed current, I_{DMmax}, is specified in these two charts: this maximum value is mainly limited by contact devices like bounding wire diameter, metallization and thermal resistance of the encapsulated device. I_{DMmax} is around two to six times the nominal current, and is weaker than the short circuit current. In the

following graph, we can see that the I_{DMmax} is 4.3 times the nominal current, with a current density of 118 A.cm^{-2}. Nevertheless, this device sustained around 160 A.cm^{-2} during short circuit.

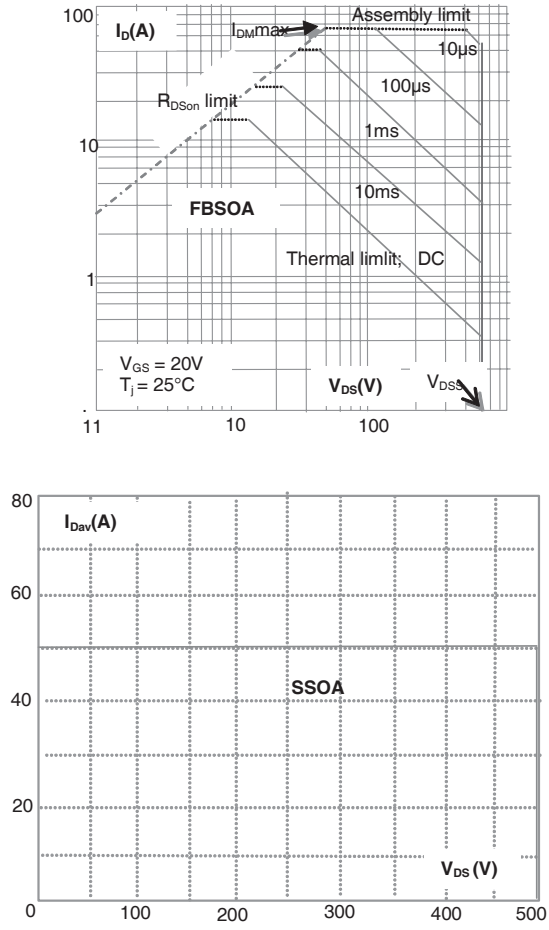


Figure 1.41. *500 V, 14 A, 0.4 Ω MOSFET safe operating areas*

For the FBSOA, four limits can occur:

The maximum sustaining voltage, V_{DSS}. Normally, this is specified slightly under the avalanche voltage of the die, but a voltage applied over this value is not good for device lifetime.

The junction temperature limit, which is generally between 150°C and 175°C. This limit decreases when the pulse duration (Δt) increases. Maximum dissipated energy in the die is:

$$W = U.I.\Delta t$$

and is constant for a same die size.

The maximum current, I_{DM}, also varies with the pulse width, due to the same thermal limitations: requested time for the thermal energy to reach the wires during short pulses, and maximum thermal capacity of the elements.

R_{DSon} limit varies because the voltage drop on the MOSFET is limited by: $I_D . R_{DSon}$.

1.8. Future developments of the power MOSFET

Voltage drop of power MOSFET is defined by R_{DSon}, and dynamic performances by the gate oxide. Thus, the main target, for designers, is to reduce internal resistance and capacitance, keeping ruggedness of the MOSFET at least at the same level.

In a low voltage power MOSFET, the main part of R_{DSon} is set by the channel and access resistances. Thus, cell density should be increased. However, a JFET then appears between adjacent cells, which limits the available current when cells are too close. The technological limit is around 45,000 cells/mm^2. Thus, a vertical gate is the current solution for channel resistance reduction, depicted in Figure 1.42.

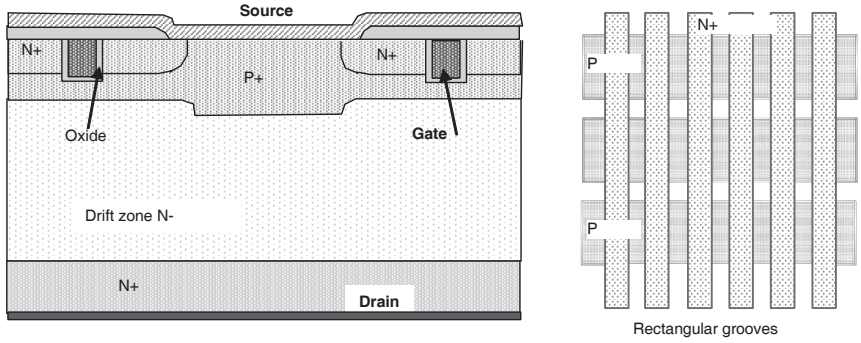


Figure 1.42. *Trench gate MOSFET*

RMOS from Matsushita, and RMOS, or Trench Gate from General Electric, provided the solution: a vertical way for current avoids any access resistance, and the short distance of the gate oxide close to N- makes a low $C_{gd,}$ through C_{oxd} reduction. Gate grooves cannot be as close as could be expected, as P+ contact needs enough place. An enhancement was made by crossing gate grooves, N+ sources and P well. The gate groove is approximately 3 µm in width, with an approximate 5 µm spacing around. Substrate resistance is around 10% of the total resistance of a low voltage MOSFET: its thickness is designed in order to insure the mechanical resistance of the wafer. A new technology, called "thin wafer", could provide further improvement of R_{DSon}.

For a high voltage power MOSFET, R_{DSon} is mainly due to the N- drift zone. Its resistivity is tied to the sustaining voltage, so there are few possibilities for resistance improvement.

Recent research into bipolar diodes led to the discovery of a new technology called "superjunction", which may dramatically improve drift zone resistance. The trade names for these new MOSFET are "Coolmos" or "MDmesh". P+ and N+ islands are introduced into the N- region in order to decrease the R_{DSon}, for the same breakdown voltage, as shown in Figure 1.43.

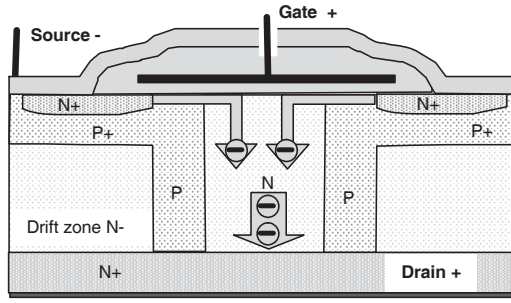


Figure 1.43. *"Superjunction" MOSFET*

At the beginning of switch-off, space charge starts between the N+ and P+ islands, and at the completion of switch-off this space charge spreads out into the total drift zone. The electric field is not only in the vertical part, but also in the horizontal part: this leads to a tri-dimensional structure. Thus, N- drift zone resistivity is no longer tied to $V_{DSS}^{2.5}$. This new technology divides the R_{DSon} of medium and high voltage power MOSFETs by an approximate factor of five. This makes them competitive compared to 500 V IGBT, but also compared to 1,000 V IGBT. The R_{Dson} of a 1,000 V MOSFET may be in the range of 0.2 Ω.cm, at 100°C. This means a voltage drop of around 2 V, with a drain current of 10 A.

The main drawback is the cost of such a technology, where P+ and N+ islands must be introduced in the N- zone.

In a high voltage power MOSFET, the Miller capacitance C_{gd} may also be reduced by decreasing the gate oxide capacitance C_{oxd} over the N- drain. For this, oxide thickness over the N- zone is increased. This technology requires sufficient space between cells, which can only be made within high voltage devices, as shown in Figure 1.44.

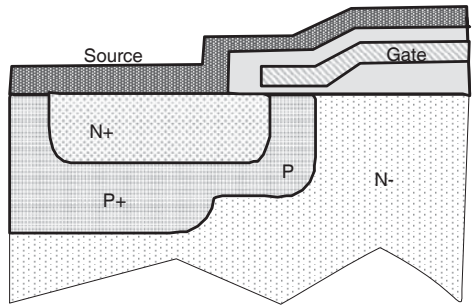


Figure 1.44. *"Up gate" MOSFET*

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Chapter 2

Insulated Gate Bipolar Transistors

2.1. Introduction

MOSFETs and bipolar power transistors show complementary characteristics. On the one hand, bipolar junction transistors (BJT) show a low voltage drop, mainly for high voltage devices; however, the base drive needs a drive current, and they are weak close to their limits. On the other hand, power MOSFETs are very fast for switching operations, strong in overload operations, and the gate drive only requires very low energy (a voltage drive). However, for high voltage devices, MOSFET internal resistance is high, leading to a large voltage drop. As the useful characteristics of both BJTs and MOSFETs were required, manufacturers conjugated the two to create a new device, the insulated gate bipolar transistor (IGBT). After 20 years of consistently good performance IGBT was close to having a monopoly on the market of high voltage applications, from 1 kV to 8 kV, also replacing GTO for some applications.

Devices from a few amps to kilo-amps are today allowable on the market, in several packages. Good adaptation between IGBTs and applications is also allowable: some IGBTs have a low voltage drop but quite slow commutations, while other devices are very fast, with a higher voltage drop.

Chapter written by Pierre ALOÏSI.

2.2. IGBT technology

2.2.1. *IGBT structure*

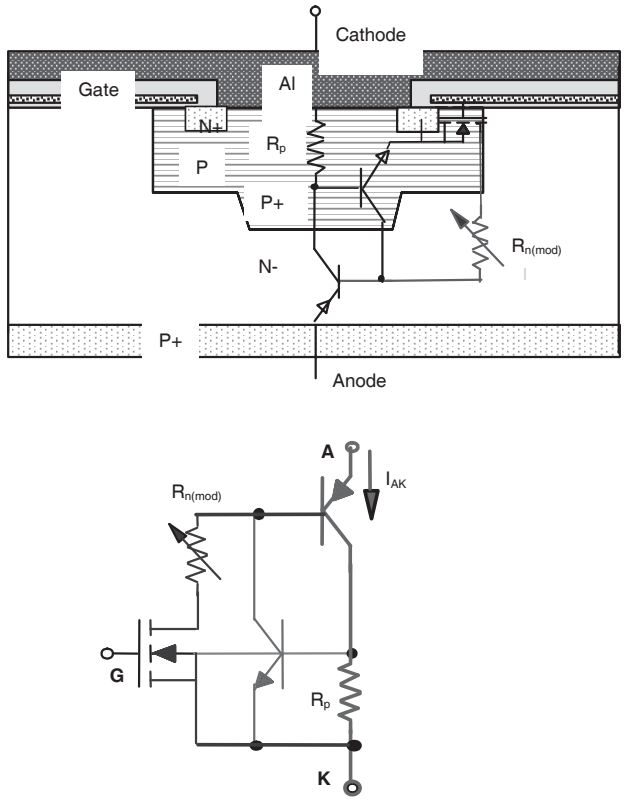


Figure 2.1. *IGBT structure*

Figure 2.1 shows the vertical section of an IGBT: it is like a power MOSFET construction, but N+ MOS substrate is replaced by a highly doped P+ substrate. The new P+ N- junction injects some holes into the N- drift zone, which is modulated by electrons coming from the channel. The equivalent circuit is also shown in Figure 2.1, where the parasitic JFET and the internal capacitances are not revealed. The main elements of the structure are:

– the bipolar PNP where the emitter is the P+ layer (IGBT anode or collector), the base is the drift zone N- layer, and the P+ well is the collector;

– the NPN parasitic transistor where the emitter is the N+ source (IGBT cathode or emitter), the base is the P+ well, and the collector is the N- zone;

– two resistances, R_p and R_{mod}, which are the resistance of the Pwell under the source, and modulated resistance of the N- drift zone;

– the channel.

The two NPN and PNP transistors are connected in such way that they represent a four layer structure, called a thyristor. This is a positive feedback device, which means that once started, it cannot be switched off. As this is the case, the thyristor should not be switched on, in order to avoid any IGBT failure. There are two possible options for avoiding IGBT failure.

The first option is to set the gain of the PNP transistor at only the value requested for the IGBT main characteristics, and dramatically reduce the sheet resistance R_p, in order to maintain the veracity of the following inequality:

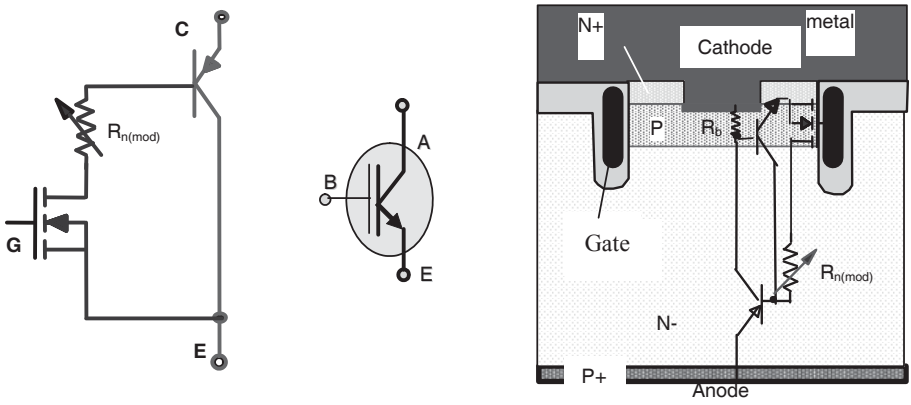
$$R_P \cdot I_{C(PNP)} = R_P \cdot \frac{\beta_{PNP}}{1+\beta_{PNP}} \cdot I_{C\max} < 0.6\ V$$

$$\text{which gives} \qquad R_P < \frac{1+\beta_{PNP}}{\beta_{PNP}} \cdot \frac{0.6}{I_{C\max}}$$

I_{Cmax} is the thyristor latching current. Beyond it, IGBT switch-off is impossible, and the device is destroyed.

R_p reduction requires a shorter source length, with a higher Pwell doping level. P/P+ diffusion technique allows increased doping levels between and under sources, keeping the adequate channel doping level in line with the threshold voltage, Vth.

A second way is to reduce the I_C(PNP) current through R_p by decreasing the gain of the PNP transistor, β_{PNP}. But this gain sets the injection levelof the holes, and consequently the resistivity modulation in the N- drift zone. So, the device designer has to make a compromise: a low gain to cancel the thyristor operation or a high gain for low V_{CEsat}.



(a) (b) (c)

Figure 2.2. *IGBT equivalent circuit, symbol and trench gate IGBT*

Figure 2.2 shows the IGBT equivalent circuit, when the NPN transistor is technologically cancelled, and the series resistance R_p is very low. A bipolar PNP transistor remains, driven by a MOSFET with an internal resistance, R_{MOD}. The common IGBT symbol is also shown.

This equivalent circuit shows that the MOSFET is always a low voltage MOSFET, connected between the PNP transistor base and the collector. Load current is divided between MOS and the bipolar transistor: meaning a very low MOSFET R_{dson} is welcomed to obtain a low IGBT V_{sat}. Today, most IGBTs are built with a trench gate MOSFET (see Figure 2.2c). The Pwell is a very thin layer, short-circuited by the source (emitter) metallization. Thus, on modern IGBTs, R_p is close to zero.

2.2.2. *Voltage and current characteristics*

It is mainly the PNP bipolar transistor, with an opened base, that gives the IGBT maximum voltage. When a supply voltage is applied on the IGBT, the drift zone is divided into two regions. The first region, W_m, is close to the IGBT collector, and has a weak injection level, due to the PNP emitter-base junction forward polarization. A second region, W_{ZD}, is a space charge region, close to the MOSFET (PNP collector), and is a product of the junction P+N- reverse polarization, (see Figure 2.3). Total current I_A, at the space charge output, is the sum of two currents: a

generation current I_{gen} in the space charge region, and an injected current from the weak injection region in the space charge. This is then multiplied by M in the space charge region, as seen in the following equation:

$I_A = \gamma_{PE}.\alpha_{Tm}.I_A.M + I_{gen}.M$ which gives: $I_A = I_{gen}.M.(1-\gamma_{PE}.\alpha_{Tm}.M)^{-1}$

where γ_{PE} is the P+N-P transistor emitter injection coefficient, and α_{Tm} is the effective base W_m transport coefficient, with a low injection level, less than one. Actually, it represents the ratio between the hole current at the output and at the input region W_m:

$$a_{Tm} = \frac{1}{\cos\frac{W_m}{L_p}}$$

where L_p is the hole diffusion constant in the $W_{m.}$ region.

When $\gamma_{PE}.\alpha_{Tm}.M > 1$, avalanche occurs giving

$$M = (\gamma_{PE}.\alpha_{Tm})^{-1}.$$

If the well known expression:

$$M = \left[1 - \left(\frac{V_{app}}{V_{DSS}}\right)^n\right]^{-1}$$

is used, the ratio between the two structures sustaining voltages, V_{CES} for PNP transistor and V_{DSS} for MOSFET is:

$$V_{CES} = (1 - \gamma_{P_E}.\alpha_{Tm})^{\frac{1}{n}} \cdot V_{DSS}$$

where n is between 4 and 6 for a P+N junction, and between 2 and 4 for the N+P junction.

Thus, the IGBT sustaining voltage is slightly less than that of a MOSFET with the same N- thickness.

For example: if $\gamma_{PE} = 0.8$ and $\alpha_{Tm} = 0.5$, $V_{CES} = 0.8V_{DSS}$ with n = 5

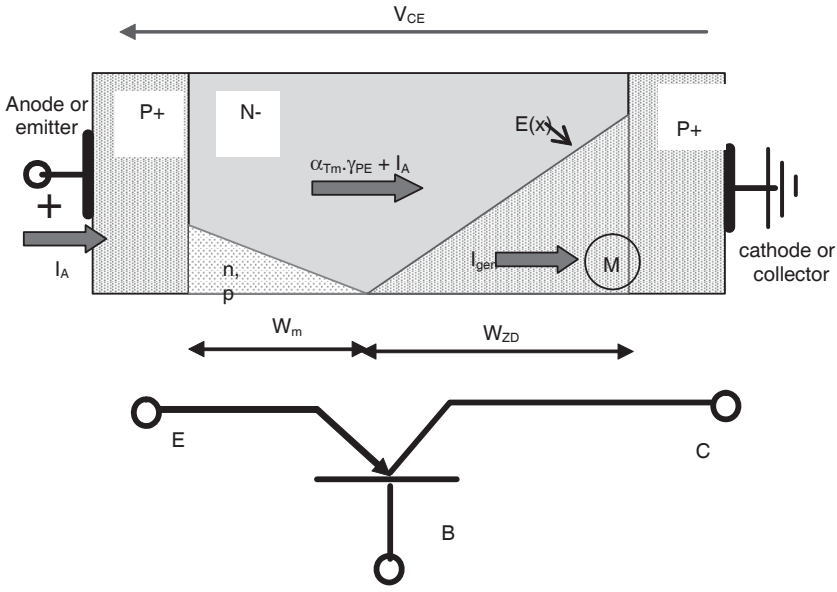


Figure 2.3. *IGBT static sustaining voltage*

The thermal aspects of the system mainly define the maximum current limitation for both IGBT and power MOSFET. Current density in the IGBT is larger when the voltage drop and thermal resistance are lower. If the following equation is true:

$$J_{AK} = \frac{T_j - T_{env}}{R_{th(j-c)} V_{AK}}$$

the theoretical current density is around 330 A.cm^{-2}, for:

– a silicon maximum temperature of $T_j = 150°C$,

– an ambient temperature $T_{amb} = 50°C$,

– a thermal resistance per square centimeter of silicon of 0.1°C/W (quite impossible to obtain),

– and a voltage drop of 3 V.

Normally, in a 1,000 V IGBT, the maximum current density is around 50 to 150 A.cm^{-2}, and 100 to 200 A.cm^{-2} in a 600 V IGBT. Recall that the current density in a 1,000 V power MOSFET is only a few A.cm^{-2}.

2.3. Operation technique

2.3.1. *Basic principle*

IGBTs are used in bipolar power devices. Two types of carriers, holes and electrons, transport the current through the drift zone of the device. The channel drives electrons when a gate voltage over the threshold voltage is applied. The anode P+N- junction injects holes when a positive voltage is applied between the anode and cathode of IGBT. Electrons and holes move in opposite directions inside the drift zone, electrons to the anode and holes to the cathode. At the end of N- drift zone, some of the electrons enter the P+ anode. Simultaneously, some of the holes come into the Pwell. The difference between incoming and outgoing electrons, discounting recombination, is the Q stored charge in the drift zone. Because of electrical neutrality, the difference between holes is the same as the difference between electrons; these stored charges modulate the drift zone in the on-state. Figure 2.4 shows this exchange of charges in the on-state IGBT.

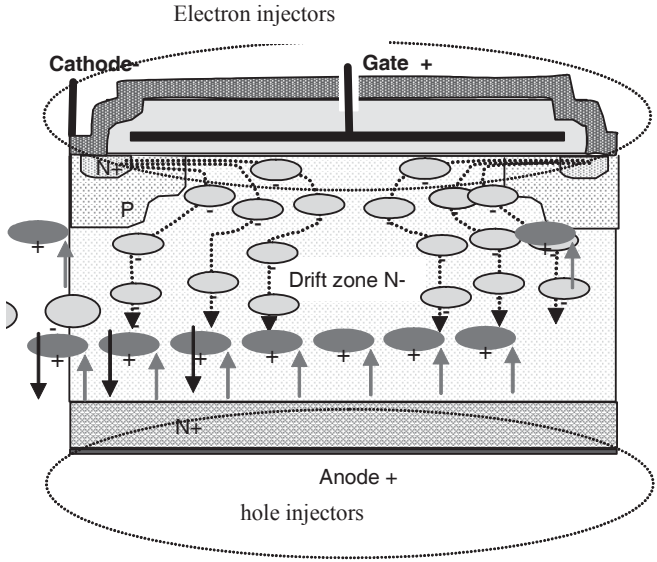


Figure 2.4. *Charge injection during on-state*

At switch-off, gate voltage decreases, and the electron injection stops when the gate voltage becomes lower than the threshold voltage V_{th}. In order to really switch-off the IGBT, stopping the electron injection is not enough, the stored charge Q (electrons and holes in equal quantity) must also be cleared out. Removal of these

charges (sometimes called "trapped charges") at the PNP base is impossible, because it opens when MOS is switched off. Thus, they should recombine on site (see Figure 2.5).

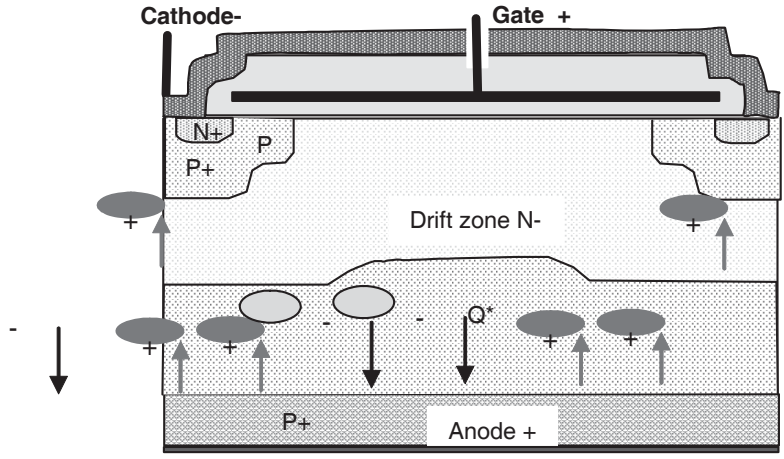


Figure 2.5. *Recombination of charges during switch-off*

2.3.2. *Continuous operation*

During "on" time, the load imposes an anode current I_A equal to the cathode current. Inside the device, this cathode current is driven by the electron current coming from the channel, and the hole current coming from the drift zone and P+ well. The anode current is comprised of the electron current coming from the drift zone, and the hole current coming from the PNP emitter. Stored charge Q is created by the difference between electrons coming from the channel and those entering in the P+ injector (or by the difference between the holes coming from the PNP emitter and those entering the Pwell), minus the electrons (or holes) recombined on site. If $J_{n(K)}$ and $J_{P(K)}$ are the current densities at the cathode end and $J_{n(A)}$ and $J_{P(A)}$ are the current densities at the anode end, the stored charge per square centimeter is:

$$Q^* = \tau.(J_{n(K)} - J_{n(A)}) = \tau.(J_{p(A)} - J_{p(K)})$$

where τ is the unique recombination rate for electrons and holes, blended by the carrier lifetime.

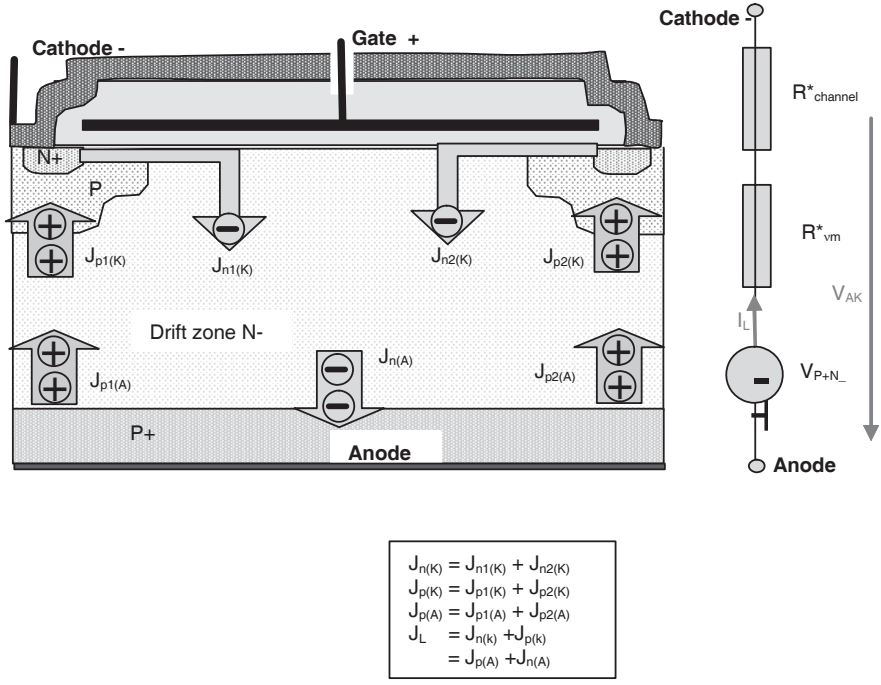


Figure 2.6. *Charges moving in the on-state IGBT and the equivalent circuit*

The IGBT voltage drop, V_{AK}, is composed of the channel voltage, $V_{channel}$ (close to the $R_{channel}.I_L$), and the modulated drift zone voltage, $V_m \approx R_{vm}.I_L$, by the hole injector voltage V_{P+N-} (see Figure 2.6). Channel voltage is the same as for a MOS:

$$R_{channel} \approx \left[\frac{Z}{L} \mu_{ns} \frac{\varepsilon_{ox}}{d_{ox}} (V_{GS} - V_{th}) \right]^{-1}$$

Calculation of V_m and V_{P+N-} is more difficult and requires not only the stored charge quantity, but also the charge profile in the drift zone. Numerical expressions are requested. Figure 2.7 shows two possible profiles versus gain, $\beta_{PNP} = J_P(W_v)/J_n(W_v)$. For $\beta_{PNP} > 1/b$ (where b is the ratio between electron mobility and hole mobility; $b \approx 3$), we can admit, neglecting the carrier concentration, $p(W_v)$, that the carrier distribution is triangular, according to Figure 2.7c. In this case, the stored charge density and the drift zone resistance per square centimeter of silicon may be estimated by the equation:

$$R^*_{vm} = \frac{1}{q(1+b)\mu_n}\int_0^{W_v}\frac{1}{N_D + p(x)}dx = \frac{W_v^{\,2}}{2(1+b)\mu_n Q^*}\cdot\ln\left(1+\frac{2Q^*}{qN_D W_v}\right)$$

where γ_p and γ_n are the injection coefficients for holes and electrons, defined by the two following expressions:

$$\gamma_p = \frac{J_p(0)}{J_A} \qquad \text{and} \qquad \gamma_n = \frac{J_n(W_v)}{J_A} = \frac{J_{Channel}}{J_A}$$

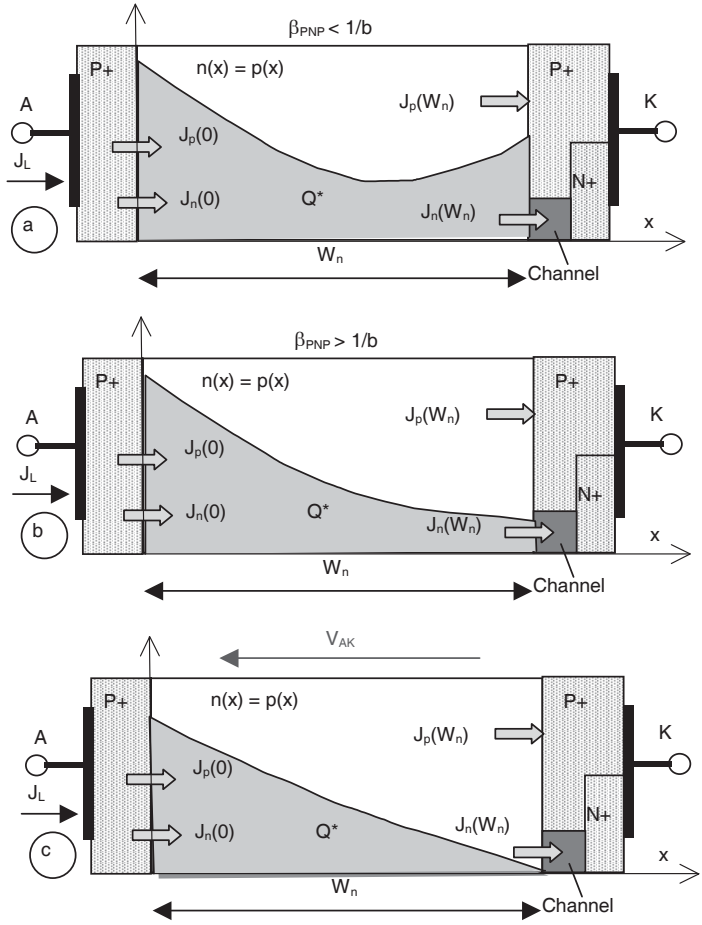


Figure 2.7. *Charge distribution in the drift zone*

Figure 2.8 shows an example of drift zone resistance modulation, R^*_{vm}, by the stored charges Q*. The following numerical values were used: $N_D = 10^{14}$ cm^{-3}, μ_n = 1,000 cm^2 V^{-1}s^{-1}, W_v = 100 μm. We can clearly see that the resistivity is divided by a factor greater than 100, for a stored charge density of 1 μC.cm^{-2}. Now, we can also see that the stored charge must be controlled, because, over a defined level of charge the modulation effect is reduced even with a large quantity of charges. The internal hole injector voltage V_{P+N-} may be estimated using the following equation:

$$V_{P^+N^-} = U_T \ln(1 + \frac{p(0)N_D}{n_i^2}) = U_T \ln(1 + \frac{2Q^* N_D}{qW_v n_i^2})$$

This value is set from 0.5 V to around 1 V.

Three methods exist for the control of stored charges: by recombination rate τ, by holes injection coefficient γ_P, and by electron injection coefficient γ_n. The recombination rate control is achieved by injecting a heavy metal (gold or platinum) into the N- drift zone, or by electron irradiation. The goal of these techniques is to provide some recombination centers for trapped charges.

The electron injection coefficient of electron injector, γ_n, set at a high level in order to avoid any parasitic thyristor switch-on, and in order to control the channel voltage drop. Recombination is improved by controlling the hole injector γ_P on the anode. Two methods are in competition: “punch through” and “non-punch through” technologies (see Figure 2.9).

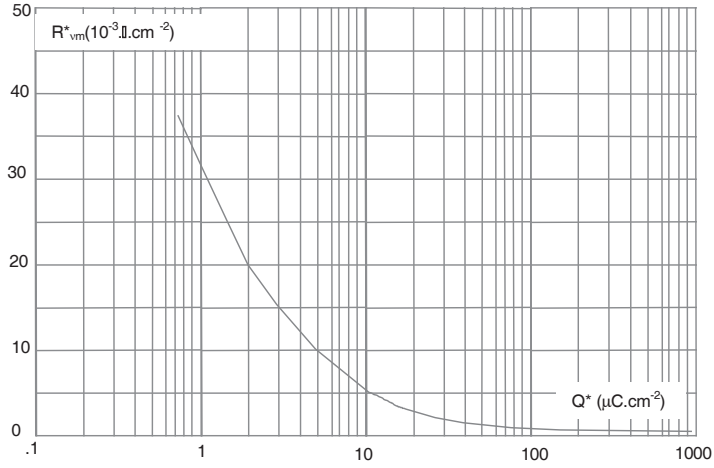
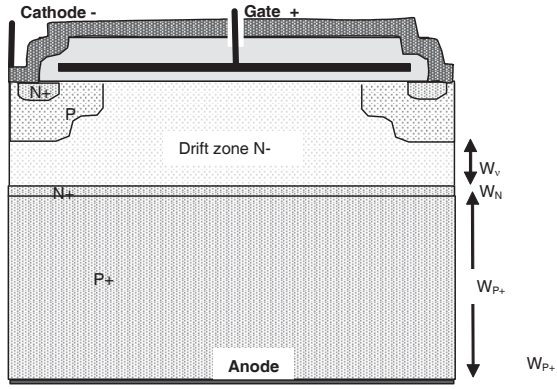


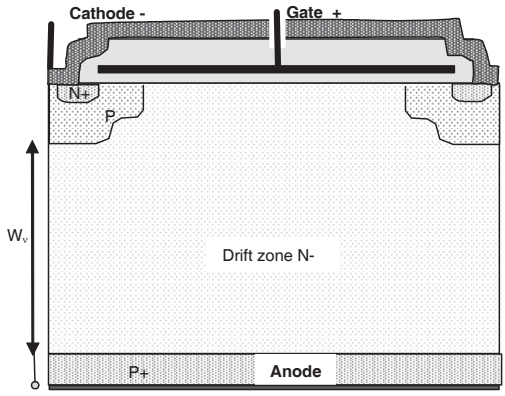
Figure 2.8. *R_{vm} modulation resistance by charge injection: example*

Punch through (PT) technology is directly designed from the power MOSFET technology, where the N+ substrate is replaced by a P+ substrate, with a thickness of approximately 300 µm. The N- drift zone is created by an epitaxy technology. A N+ buried layer, W_N, with a thickness of a few microns, is grown by epitaxy between the P+N- junctions, to insure the control of the injection coefficient, γ_P.

Without a buried layer, the N- drift zone must be thick enough in order to prevent the electric field from rising to the P+ anode layer, under maximum voltage. This buried layer allows the electric field to be inside a thinner N- drift zone, W_v. This buried layer gives the PT-IGBT an asymmetric voltage.



Buried layer technology (Punch Through)



Homogenous layer technology (Non-Punch Through)

Figure 2.9. *Two IGBT technologies*

Figure 2.10 shows the electric field inside the drift zone under the maximum voltage of the device, both with and without the buried layer.

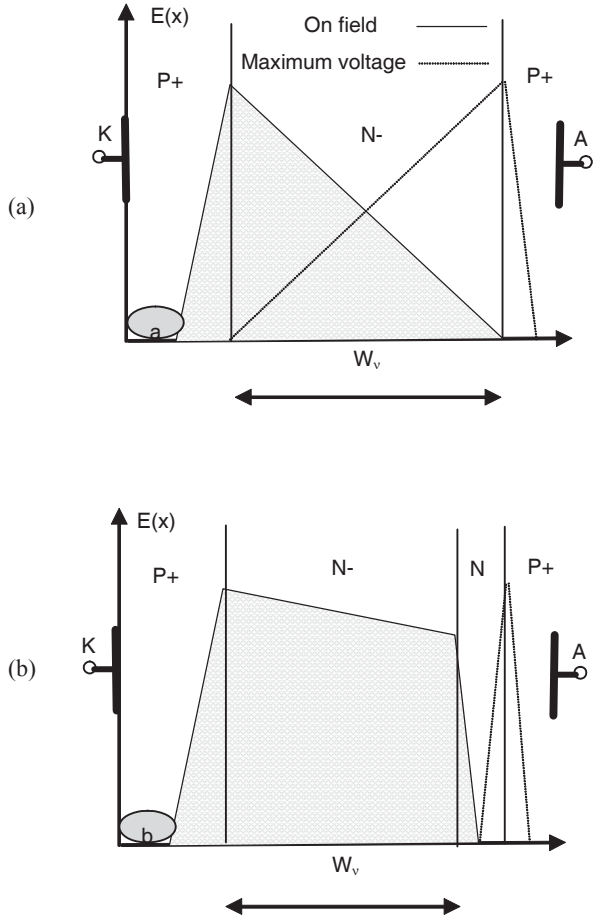


Figure 2.10. *Electric field in the drift zone*
a) without buried layer; b) with buried layer

The W_N thickness and the doping level N of the buried layer are the two parameters for the control of the injection coefficient, γ_P. This is lower when the layer is thicker, and its doping level higher.

Its value is given by the following approximate equation:

$$\gamma_p = \frac{qD_{pN}}{J_A L_{pN} \sinh \frac{W_N}{L_{pN}}} \cdot \left(\frac{p_{N^-}{}^2}{N} \cdot \cosh \frac{W_N}{L_{pN}} - p_N \right)$$

where L_{PN} and D_{PN} represent respectively the length and the hole diffusion constant in the buried layer, P_N represents the hole concentration in the buried layer (assuming the design has a weak doping level) to the P+ anode contact, and P_{N-} represents the hole (or electron) concentration in the drift zone (assuming the design has a high doping level) to the buried layer contact (see Figure 2.11a).

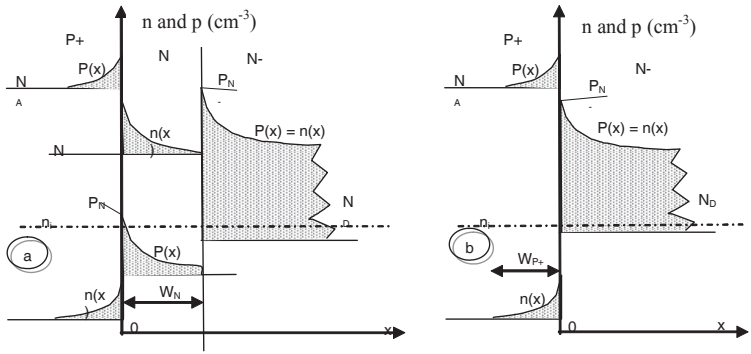


Figure 2.11. *Hole injection control:*
a) by buried layer W_N; b) by W_{p+} thickness

In the NPT-IGBT, the N- drift zone is installed in the overall wafer width, in order to keep a sufficient stiffness: this is at least around 200 µm. This thickness can sustain around 2,000 V. So, a medium voltage IGBT, approximately 1,200 V, is penalized for its forward voltage drop. "Thin wafer" manufacture will be a solution. The P+ anode is made with a boron diffusion or an implantation with small thickness (less than 1 µm). Stored charge is controled by the injection coefficient γ_p, set by the P+ anode thickness. The recombination coefficient is kept high in order to have a modulation in the whole part of the N- zone. γ_p is given by the following equation:

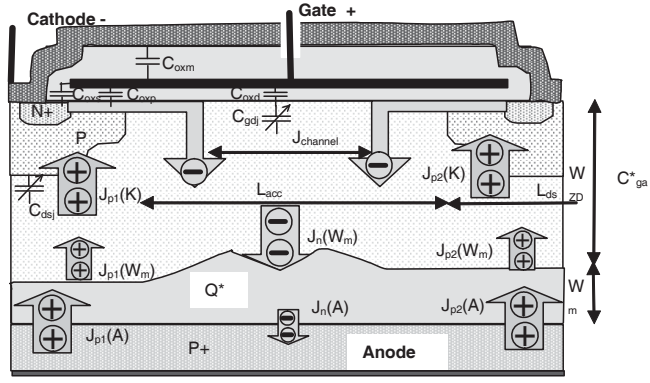
$$\gamma_p = 1 - \frac{qD_{nP^+}}{W_{P^+}} \cdot \frac{p_{N^-}{}^2}{N_A} \cdot \frac{1}{J_A}$$

where D_{nP+}, N_A, P_{N-} represent respectively, the electron diffusion constant in the P+ anode, the doping level of the anode and the charge concentration in the drift zone to anode contact (see Figure 2.11b).

2.3.3. *Dynamic operation*

The dynamic operation of IGBT is much more complex than in MOSFET operation, because the IGBT mechanism is a mix of capacitive operation, like MOSFET and bipolar operation. Also, the N- drift zone cannot be split into several regions of different natures. For example, a highly modulated region and space charge, a lowly modulated region and a space charge region, a highly modulated region and a space charge, with a neutral region between. All these combinations depend on the switching conditions even during the same switching evolution.

(a)



(b)

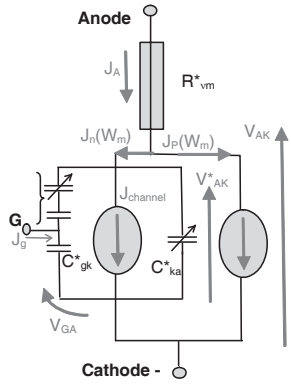


Figure 2.12. *IGBT dynamic operation: a) internal elements; b) equivalent circuit*

Figure 2.12a shows, for example, the IGBT internal state with a high level modulated region, W_m, and a space charge, W_{ZD}. It represents the IGBT internal state during hard switching, with an inductive load. Figure 2.12b shows the equivalent circuit for the same state, with similar elements as in a power MOSFET. Under switching conditions, the voltage drop inside the modulated region is low, so the IGBT voltage drop is equal to this space charge voltage:

$$V_{AK}(t) = V^*_{AK}(t).$$

In this case, with the equivalent circuit, the following equations may be written as an IGBT model for a hard switching operation:

$$(C^*_{AK} + C^*_{GA})\frac{dV_{AK}}{dt} - C^*_{GA}\frac{dV_{GK}}{dt} = \frac{1}{1+\beta_{PNPm}}J_A - J_{Channel}$$

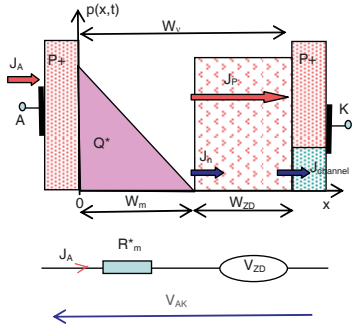
$$(C^*_{GK} + C^*_{GA})\frac{dV_{GK}}{dt} = C^*_{GA}\frac{dV_{AK}}{dt} + J_g$$

$$\frac{dQ(t)^*}{dt} = -\frac{Q(t)^*}{\tau} + J_{p(A)} - J_{p(W_m)} = -\frac{Q(t)^*}{\tau} + (\gamma_p - \frac{\beta_{PNPm}}{1+\beta_{PNPm}}) \cdot J_A$$

$$W_m = W_v - \sqrt{\frac{2\varepsilon_{Si}V_{AK}}{qN_D}}$$

where β_{PNPm} is the PNP dynamic gain, with a real base $W_m(t)$, which changes during switching operation.

Using these equations, we can see that the current or voltage speeds can be driven by the channel current, and thus by the gate drive. With the hypothesis of a linear distribution of charges in the modulated region, Table 2.1 shows a mono-dimensional analytically simplified model of the drift zone for the following three cases: a high modulated region and a space charge region, a high modulated region and a neutral region, a high modulated region and a neutral region and a space charge region. These represent the approximate states of the drift zone in the power electronics applications.



$$V_{drift}(t) = V_{ZD}(t) \text{ and } J_A(t) = J_{channel}(t) + J_P(W_m,t)$$

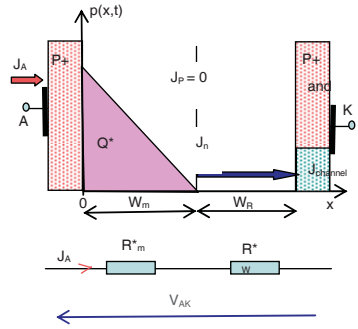
$$J_n(W_m,t) = \frac{b}{1+b} J_A(t) - qD\frac{p(0,t)}{W_m(t)} - J_{dep}(W_m,t)$$

$$J_P(W_m,t) = \frac{b}{1+b} J_A(t) + qD\frac{p(0,t)}{W_m(t)} + J_{dep}(W_m,t)$$

$$J_{dep}(W_m,t) = \frac{Q^*(t)}{3W_m(t)qN_D}.C^*_{ZD}\frac{dV_{ZD}(t)}{dt}$$

$$J_{channel}(t) = J_n(W_m,t).C^*_{ZD}\frac{dV_{ZD}(t)}{dt}$$

$$C^*_{ZD} = \sqrt{\frac{q\varepsilon_{si}N_D}{2V_{ZD}(t)}} \quad \text{and} \quad Q^*(t) = \frac{1}{2}qW_m(t)p(0,t)$$



$$V_{drift}(t) \approx [R^*_m(t) + R^*_W(t)]J_A(t)$$

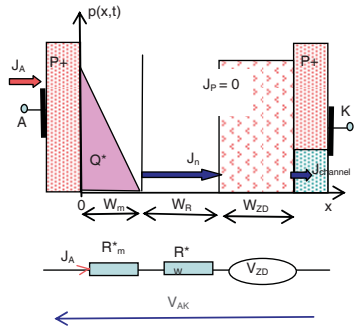
$$J_A(t) = J_{channel}(t)$$

$$R^*_W(t) = \frac{1}{q\mu_n N_D}.W_R$$

$$R^*_m(t) = \frac{1}{q\mu_n(1+b)}.\int_0^{W_m}\frac{1}{N_D + p(x,t)}dx$$

$$p(x,t) = p(0,t)\left[1 - \frac{x}{W_m(t)}\right]$$

$$Q^*(t) = \frac{1}{2}qW_m(t)p(0,t) \text{ and } \frac{dQ^*(t)}{dt} = -\frac{Q^*(t)}{\tau} + J_A(t)$$



$$V_{drift}(t) \approx [R^*_m(t) + R^*_W(t)]J_A(t) + V_{ZD}(t)$$

$$J_A(t) = J_{channel}(t) + C^*_{ZD}\frac{dV_{ZD}(t)}{dt}$$

$$R^*_W(t) = \frac{1}{q\mu_n N_D}.W_R$$

$$R^*_m(t) = \frac{1}{q\mu_n(1+b)}.\int_0^{W_m}\frac{1}{N_D + p(x,t)}dx$$

$$p(x,t) = p(0,t)\left[1 - \frac{x}{W_m(t)}\right]$$

$$Q^*(t) = \frac{1}{2}qW_m(t)p(0,t) \quad \text{and} \quad \frac{dQ^*(t)}{dt} = -\frac{Q^*(t)}{\tau} + J_A(t)$$

Table 2.1. *Simplified models of drift zone, in dynamic operation of an IGBT*

2.4. Main IGBT characteristics

The externally measurable relations between the three main parameters in static and quasi-static operations, V_{AK}, I_A, and V_{GK}, are given by the output and transfer characteristics. Figures 2.13a and 2.13b show characteristics of a 1,000 V, 50 A IGBT. As for a power MOSFET output, characteristics show two zones of operation, a saturated zone and a linear zone, separated by a curve which represents the maximum current the IGBT can sustain without any de-saturation (or without channel pinch off). This maximum current is approximately given by the following equation:

$$I_{A\max} = (1+\frac{1}{b})\left[\frac{K_p}{2}(V_{GK}-V_{th})^2 + \frac{2DQ}{W_v{}^2}\right]$$

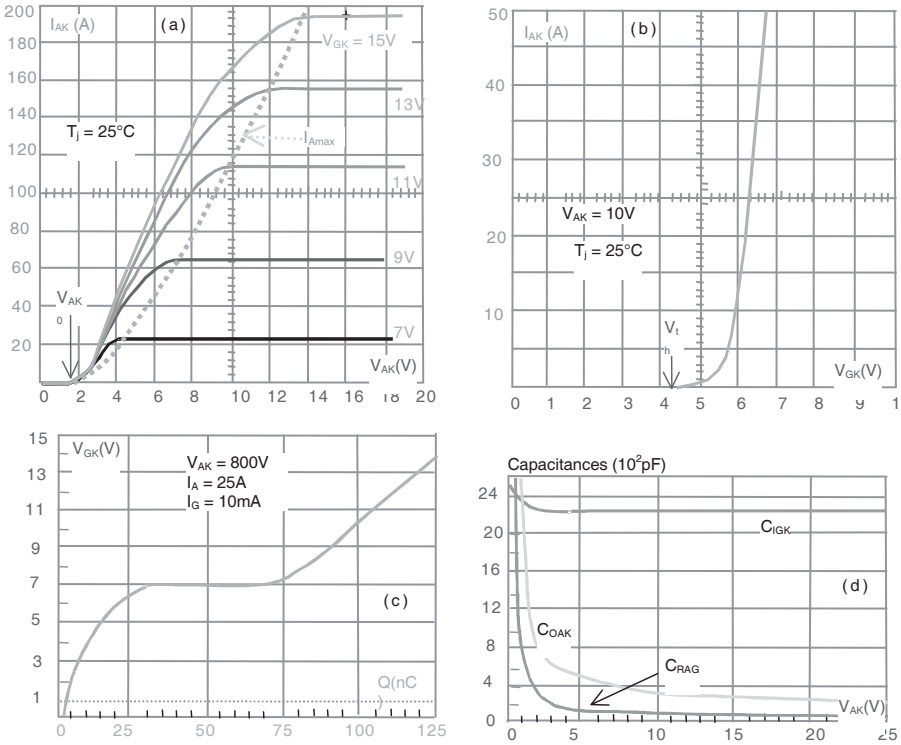


Figure 2.13. *1,000 V, 50 A NPT-IGBT characteristics*

In contrast to the MOSFET I_{Dmax}, the hole current contribution is tied with the bipolar effect. This IGBT output characteristic shows that the voltage drop V_{AK} (around 1V; V_{AK} is the voltage with a quasi-zero current) is larger than that of the MOSFET (around 0V), and larger than that of the bipolar transistor (around 0.2 V), for a 1,000 V device. Voltage drop for this device is around 4 V with a 50 A nominal current, at 25°C. Threshold voltage is V_{th} = 4.5 V, according to the transfer characteristic. Figure 2.13 shows the capacitance characteristics C_{iks}, C_{oks}, C_{rks}, (C_{ga} = C_{rks}, C_{gk} = C_{iks} – C_{rks}, and C_{ak} = C_{oks} – C_{rks}) versus V_{AK} and gate charge. These characteristics are very similar to MOSFET characteristics.

2.5. One cycle of hard switching on the inductive load

Figure 2.14 shows the power circuit and the IGBT simplified model. Parasitic inductive effects in the gate drive and in the power load loop are avoided. Figure 2.15 dipicts the switching waveforms. Compared with the MOSFET current forms, a large difference appears in the anode switch-off current form: instead of quickly going to zero when the anode voltage raises the power supply voltage E, the anode current shows two phases during its fall time: the first is very fast, similar to the MOSFET fall time, and the second is very slow, called the "queue current" or "tail current". Due to the large voltage applied to the IGBT connections at this time, losses due to the "tail" are significant.

The inductive cycle will now be examined phase by phase.

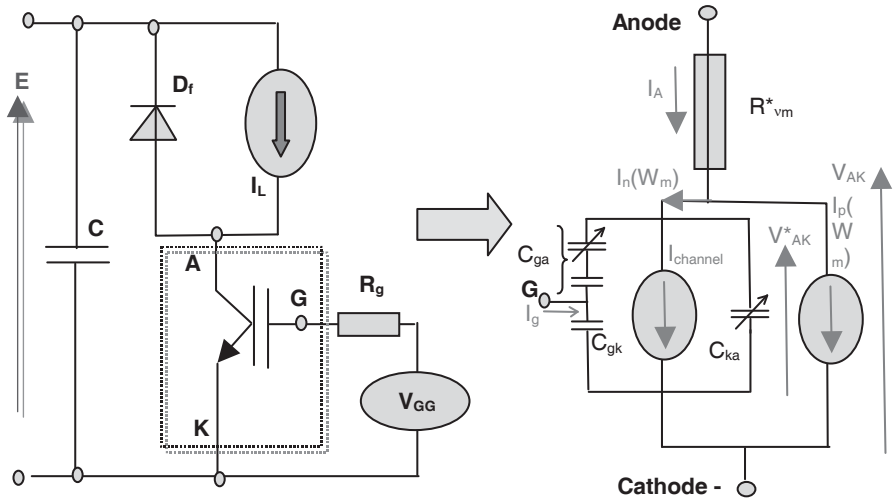


Figure 2.14. *Power circuit and IGBT equivalent circuit during hard switching*

2.5.1. *Switch-on study*

2.5.1.1. *Switch-on delay time $t_{d(on)}$*

Drive voltage rises instantaneously from $-V_{GG}$ to $+V_{GG}$. Gate charge is created according the following equation:

$$V_{GK}(t) = V_{GG}\left[1-2e^{-\frac{t}{R_g(C_{gk}+C_{ga})}}\right] \approx V_{GG}\left[1-2e^{-\frac{t}{R_gCgk}}\right] < V_{th}$$

This operation is the same in a power MOS: anode current is zero because V_{th} was not yet risen, and the anode voltage is the supply voltage, E.

2.5.1.2. *Current rise time $t_{r(on)}$*

$I_A(t)$ starts when $V_{GK} \geq V_{TH}$, and it increases while the gate is loading. During this phase, the drift zone changes. At the beginning, stored charge quantity is low and the drift zone is divided into three parts, according to Figure 2.16. The first is W_{ZD}, close to the cathode in order to sustain the E voltage. Second is a low level modulated region (W_m), close to the anode. Between these two is an ohmic region, W_R. With the current rise time $I_A(t)$, the stored charge quantity, Q(t), increases, and therefore the low level modulated region becomes a high level region. Also, it expands, and the ohmic region disappears. This phenomenon is complex and will be ignored here. We suppose that, from the starting phase, the drift region is divided into a high-level modulated part, and a space charge part. Space charge distribution is also assumed to be linear. Thus, the increase of anode current is given by the following expression:

$$I_A(t) = (1+\frac{1}{b})\left[\frac{K_p}{2}(V_{GK}(t)-V_{th})^2 + \frac{2DQ(t)}{W_m(t)^2}\right]$$

where the charge accumulation, neglecting recombination, is given by:

$$\frac{dQ(t)}{dt} = I_{Channel}(t) - [1-\gamma_p(t)]I_A(t)$$

and I_{AK} increases up to the external limit: $I_L + I_{RM}$.

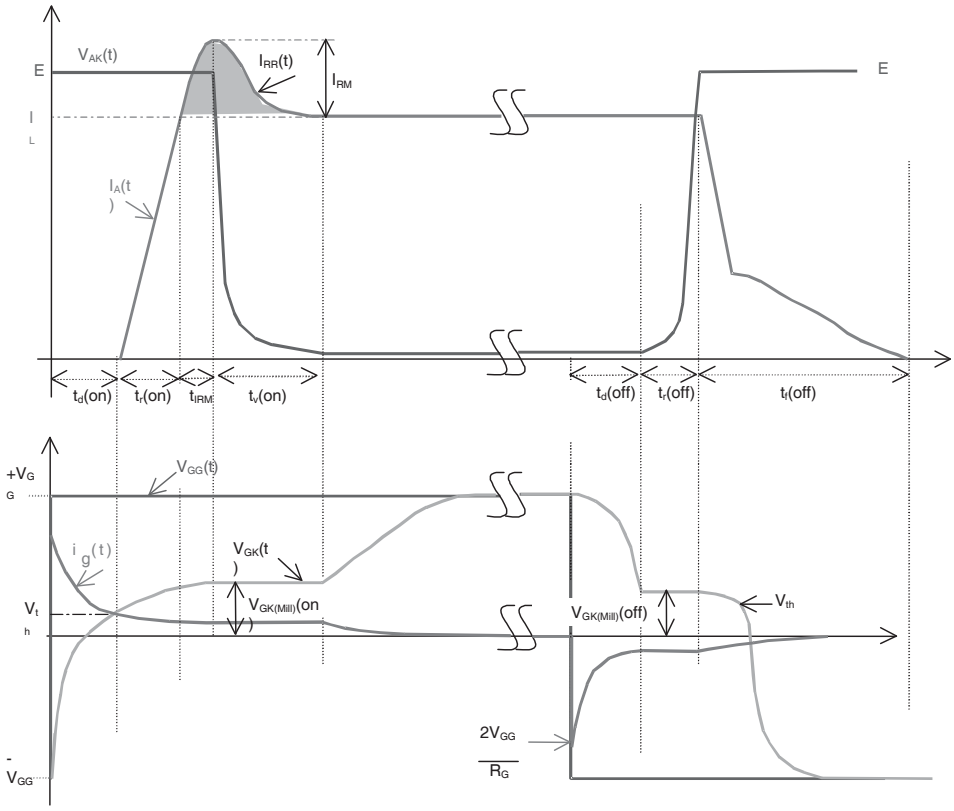


Figure 2.15. *Switching waveforms with inductive load*

2.5.1.3. *Fall time voltage $t_{v(on)}$*

When $I_{AK}(t) = I_L + I_{RM}$, V_{AK} could fall, however, C_{GK} discharges, tied to $dV_{AK}(t)/dt$, and V_{AK} is quasi-constant and is equal to Miller voltage $V_{AK(Miller)on}$. Miller voltage is given by the following expression:

$$I_L + I_{RM} = (1+\frac{1}{b})\left[\frac{K_p}{2}(V_{GK(Miller)on} - V_{th})^2 + \frac{2DQ}{W_m^{\ 2}}\right]$$

$V_{AK}(t)$ fall time is defined, neglecting the voltage drop in the modulated region, however, the displacing current, tied to the quick change of the boundary between modulated and space charge regions, is taken into account:

$$\frac{dV_{AK}(t)}{dt} = \frac{I_L + I_{RR} - (1+\frac{1}{b})\left[\frac{K_p}{2}(V_{GK} - V_{th})^2 + \frac{2QD}{W_m^{\,2}}\right] + (1+\frac{1}{b})\frac{C_{ga}}{C_{ga}+C_{gk}} i_g}{(1+\frac{1}{b})\left[C_{ak} + \frac{C_{gk}C_{ga}}{C_{ga}+C_{gk}} + \frac{C_{ZD}}{3}\cdot\frac{Q}{Q_{Bm}}\right]}$$

$$C_{ZD} = S_{Si}\sqrt{\frac{q\varepsilon_{Si}N_D}{2V_{AK}}} \qquad \text{and} \qquad Q_{Bm} = qN_D W_m S_{Si}$$

As with MOSFETs, we can see a fast fall time at the beginning, and slower fall time as $V_{AK}(t)$ decreases. Stored charges increase according to the equation:

$$\frac{dQ(t)}{dt} = I_{Channel}(t) - (1-\gamma_p)\cdot\left[I_L + I_{RR}\right]$$

However, the increase is negligible while time $t_{v(on)}$ is generally very short. Current $I_{AK}(t)$ during this entire phase is defined by the external current $I_A = I_L + I_{RM}$. When $dV_{AK}/dt = 0$, $V_{GK}(t)$ increases up to V_{GG}, according to the following expression:

$$V_{GK}(t) = V_{GG}\left[2e^{-\frac{t}{R_g(C_{gk}+C_{ga})}} - 1\right] > V_{GK(Miller)on}$$

2.5.2. *Switch-off study*

2.5.2.1. *Switch-off delay time $t_{d(off)}$*

The gate drive voltage decreases instantaneously from $+V_{GG}$ down to $-V_{GG}$. Gate voltage discharge is given by:

$$V_{GK}(t) = V_{GG}\left[2e^{-\frac{t}{R_g(C_{gk}+C_{ga})}} - 1\right] > V_{GK(Miller)off} > V_{th}$$

IGBT voltage slightly increases until gate voltage V_{GK} is higher than switch-off Miller voltage $V_{GK(Miller)off}$ according to:

$$I_L = (1+\frac{1}{b})\left[\frac{K_p}{2}(V_{GK(Miller)off} - V_{th})^2 + \frac{2DQ}{W_\nu^{\,2}}\right]$$

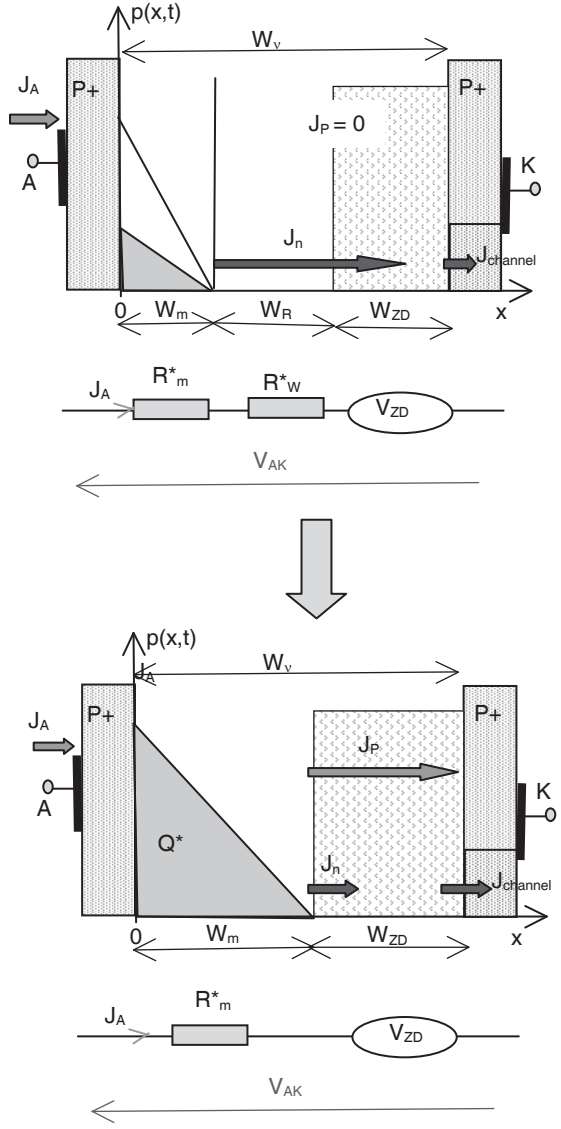


Figure 2.16. *Drift zone evolution during the anode current rising time*

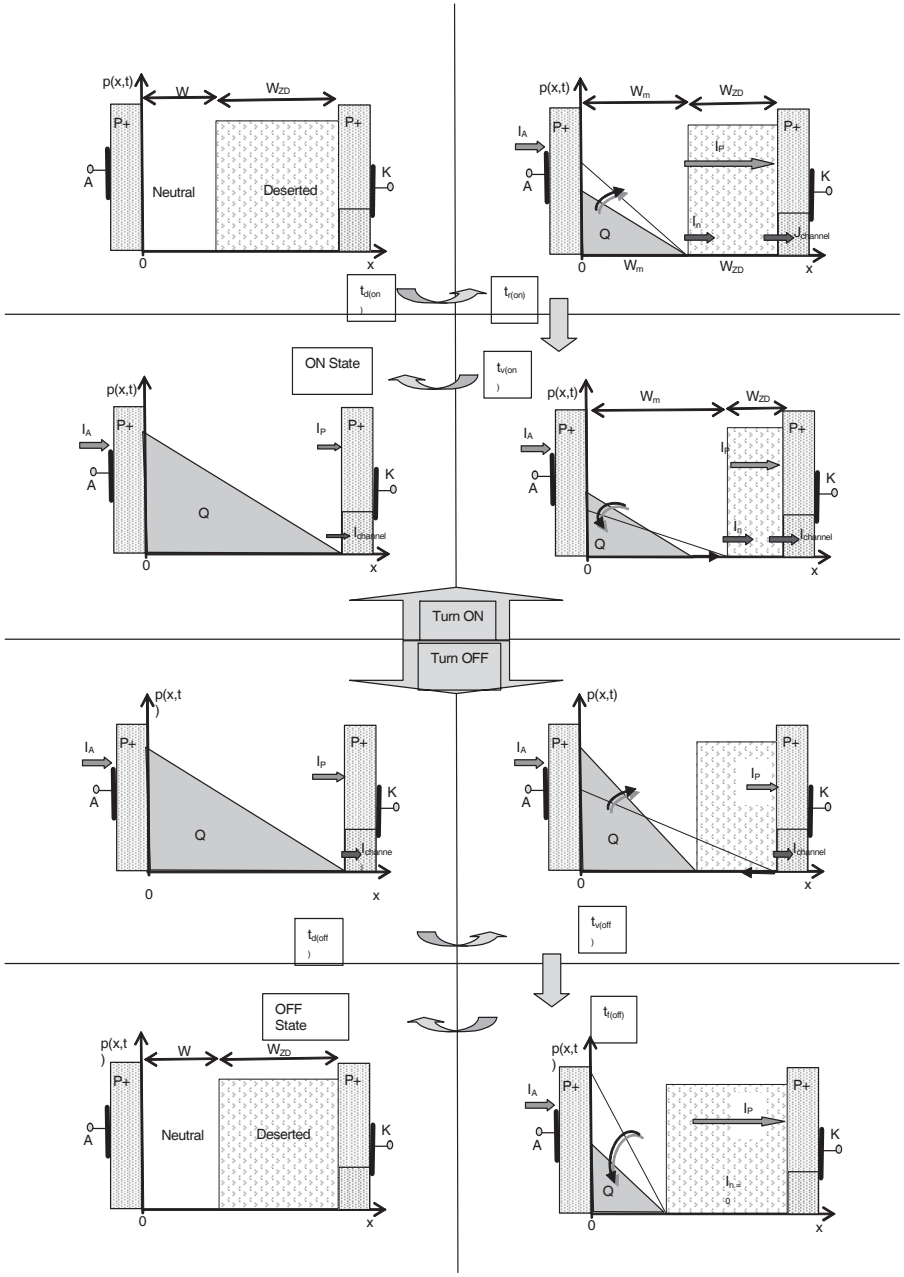


Figure 2.17. *Charge evolution in the drift zone during one switching cycle on an inductive load*

I_{AK} is still forced to equalize the load current, I_L, and the voltage V_{AK} is under the same law that applied in the on-phase. Channel current (electrons) decreases because the gate voltage decreases, and the process of charge storage slows down. Stored charge also decreases if the delay is large (high R_G). The quantity of charge is determined by the following equation:

$$\frac{dQ(t)}{dt} = -\frac{Q}{\tau} + I_{Channel}(t) - (1-\gamma_p)I_L$$

2.5.2.2. *Voltage rise time $t_{v(off)}$*

When the gate voltage V_{GK} is equal to the Miller voltage $V_{GK(Miller)off}$, V_{AK} starts to rise. The gate voltage is constant and equal to $V_{GK(Miller)off}$, because capacitance C_{GA} is charged by the current allowed by $dV_{AK}(t)/dt$. Speed is given by:

$$\frac{dV_{AK}(t)}{dt} = \frac{I_L - (1+\frac{1}{b})\left[\frac{K_p}{2}(V_{GK}-V_{th})^2 + \frac{2QD}{W_m{}^2}\right] + (1+\frac{1}{b})\frac{C_{ga}}{C_{ga}+C_{gk}}i_g}{(1+\frac{1}{b})\left[C_{ak} + \frac{C_{ge}C_{gc}}{C_{ga}+C_{gk}} + \frac{C_{ZD}}{3}\cdot\frac{Q}{Q_{Bm}}\right]}$$

As with MOSFETs, and for the same reasons, voltage rise starts slowly then increases speed. Current I_{AK} is still equal to I_L during this phase, and the charge quantity follows the aforementioned law. $t_{v(off)}$ is generally short and the stored charge variation can be neglected.

2.5.2.3. *Current fall time $t_{f(off)}$*

When V_{AK} raises the supply voltage, E, Miller effect disappears with $dV_{AK}(t)$ / = 0. Gate voltage can now decrease according to the equation:

$$V_{GK}(t) = V_{GG}\left[2e^{-\frac{t}{R_g(C_{ga}+C_{ga})}} - 1\right] \approx V_{GG}\left[2e^{-\frac{t}{R_g C_{gk}}} - 1\right] > V_{th}$$

Anode current can also decrease: fast decrease also occurs with power MOSFET and follows the gate voltage discharge, then a "tail" starts when the channel is opened ($V_{AK}(t)<V_{th}$). As the tail is slow, we can admit that: $t_{f(off)} = t_{tail}$. The tail value

and its duration depends on the stored charge and the recombination rate. It may be estimated as:

$$I_A(t) = I_{tail}(t) = (1+\frac{1}{b})\frac{2DQ(t)}{W_m{}^2} \qquad \text{with} \qquad W_m = W_v - \sqrt{\frac{2\varepsilon_{Si}E}{qN_D}}$$

Charges mainly disappear by recombination, but electron injection into the P+ anode (reverse injection) speeds up the process. Thus:

$$\frac{dQ(t)}{dt} = -\frac{Q(t)}{\tau} - (1-\gamma_p)I_A(t)$$

According to this equation, the reverse injection of electrons in the P+ anode is equivalent to a stored charge extraction, and its effect is stronger when the P+N- injection coefficient is smaller. This phase ends when stored charges in the drift zone are close to zero.

If the stored charge is assumed to be linear, Figure 2.17 shows qualitatively the charge evolution in the drift zone, on inductive load, during the entire switching cycle.

Table 2.2 lists the various external parameters variations.

From the previous analysis, we can see that a high speed of the gate drive allows a decrease of switching times and an increase of $dI_A(t)/dt$ and $dV_{AK}(t)/dt$, during switch-on and switch-off. Accordingly, its allows for a reduction of losses.

SWITCH-ON					
$t_{d(on)}$	$V_{ak}(t) = E$	$I_A(t) = 0$	$V_{GK}(t) = V_{GG}\left[1-2e^{-\frac{t}{R_g(C_{gk}+C_{ga})}}\right] \approx V_{GG}\left[1-2e^{-\frac{t}{R_gC_{gk}}}\right] < V_{th}$		$Q(t) = 0$
$t_{r(on)}$	$V_{AK}(t) = E$ $I_A(t) = (1+\frac{1}{b})\left[\frac{K_p}{2}(V_{GK}(t)-V_{th})^2 + \frac{2DQ(t)}{W_m(t)^2}\right]$		$V_{GK}(t) = V_{GG}\left[1-2e^{-\frac{t}{R_g(C_{gk}+C_{ga})}}\right]$ $\approx V_{GG}\left[1-2e^{-\frac{t}{R_gC_{gk}}}\right] > V_{th}$		$\frac{dQ(t)}{dt} = I_{Channel}(t)$ $-(1-\gamma_p)I_A(t)$
$t_{V(on)}$	$\frac{dV_{AK}(t)}{dt} = \frac{I_L + I_{RR} - (1+\frac{1}{b})\left[I_{An} - \frac{C_{ga}}{C_{ga}+C_{gk}}i_g\right]}{(1+\frac{1}{b})\left[C_{ak} + \frac{C_{gk}C_{ga}}{C_{ga}+C_{gk}} + \frac{C_{ZD}}{3}\cdot\frac{Q}{Q_{Bm}}\right]}$ $I_L = \frac{K_p}{2}(V_{GK}-V_{th})^2 + \frac{2QD}{W_m{}^2}$		$I_A = I_L + I_{RR}$	$V_{GK}=V_{GK(Miller)on}$	$\frac{dQ(t)}{dt} = I_{Channel}(t)$ $-(1-\gamma_p)(I_L + I_{RR})$
ON-STATE					
	$V_{AK} = V_{P^+N^-} + I_L\cdot(R_{vm} + R_{Channel})$	$I_A = I_L$	$V_{GK} = +V_{GG}$		$Q = (\gamma_p - \frac{\beta_{PNP}}{1+\beta_{PNP}})\cdot I_L\cdot\tau$
SWITCH-OFF					
$t_{V(off)}$	$\frac{dV_{AK}(t)}{dt} = \frac{I_L - (1+\frac{1}{b})\left[I_L - \frac{C_{ga}}{C_{ga}+C_{gk}}i_g\right]}{(1+\frac{1}{b})\left[C_{ak} + \frac{C_{gk}C_{ga}}{C_{ga}+C_{gk}} + \frac{C_{ZD}}{3}\cdot\frac{Q}{Q_{Bm}}\right]}$ $I_L = \frac{K_p}{2}(V_{GK}-V_{th})^2 + \frac{2QD}{W_m{}^2}$		$I_A(t) = I_L$	$V_{GK} = V_{GK(Miller)off}$	$\frac{dQ(t)}{dt} = -\frac{Q}{\tau} + I_{Channel}(t) - (1-\gamma_p)I_L$

$t_{f(off)}$	$V_{AK}(t) = E$	$I_A(t) = (1+\frac{1}{b})\frac{2DQ}{W_m{}^2}$	$V_{GK}(t) = V_{GG}\left[2e^{-\frac{t}{R_g(C_{gk}+C_{gk})}} - 1\right] < V_{th}$	$\frac{dQ(t)}{dt} = -\frac{Q(t)}{\tau} - (1-\gamma_p)I_L(t)$
OFF-STATE				
	$V_{AK}(t) = E$	$I_A(t) = 0$	$V_{GK}(t) = -V_{GG}$	$Q = 0$

Table 2.2. E*volution of external quantities during one switching cycle on an inductive load*

A power load circuit has various effects that differ at switch-on and switch-off. Table 2.3 gives a qualitative evaluation. Figure 2.18 shows application results from a 1,000 V, 50 A PT-IGBT, with the same drive and test temperature. We can see that voltage E only has an effect on stored charge, after the current's initial rising phase.

The duration of the Miller "plateau", at switch-on and switch-off, depends on R_g: it is short when R_g is small. When the drive is fast and current i_g is larger than the charge and discharge currents given by $dV_{AK}(t)/dt$, the Miller effect disappears. In this case, $dV_{AK}(t)/dt$ is the same, but V_{GK} voltage is no longer constant during $t_{v(on)}$ and $t_{v(off)}$, and is given by the equation:

$$(C_{gk} + C_{ga})\frac{dV_{GK}}{dt} = C_{ga}\frac{dV_{AK}}{dt} + i_g$$

$$V_{GG} = R_g i_g + V_{GK}$$

POWER	SWITCH ON			SWITCH OFF		
	$dI_A(t)/dt$	$dV_{AK}(t)/dt$	$V_{GK(Miller)on}$	$I_{tail}(t)$	$dV_{AK}(t)/dt$	$V_{GK(Miller)off}$
E ↗(W_m ↘)	↗	(↗)		↗	(↗)	
I_L ↗	(↗)	↘	↗	(↗)	↗	↗
I_{RR} ↗		↘	↗			

Table 2.3. *Power load effects on IGBT, during hard switching operation*

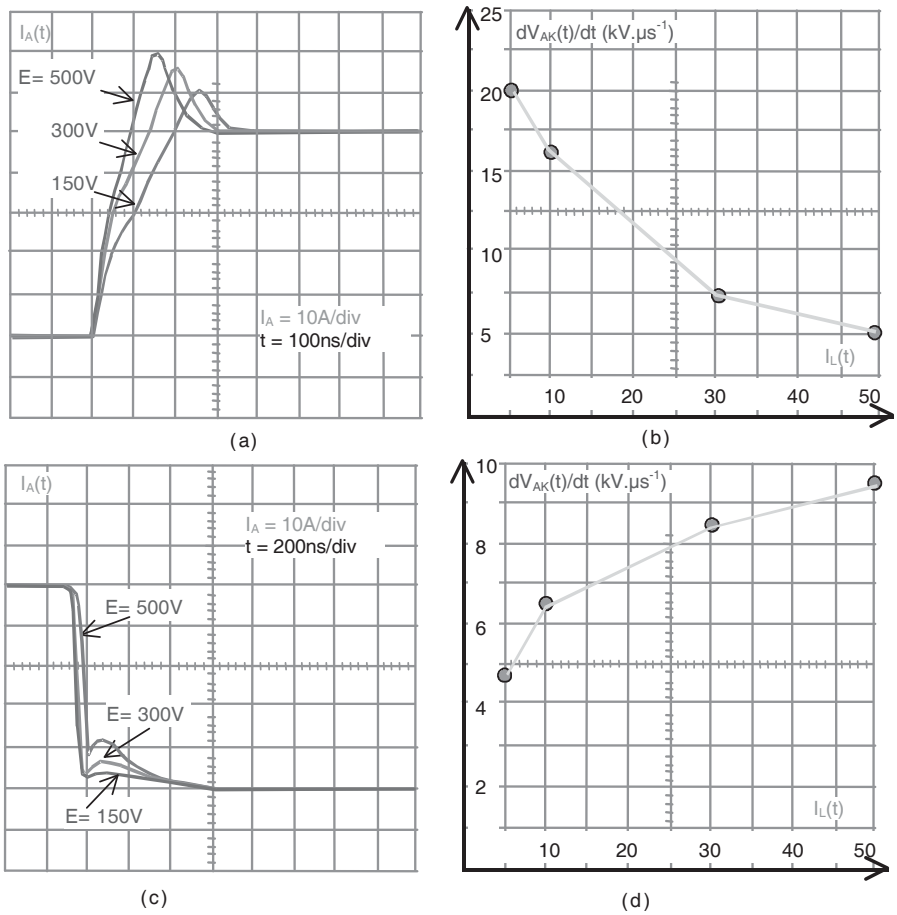


Figure 2.18. *Load effects on IGBT behavior in hard switching: a) and b) switch-on; c) and d) switch-off*

2.6. Soft switching study

2.6.1. *Soft switching switch-on: ZVS (Zero Voltage Switching)*

ZVS operation is performed during an interval at zero current and quasi-zero voltage, before connection of the power load. This interval depends on the application: Figure 2.19 shows the phases of an application, together with the associated waveforms. The ZVS target is to apply I_{load} with a low voltage V_{AKmax} and within a minimum of time $t_v(_{ZV})$, in other words with a minimal dynamic voltage. Two conditions are applied on the gate drive. First, gate voltage $V_{GG}(t)$ must occur at a sufficient time $t_{pre}(on)$ before the current application, in order to obtain a V_{GK} voltage higher than V_{th} before application of the load current. Second, the speed of increase of the gate voltage $V_{GK}(t)$ must be high enough in order to obtain a channel current greater than the applied current: $dI_{channel}(t)/dt > dI_L(t)/dt$. This operation is called "switch-on preconditioning". If this condition is not realized, a desaturation phenomenon appears, and V_{AKmax} could raise the supply voltage. With the correct preconditioning operation, the drift zone may be roughly represented by two sub-regions: one a high modulated level, W_m, and a neutral ohmic one, W_R (see Figure 2.19b). Thus, the anode to cathode voltage is approximately:

$$V_{AK}(t) = V_{P^+N^-}(t) + I_A(t) \cdot [R_m(t) + R_w(t) + R_{Channel}(t)]$$

Neglecting re-combinations, storage charges follow the law:

$$Q(t) = \int_0^t I_A(t)dt$$

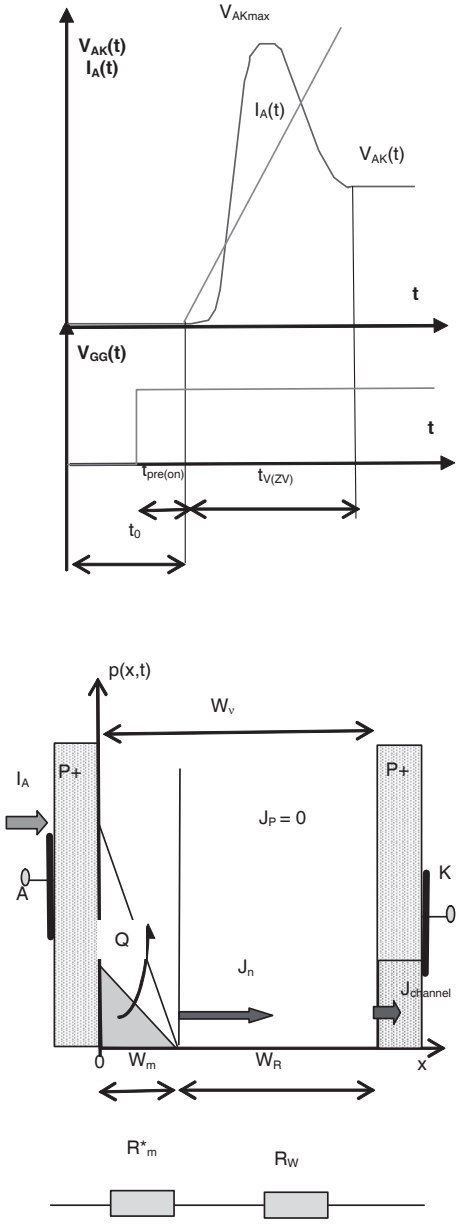


Figure 2.19. *Soft switching (ZVS): a) waveforms; b) charge evolution*

In order to obtain a reliable dynamic voltage, charges must be stored quickly. However, the available stored charge for a given load current is accordingly weak when the current speed is too fast. As a result, $V_{AK}(t)$, the soft switching dynamic voltage in ZVS during time $t_{v(ZV)}$, is highly significant when $dI_L(t)/dt$ is high. This phenomenon is the same as in bipolar diodes during switch-on. Compared to bipolar transistors, the IGBT dynamic voltage is much lower, because the charge storage made by the $I_L(t)$ current is faster than the storage made by the $I_b(t)$ current, except when the base current is higher than the I_L current in amplitude and speed. Figure 2.20 shows experimental results with a PT-IGBT, which confirm the weak IGBT dynamic voltage in ZVS operation.

2.6.2. *Soft switching switch-off: ZCS (Zero Current Switching)*

Here, two switching modes are distinguished: thyristor and thyristor-diode modes. The first mode occurs when an IGBT and anti-paralleled diode are series connected with a diode. The latter is omitted in the thyristor-diode mode. During operation, the thyristor-diode mode is characterized by a reverse current applied on the switch, while in the thyristor mode, this current is stopped by the series connected diode.

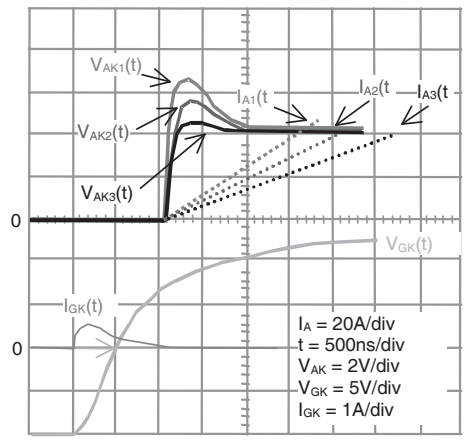


Figure 2.20. *1,000 V, 50 A PT-IGBT with ZVS*

Figure 2.21 shows various switching phases and associated waveforms for a ZCS thyristor mode operation. The IGBT anode current is cancelled by the power load current action at t = 0, and it remains zero while the V_{AK} voltage is quasi-zero, during a time t_c (it is slightly negative due to anti-paralleled diode forward voltage,

V_F). This interval is fully dependent on the power load. At the completion of t_c time, a positive voltage $V_{AK}(t)$ is applied to the switch, and IGBT terminals. At this time, a switch-on current appears, caused by the remaining stored charges in the IGBT. Soft switching in thyristor mode minimizes this current, when the load voltage appears. Switch-off of the gate drive voltage must occur before this load voltage, with a minimum advance $t_{pre(off)min}$, giving enough time to the gate drive to be under the threshold voltage V_{th}. This process is called "switch-off preconditioning drive".

At time t = 0, the conduction stored charges are in the drift zone, even if the anode current becomes zero. During t_c, Q_o is reduced using two methods: recombination, which is the main mechanism, and internal diffusion currents, which may occur only if the channel is still conducting. Thus:

$$\frac{dQ(t)}{dt} = -\frac{Q}{\tau} + qD\frac{dp(x,t)}{dx}\bigg|_{x=W_v}$$

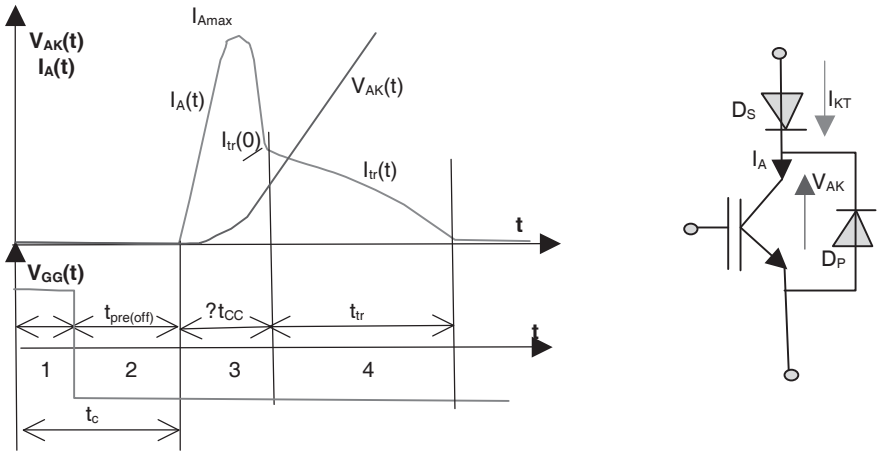


Figure 2.21. *ZCS in thyristor mode*

At t = t_c, $V_{AK}(t)$ is applied, and the channel is opened by the preconditioning, but some stored charge remains in the drift zone. IGBT is not able to sustain the imposed load voltage, so, the charge concentration at x = W_v, $p(W_v)$, is not zero. Therefore, a short circuit appears, through the IGBT and the inductive connections L_{conn}, on the applied voltage $V_{ap}(t)$, until the storage charge cancellation at x =W_v, $p(W_v) = 0$. Short circuit current (peak current) is given by the equation:

$$I_{A\max} = \frac{1}{L_{conn}} \int_{t_c}^{t_c+\Delta t_{sc}} \left[V_{ap}(t) - V_{AK}(t) \right] dt$$

This short circuit phase is longer when the stored charge at $t = t_c$ is greater.

At the end of this phase, IGBT recovers its power to sustain a positive voltage, even if some remaining charges are still in the drift zone. So, a tail can appear, as with hard switching, but the applied voltage is now variable. This tail with variable applied voltage is:

$$I_A(t) = (1 + \frac{1}{b}) \frac{2DQ(t)}{W_m{}^2} \quad , \quad \frac{dQ(t)}{dt} = -\frac{Q(t)}{\tau} - (1 - \gamma_p) I_A(t)$$

$$W_m = W_v - \sqrt{\frac{2\varepsilon_{Si} V_{AK}(t)}{qN_D}}$$

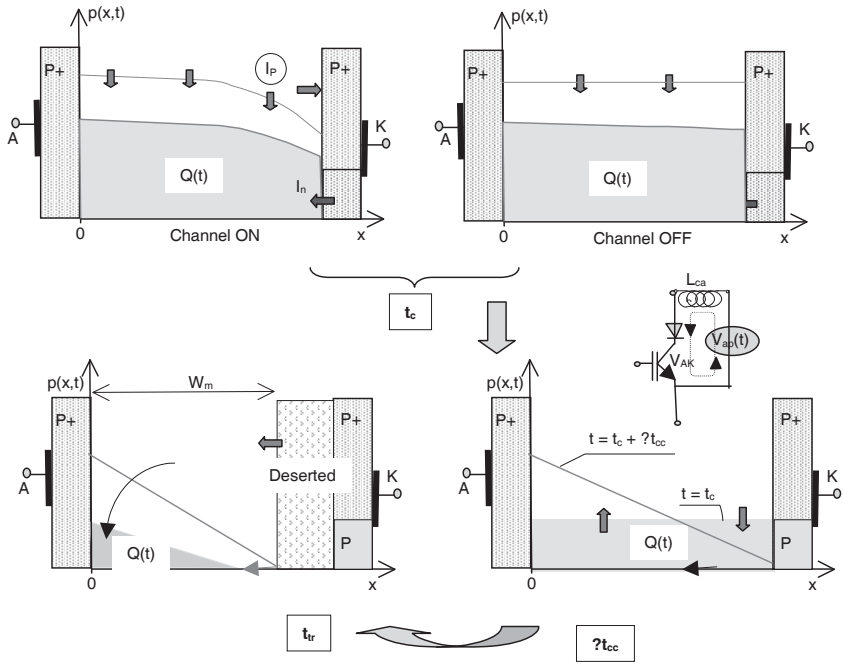


Figure 2.22. *Charge evolution in ZCS thyristor mode*

Figure 2.22 depicts charge evolution during the various ZCS phases, in the thyristor mode. The following is a list of the main switching parameters mentioned in the previous analysis:

– *The recombination time* t_c*:* the stored charge is lower when this time is long. But it is tied to the application constrains, mainly the working frequency.

– *The preconditioning time* $t_{pre(off)}$*:* in order to have diffusion currents, when the external current equals zero, this time must be as small as possible. In other words, the channel must be on for as long as possible.

– *The applied voltage speed* $dV_{AK}(t)/dt$*:* a low speed allows a small turn on current, but it is entirely tied to the application.

Figure 2.23 shows the experimental results supporting these statements. The short circuit makes few losses, even with a high peak current. The tail makes the majority of losses.

Figure 2.24a shows the various switching phases with the corresponding waveforms in the thyristor-diode mode. Some differences occur during the recombination phase t_c, and on the external voltage application, according to the thyristor mode waveforms. During t_c, instead of a zero current in a thyristor-diode mode operation, an inverse current, due to the power load, is applied to the IGBT and the anti-parallel diode. Conversely, the applied voltage shows a steep gradient, followed by a constant voltage, like in hard switching operation.

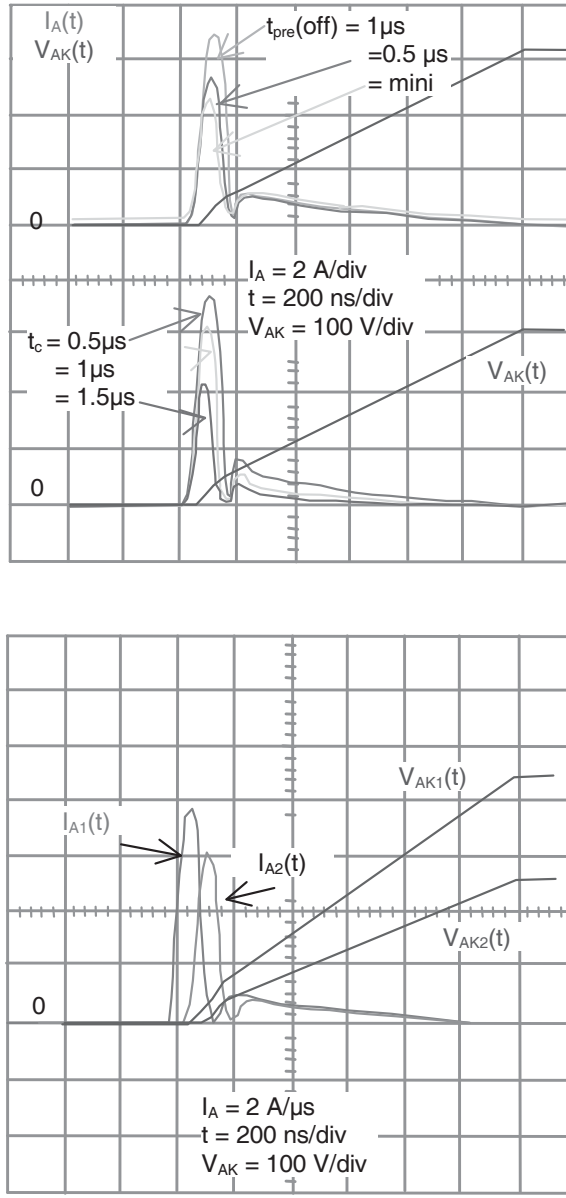


Figure 2.23. *PT-IGBT 1,000 V, 50 A in ZCS thyristor–mode, versus, $t_{pre(off)}$, t_c, $dV_{AK}(t)/dt$*

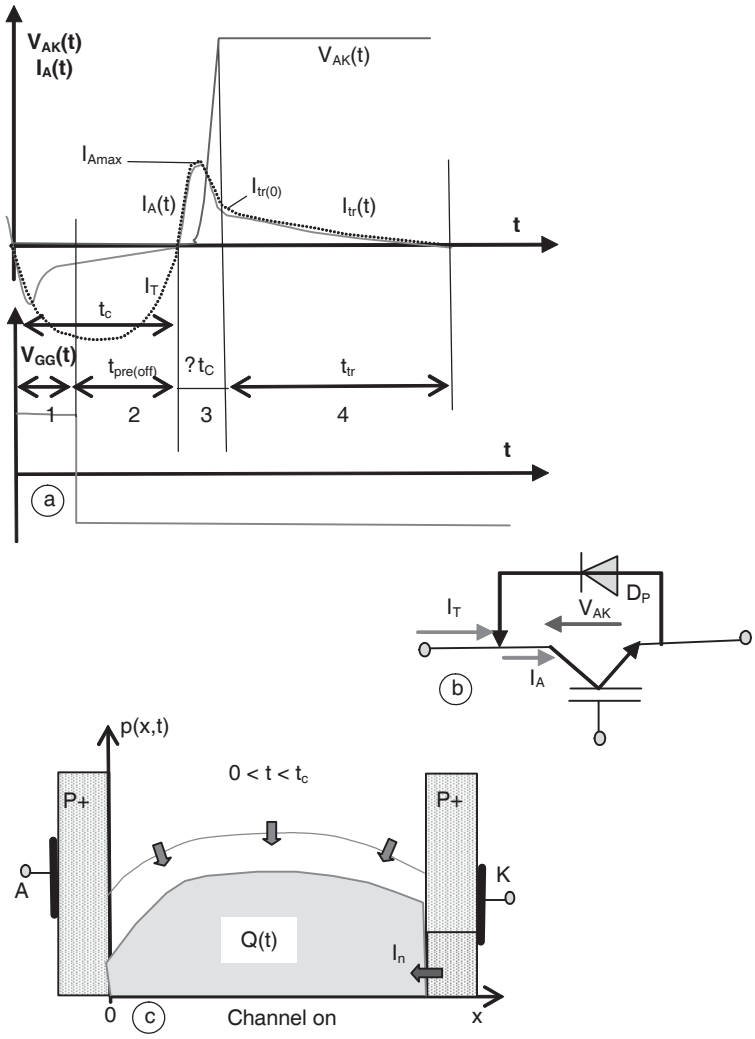


Figure 2.24. *ZCS soft switching in thyristor–mode operation*

The inverse current is split between the anti-parallel diode and the IGBT. Due to the low reverse voltage made by the diode, the IGBT forward voltage is able to take only a very small part of this current. Accordingly, the extraction of stored charge is weak. Nevertheless, it is possible to use this low reverse current to extract a maximum stored charge: during the reverse conduction, the channel may be opened; or in on-state, according to the drive applied. If the channel is opened, the reverse conduction is only made by the PNP bipolar transistor under the effect of the stored

charge effect. Thus, charge extraction is impossible, while the reverse current is comprised solely of hole charges. Now, if the channel is on, electrons create the reverse current from the channel, while the hole current is driven by the anode. Stored charge disappears by recombination, reverse current extraction and internal diffusion current (see Figure 2.24c).

$$\frac{dQ(t)}{dt} = -\frac{Q}{\tau} + qD\frac{dp(x,t)}{dx}\bigg|_{x=W_v} - I_{Treverse}$$

Figure 2.25 shows the extraction effect made by the on-channel in 1,000 V, 25 A NPT-IGBT. As for the thyristor mode operation, it is necessary to reduce the preconditioning time in order to obtain a maximum extraction. The short circuit phase is the same as in the thyristor mode operation, and the tail is equivalent to the one made by the hard switching operation.

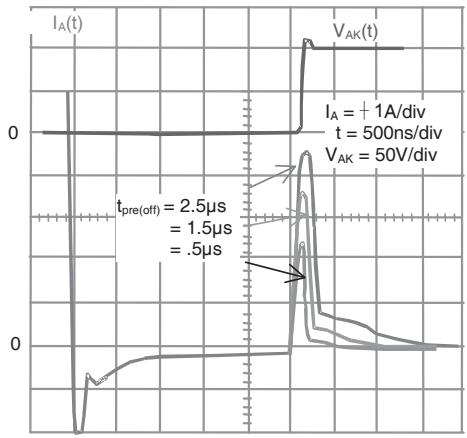


Figure 2.25. *1,000 V, 50 A NPT-IGBT in ZCS-thyristor-diode, versus* $t_{pre(off)}$

2.7. Temperature operation

Neglecting second order effects, the IGBT overall voltage drop is the sum of three parameters: the V_{P+N-} junction potential, the modulated drift zone drop voltage, and the channel voltage drop. Two resistors, R_{vm} and $R_{channel}$, could represent the two last parameters. The V_{P+N-} potential at zero current is the V_{AK0} voltage drop. It increases with the charge concentration p(0); and has a negative temperature coefficient. The channel resistance has a positive temperature coefficient, thanks to

the reduction of electron surface mobility. R_{vm} temperature coefficient depends on μ_n and Q, two terms which have two opposite temperature coefficients. Versus temperature, electron bulk mobility μ_n decreases while quantity of charges Q increases, due to an increase of the carriers lifetime. This last one and the recombination rate varies according to the following law:

$$\tau(T_j) = \tau(T_{j0}) \left[\frac{T_j}{T_{j0}} \right]^{\alpha_\tau}$$

where T is in Kelvin.

The exponential coefficient α_τ is positive and higher when the lifetime is shorter. If the quantity of stored charges Q varies with the same law (this assumption is not really verified because it could be necessary to consider the injection coefficients of injectors with temperature), the μ_n.Q term variation versus temperature is:

$$\mu_n(T_j)Q(T_j) = \mu_n(T_{j0})Q(T_{j0}) \left[\frac{T_j}{T_{j0}} \right]^{(\alpha_\tau - 2,5)}$$

The temperature coefficient of R_{vm} is positive for $\alpha_\tau < 2.5$ and negative for $\alpha_\tau > 2.5$.

In conclusion it would be seen that the global forward voltage versus temperature is quite complex, depending on each factor of the whole voltage, and on their appropriate coefficients versus temperature. Thus depending on the technological production process.

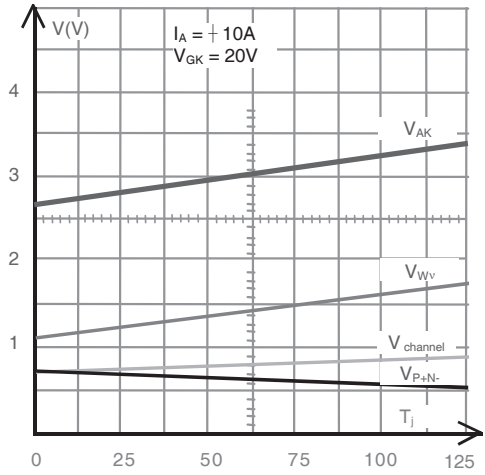


Figure 2.26. *1,000 V, 10 A PT-IGBT: three voltage distributions versus temperature*

Figure 2.26 shows an example of three voltage variations versus temperature.

The NPT-IGBT includes a large drift zone and a long carrier lifetime. If the carrier lifetime is in the region of $\alpha_\tau << 2.5$, the R_{vm} resistance temperature coefficient is positive. This way, two terms have a positive temperature coefficient: R_{vm} and $R_{channel}$, and one term has a negative temperature coefficient: V_{P+N-}. As a result, their global temperature coefficient is positive.

Now, the PT-IGBT has a very low carrier lifetime, giving a large value for α_τ. Their R_{vm} temperature coefficient is rather negative. So now, two parameters have a negative temperature coefficient: R_{vm} and V_{P+N-}, while one term has a positive temperature coefficient: $R_{channel}$. Therefore, the PT-IGBT has a negative temperature coefficient.

The anode current I_A also has an influence on the forward voltage temperature coefficient. With a very low current, voltage drops in R_{vm} and $R_{channel}$ are small compared to those in V_{P+N-} (close to V_{AK0}). Thus, the temperature coefficient is negative, whatever the technology, PT or NPT. When I_A increases, the voltage drops in R_{vm} and $R_{channel}$ increase, and the whole temperature coefficient may be positive or negative, according to the R_{vm} temperature coefficient. With a large current, the part tied to the channel, $R_{channel}$, is preponderant and the temperature coefficient is positive whatever the technology. Figure 2.27 shows static characteristics I_A, V_{AK} at 25°C and 125°C, for a 1,200 V, 150 A NPT-IGBT, and a 1,200 V, 100 A PT-IGBT.

Charge recombination rates are respectively 20 µs and 0.4 µs. We can see that the 25°C and 125°C curves cross, whatever the technology. However, the cross point is located at very low current for the NPT-IGBT, and at a higher current level for the PT-IGBT.

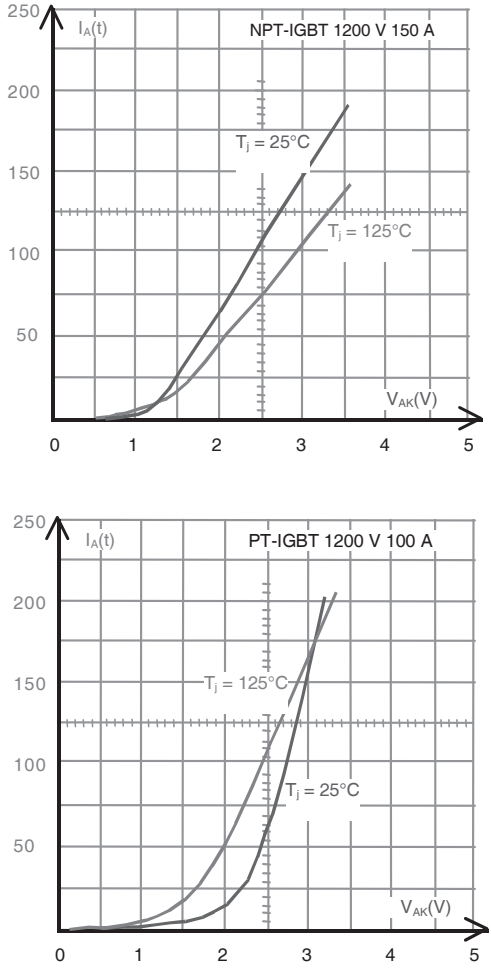


Figure 2.27. *I_A, V_{AK} characteristics versus temperature*

Temperature makes a stored charge increase and a channel conductivity decrease, so the overall IGBT switching performances are worse when temperature increases. For the hard switching operation, the switch-on and switch-off speeds, $dI_A(t)/dt$ and $dV_{AK}(t)/dt$, are reduced and the tail current is seriously enlarged (see

Figure 2.28a and b). For the soft switching operation, the increase of temperature damages the dynamic voltage (ZVS), increases the re-starting current (ZCS), and so makes an increase of switching losses (see Figure 2.28c and d).

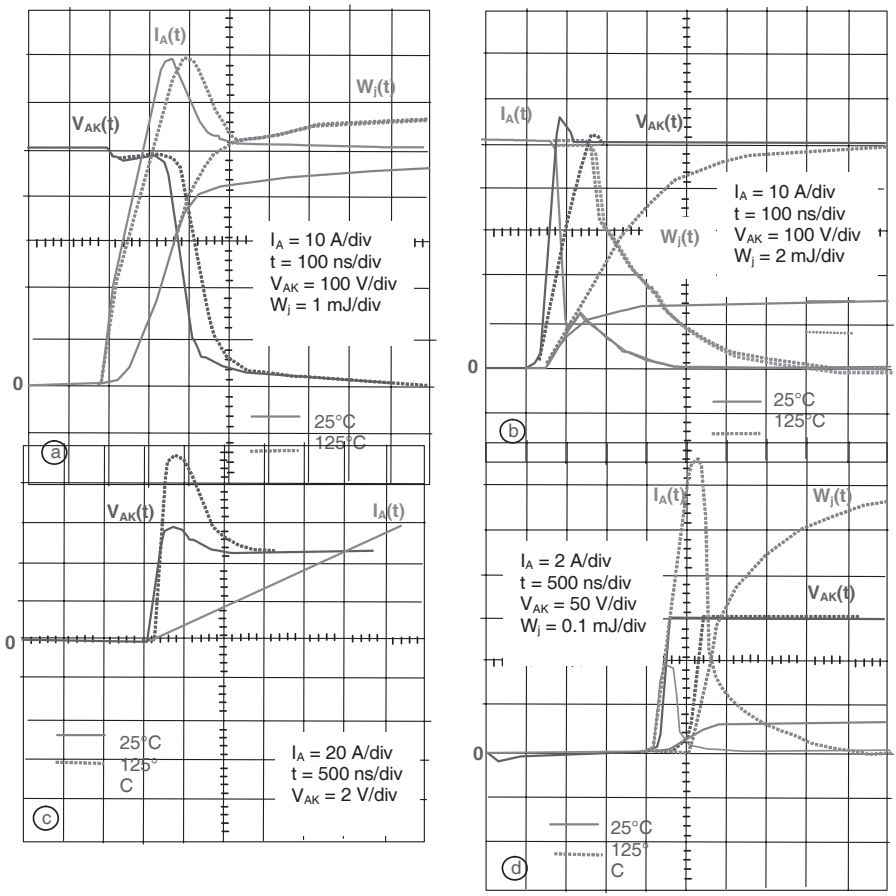


Figure 2.28. *a) Hard switching turn-on, b) hard switching turn-off, c) ZVS turn-on d) ZCS turn-off*

2.8. Over-constraint operations

2.8.1. *Overvoltage*

Overvoltages may occur on gate or anode. Channel structure for MOSFET or IGBT is the same, so the remarks made for the MOSFET in over-constrained

regimes are the same. Anode-cathode avalanche sustaining voltage is less for IGBT than for MOSFET, due to the internal PNP. Even if the IGBT are specificed as sustaining an avalanche voltage, of lower magnitude than the MOSFET, it is advised to use an avalanche protection between anode and cathode for a longer lifetime. While the NPT-IGBT has a thick drift zone, and while the PNP bipolar transistor is weaker than that in the PT technology, this NPT technology is better in terms of sustaining an avalanche.

2.8.2. *Over-current*

If the mounting procedure is sound, two phenomenons roughly limit the anode current density in the transient regime of an IGBT: the parasitic thyristor switch-on, and the N- drift zone avalanching at high current density (also called dynamic avalanche). The parasitic thyristor turns on when:

$$J_{A\max(Thy)} < (1+\frac{1}{\beta_{PNP}})\cdot\frac{0.6}{R_P \cdot S_{Si}}$$

Resistance R_p (according to Figure 2.29) is given by:

$$R_P = \frac{L_P}{H \cdot Z}\cdot\frac{1}{q\mu_p N_A}$$

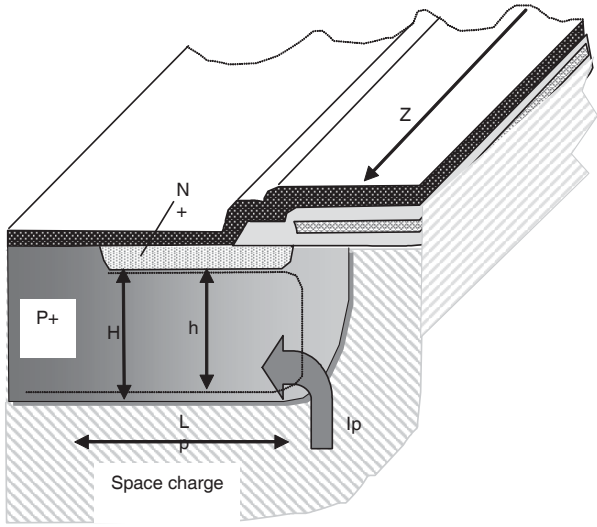


Figure 2.29. *R_p in the Pwell, with a hole current*

For a Pwell defined by L_p = 6 µm, $N_A = 10^{17}$ cm^{-3}, H = 10 µm, μ_p = 300 $cm^2.V^{-1}.s^{-1}$, Z = 5m per square centimeter of silicon, resistance R_p is equal to 0.25 mΩ. The theoretical density $J_{Amax(thy)}$ achieved is 9.6 $kA.cm^{-2}$ and 4.8 $kA.cm^{-2}$ respectively, for a β_{PNP} of 0.3 or 1 we can see that these values are very large.

$J_{Amax(thy)}$ is also linked to the operation conditions. Due to the space charge extension in the P region of the Pwell when the applied voltage on the anode increases, the way through for holes shrinks, causing a $J_{Amax(thy)}$ reduction. This effect is not important, due to the great dissymmetry in the doping levels N_A and N_D. For example, an anode voltage of 600 V leads to an H-h of 0.1µm. Temperature also has a negative effect on the triggering current density, because it decreases the hole mobility in the Pwell. For example, $J_{Amax(thy)}$ is divided by two when the temperature increases from 25°C to 125°C. Voltage and temperature increase the β_{PNP} gain, which in turn reduces $J_{Amax(thy)}$. As a conclusion, today, the parasitic thyristor of IGBT is no longer a difficulty if the maximum gate voltage is respected.

If an over-current occurs together with a gate overvoltage, the channel current could potentially be high enough to switch the thyristor on. The maximum current versus gate overvoltage (<20 V) assessment is complex. The following expression can approximate the maximum current if a high level modulated region and a space region divide the drift zone:

$$J_{A\max} = (1+\frac{1}{b})\left[\frac{K^*_p}{2}(V_{GK\max} - V_{th})^2 + \frac{2DQ^*_{\max}}{W_{m(\min)}^2}\right]$$

where Q^*_{max} and $W_{m(min)}$ represent the maximum stored charge density and the modulated regions minimum thickness.

This equation shows that J_{Amax} is larger when V_{GK} increases. If J_{Amax} is compared to MOSFET J_{Dmax}, equations show the additional hole current in the IGBT. Figure 2.30a shows J_{Amax} versus gate overvoltage, for an experimental example. At high V_{GK}, a saturated behavior occurs for J_{Amax}, under a high electric field, due to electron mobility reduction in the channel. Despite this self limitation, current density J_{Amax} can be very high if the gate overvoltage is excessive, and thus, switch-on of the thyristor could occur, (see Figure 2.30b). Therefore, a gate overvoltage protection must be used.

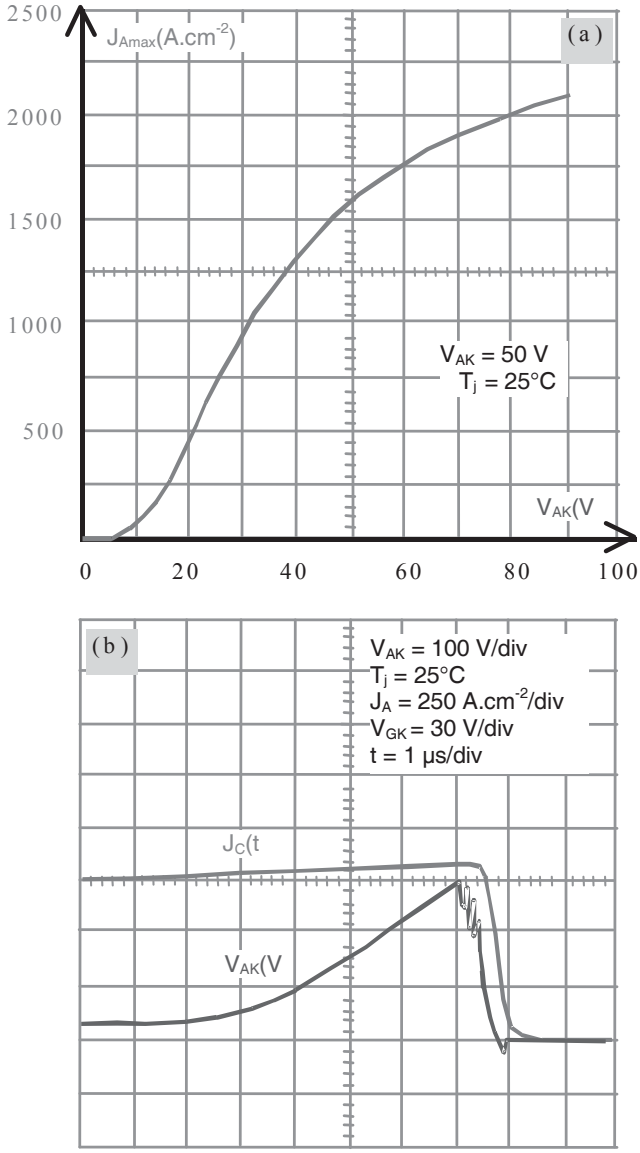


Figure 2.30. *a) Max current density with high gate voltage; b) NPT-IGBT parasitic thyristor switch-on*

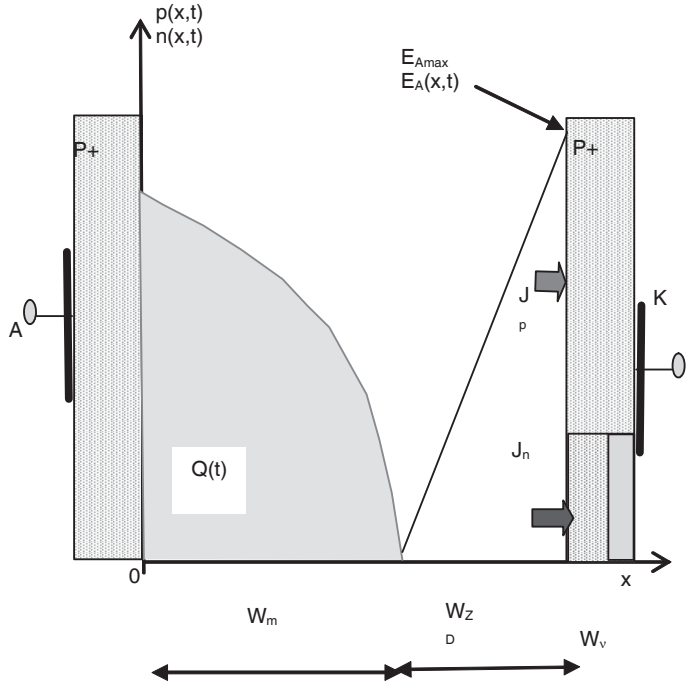
With an applied voltage on anode-cathode terminals, an electric field is installed in the drift zone, if it exists, and at the same time a high anode current is applied. The electric field peak can be amplified, and may raise the silicon critical field. At this time, a dynamic avalanche occurs. The following equation ties the electric field and the space charge (see Figure 2.31a):

$$\frac{dE_A(x,t)}{dx} = -\frac{q}{\varepsilon_{si}}[N_D + p(x,t) - n(x,t)] = -\frac{q}{\varepsilon_{si}}[N_D + \frac{1}{qv_n(x,t)} \cdot \frac{K_{PNP}(x,t)\delta(x,t) - 1}{1 + K_{PNP}(x,t)} \cdot J_A]$$

where $\delta(x,t)$ is the ratio between hole and electron speeds $v_n(x,t)/v_p(x,t)$, and $K_{PNP}(x,t)$ is the ratio between hole current and the electron current densities $Jp(x,t)/Jn(x,t)$.

Reasonably, $K_{PNP}(x,t)$ can be exchanged with the PNP bipolar transistor dynamic gain, β_{PNPdyn}, and we can assume that this gain is constant along the space charge. Electron speed is three times higher than the hole speed at a low electric field, but these two speeds are the same ($v_{ns} = v_{ps} = 10^7 cm.s^{-1}$) when the field is higher than 5 $V.\mu m^{-1}$. Then the field E_{Amax} raises the silicon critical field E_{simax}. $E_A(x,t)$ is higher than 5 $V.cm^{-1}$ on a large part of the space charge. Consequently the hypothesis $\delta(x,t) = 1$ on the whole space charge can be considered as acceptable (see Figure 2.31b). Thus, the previous equation becomes:

$$\frac{dE_A(x,t)}{dx} = -\frac{q}{\varepsilon_{si}}[N_D + \frac{1}{qv_{ns}} \cdot \frac{\beta_{PNPdyn} - 1}{1 + \beta_{PNPdyn}} \cdot J_A]$$



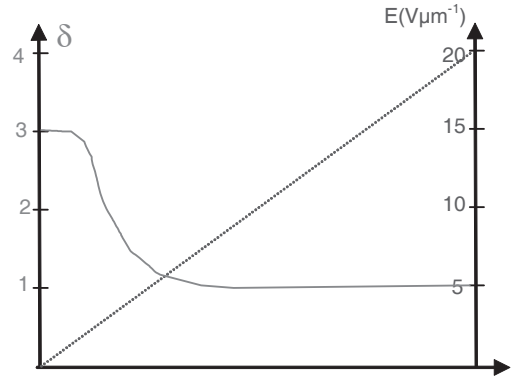


Figure 2.31. *Simultaneous occurrence of high voltage and large current in the drift zone*

We can see that β_{PNPdyn} is a determinant factor in the avalanche effect due to high current, influencing the effect in three ways:

– Hole current density is equal to electron density, β_{PNPdyn}= 1: therefore, no dynamic avalanche affects the electric field.

– Hole current density is higher than the electron current density, $\beta_{PNPdyn} > 1$. Field gradient increases with current. For a given V_{AK} voltage, when the current density increases, E_{Amax} becomes larger. Avalanching phenomenon occurs when E_{Amax} raises the silicon critical field, for example at 20 V.cm^{-1} for $N_D = 10^{14}$.cm^{-3}.

– Hole current density is less than the electron current density, $\beta_{PNPdyn} < 1$: field gradient decreases with the current, so no dynamic avalanching occurs.

Short circuit is an important constraint for IGBT dynamic avalanche. Figure 2.32 shows the short circuit waveforms of a 1,200 V, 25 A NPT-IGBT, when the load circuit V_{AK} imposes $V_{AK} = V_{SC}$, and the current is fixed by the IGBT, formulated by:

$$J_{SC}(t) = J_n(t) + J_p(t) = \frac{K^*_p}{2}(V_{GK} - V_{th})^2 + J_p(t)$$

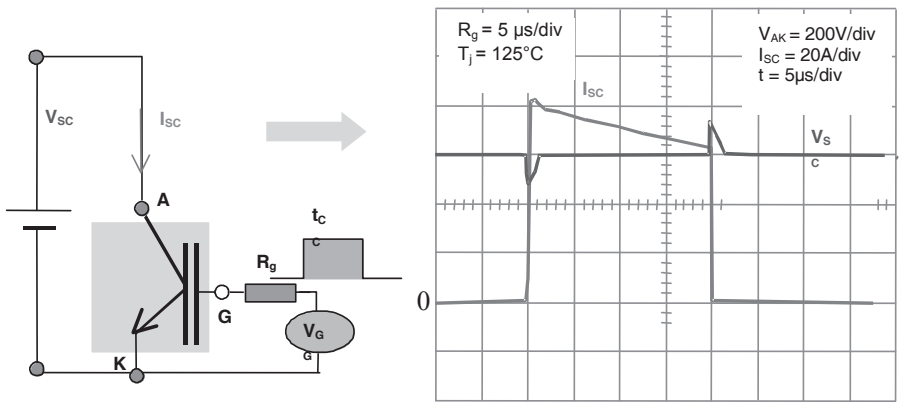


Figure 2.32. *Short circuit waveforms for a 1,200 V, 25 A NPT-IGBT*

Electron current part, $J_n(t)$, is established and rises to its maximum almost instantaneously when the short circuit occurs, because it follows the $V_{GK}(t)$ voltage. It then decreases with the short circuit because of the increase in temperature, due to losses. Hole current is established slowly, because it follows the speed of storage of charges. So, the short circuit current is, at the beginning, mainly an electron current, and, in the following of the short circuit, the hole current increases until the short circuit current is established. Despite all of this, the short circuit current slightly decreases with time: hole current cannot compensate for the decrease due to the temperature of electron current.

Dynamic avalanche study, in the short circuit case, consists of determining the maximum short circuit current density that the IGBT can sustain with a given V_{SC}. For that, β_{PNPdyn} must be determined as precisely as possible, because dynamic avalanche is completely dependant on it. However, β_{PNPdyn} varies with time, and knowledge of hole current evolution during short circuit is required. One hypothesis considers that the modulated region W_m is entirely at high level, and that charge distribution is a decreasing function. According to this hypothesis, hole current density is:

$$J_p(t) = \frac{J_n(t)}{b} - qD(1+\frac{1}{b})\cdot\frac{dp(x,t)}{dx} > \frac{1}{b}J_n(t)$$

In this case, β_{PNPdyn} is necessarily higher than 1/b, which gives a hole current compulsorily higher than $I_{SC}/(1+b)$, or 25%. I_{SC}. If the short circuit is turned off by a quick drive, this hole current will be found in the current tail at switch-off.

By experience, in the short circuit conditions specified by manufacturers, this current is not really seen. It could be possible with a high PNP gain in a PT-IGBT with a short circuit voltage close to the maximum voltage. This means short circuit dynamic gain, β_{PNPdyn}, is much lower than 1/b, and the previous hypothesis is not always usable. It is necessary to get a more accurate model. For example, the modulated region may be divided in two regions: a high level first one close to the anode, and a low level second one close to the space charge.

Instead of determining β_{PNPdyn}, it could be better to use it as a parameter. If a linear distribution for the electric field in the space charge is considered, the current density limit imposed by the avalanche, for $\beta_{PNPdyn} > 1$, is:

$$J_{A\max} \le \frac{1+\beta_{PNPdyn}}{\beta_{PNPdyn}-1}\cdot\{\frac{E_{Si\max}^{\ 2}}{2V_{AK}}v_{ns}\varepsilon_{si} - qN_D v_{ns}\}$$

Figure 2.33 shows this limitation for two different β_{PNPdyn} gains, 2 and 1.5, with an identical doping level $N_D = 10^{14}.cm^{-3}$. With a low anode voltage, the limiting density tied to dynamic avalanche is relatively large, therefore, only the thyristor switch-off sets the maximum density, a density which is preponderant when the anode voltage is high.

Electron current flow is possible only if the channel is conducting. The limit density given by the previous equation represents a theoretical Forward Bias Safe Operating Area (FBSOA). After the short circuit switch-off, channel is opened and only a hole current (current tail) is going through the space charge; $\beta_{PNPdyn} = \infty$. Its limit density imposed by the dynamic avalanche is:

$$J_{p\max} = J_{tail\max} \le \frac{E_{Si\max}^{\ 2}}{2V_{AK}} v_{ns}\varepsilon_{si} - qN_D v_{ns}$$

With a fast switch-off drive, J_{Dmax} may be combined with the hole current during the short circuit, thus the reverse safe operating area in short circuit, for the IGBT, may be defined (see Figure 2.33b) as:

$$J_{A\max} \le \frac{1+\beta_{PNPdyn}}{\beta_{PNPdyn}} \cdot \{\frac{E_{Si\max}^{\ 2}}{2V_{AK}} v_{ns}\varepsilon_{si} - qN_D v_{ns}\}$$

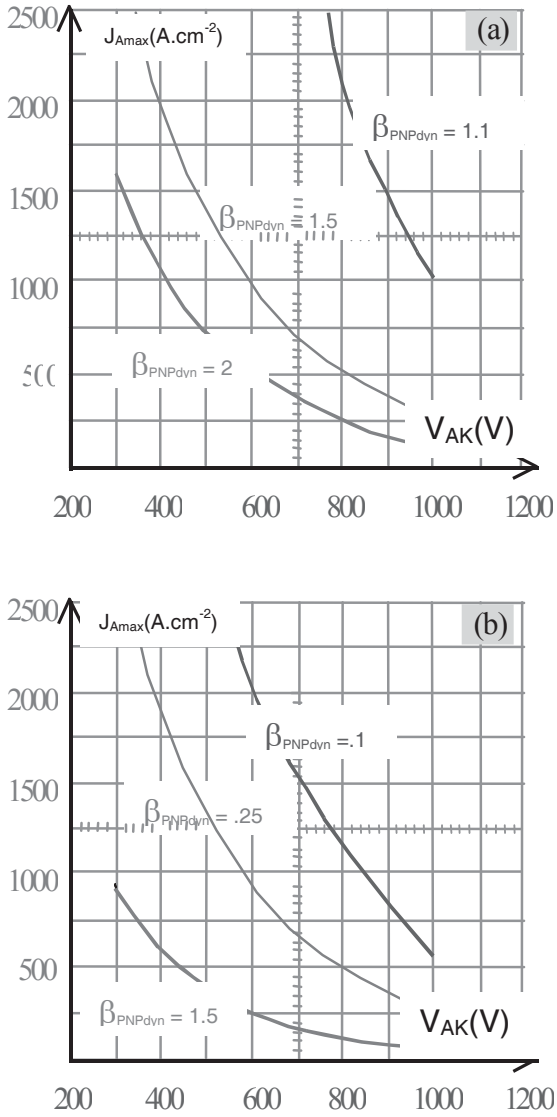


Figure 2.33. *Short circuit security areas: a) forward, for $\beta_{PNPdyn} > 1$ (no constraint for $\beta_{PNPdyn} \leq 1$); b) reverse*

If charts a) and b) from Figure 2.33 are compared, we can clearly see that the reverse safe operating area in short circuit is smaller than the area in forward short circuit.

The NPT-IGBT has a thick drift zone, which in turn gives a large W_m modulated base for the short circuit, and so a low dynamic gain $\beta_{PNPdyn} << 1$. Therefore, it can sustain large current densities under high V_{SC}, without any dynamic avalanche. Now, the PT-IGBT, with a thin drift zone, has a thin modulated base, and is weaker than the previous one. So, its β_{PNPdyn} gain is larger, and its reverse safe operating area in short circuit is smaller. In Figure 2.33, the β_{PNPdyn} gain is assumed to be constant versus short circuit voltage V_{SC}. This hypothesis is good for the NPT-IGBT thanks to its thick drift zone. For the PT-IGBT, the β_{PNPdyn} gain increases with the short circuit voltage. Accordingly, its short circuit reverse safe operating area is smaller, as seen in Figure 2.33. Inside this area, as with MOSFET, the maximum short circuit time t_{CC} only depends on silicon temperature or losses.

High switch-off current, in hard switching operations on an inductive load, may also lead the IGBT to a dynamic avalanche. In contrast to the short circuit, anode current is set by the load, rather than the IGBT itself. Until the anode voltage has not reached the supply voltage. The hole density current during switching is:

$$J_p(t) = J_A - C^*_{ZD}\frac{dV_{AK}(t)}{dt} - J_{channel}(t)$$

and is maximum when the channel is opened, with $J_{channel} = 0$. Thus:

$$J_p(t) = J_A - C^*_{ZD}\frac{dV_{AK}(t)}{dt}$$

To avoid the dynamic avalanche, current density must be limited to:

$$J_{A\max} \le \frac{E_{Si\max}^{\ 2}}{2V_{AK}(t)} v_{ns}\varepsilon_{si} - qN_D v_{ns}$$

To reduce losses, a fast drive is generally used. This means the channel turns off before the supply voltage rises (see Figure 2.34). In this case, only the hole current goes through the space charge (while $J_{channel} = 0$), and the previous expression becomes:

$$J_{A\max} \le \frac{E_{Si\max}^{\ 2}}{2V_{AK}(t)} v_{ns}\varepsilon_{si} - qN_D v_{ns} + C^*_{ZD}\frac{dV_{AK}}{dt}$$

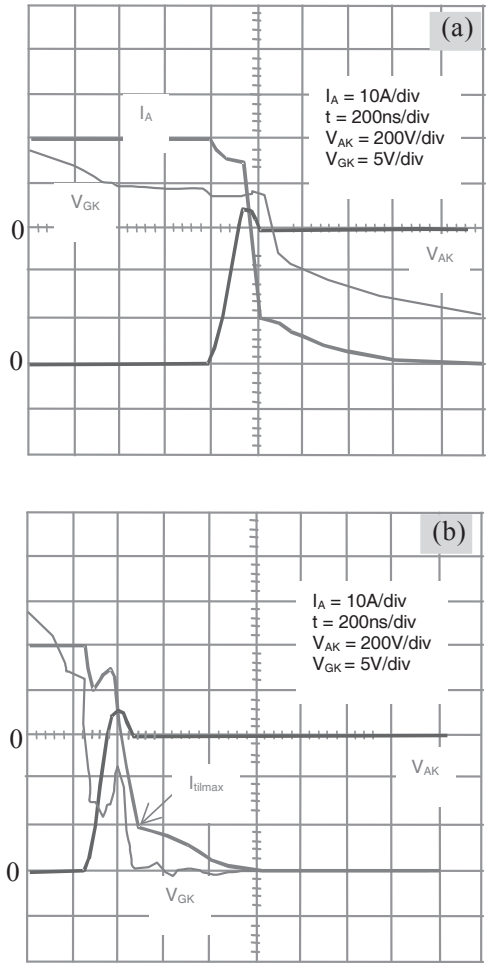


Figure 2.34. *Hard switching on inductive load switch-off: a) low drive, b) fast drive*

If the term $dV_{AK}(t)/dt$ is neglected, Figure 2.35 shows this current density versus the supply voltage. This constitutes the switch-off safe operating area for an inductive load (RBSOA). We can clearly see that this area is reduced when the anode voltage increases. However, this limitation is not entirely restrictive, due to two favorable facts:

– The rise of the anode voltage is very short because the speed $dV_{AK}(t)/dt$ with a very fast drive is very quick (tens of kV/µs): avalanching could only occur over a very short time.

– Hole current instantaneously decreases to a very low value, corresponding to the beginning of the tail, at the end of anode voltage gradient. This allows for a maximum field reduction.

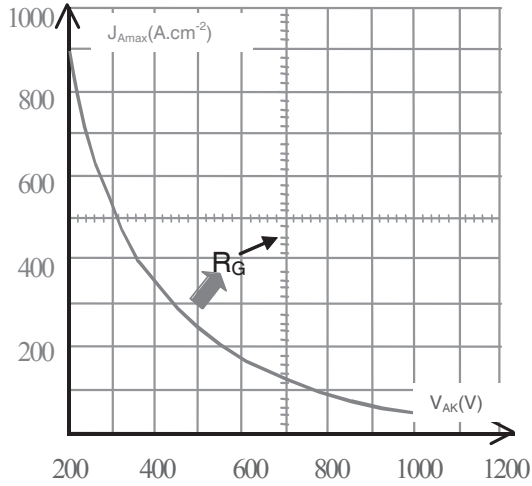


Figure 2.35. *Theoretical current limit density on an inductive load switch-off, during the anode voltage rise, with a fast drive*

Figure 2.36 shows this dynamic avalanche on a 1,200 V, 25 A NPT-IGBT. It can be seen that the dynamic avalanche occurs in a very short time. It is made at 710 V, 66 A, so for a current density of 165 A.cm^{-2}.

If the gate drive is slowed down, generally through R_G, the channel can continue conducting when the anode voltage is close to the Miller voltage. The more the channel is conducting, the more the area in Figure 2.35 is extended. If the channel current density becomes equal to or greater than the hole current density, this area becomes unlimited. When the anode voltage raises the supply voltage, the Miller voltage disappears and the channel is quickly opened. Electron current falls to zero and the hole current sustains the tail current. Its maximum value must not lead to dynamic avalanche. This is described by the following equation:

$$J_{tail\max} = J_{p\max} = (1+\frac{1}{b})\cdot\frac{2DQ^*}{W_m{}^2} \le \frac{E_{Si\max}{}^2}{2V_{AK}(t)}v_{ns}\varepsilon_{si} - qN_D v_{ns}$$

If Q*tail charge density can be blended with the conduction stored charges in this expression:

$$Q^* = (\gamma_p - \frac{\beta_{PNP}}{1+\beta_{PNP}}) \cdot J_A . \tau$$

a maximum charge density in conduction, which must not be exceeded, can be deduced:

$$Q^*_{\max} \leq \frac{b}{1+b} . \frac{W_m^{\ 2}}{2D} \left[\frac{E_{si\max}^{\ 2}}{2V_{AK}(t)} \nu_{ns} . \varepsilon_{si} - qN_D \nu_{ns} \right]$$

and finally the maximum current is achieved:

$$J_{A\max} \leq A_p \cdot \left[\frac{E_{Si\max}^{\ 2}}{2V_{AK}(t)} v_{ns} \varepsilon_{si} - qN_D v_{ns} \right]$$

with:

$$A_p = \frac{b}{1+b} \cdot \frac{1}{(\gamma_p - \frac{\beta_{PNP}}{1+\beta_{PNP}})} \cdot \frac{1}{2\tau D} \left[W_\nu - \sqrt{\frac{2\varepsilon_{si} V_{AK}}{qN_D}} \right]^2$$

This A_p coefficient is the ratio between the conduction current density and the tail maximum density. It must be greater than one, the highest possible value being preferred.

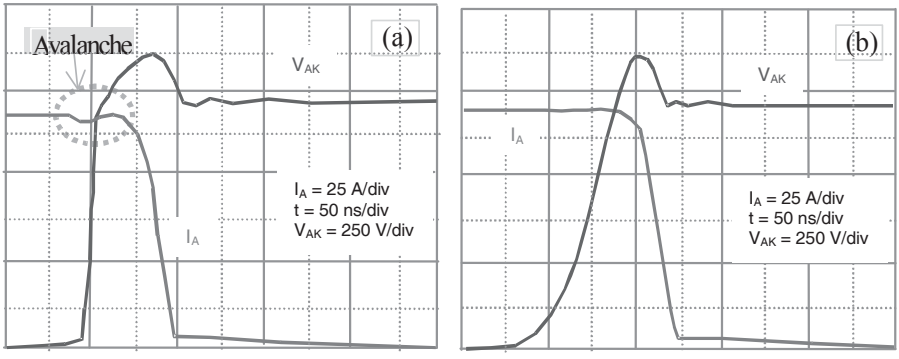


Figure 2.36. *Dynamic avalanche during hard switching -off on an inductive load: a) very low R_G with avalanche; b) high R_G without avalanche*

For this to occur, four parameters must be optimized: injection coefficient γ_p, static gain β_{PNP}, charges lifetime τ, and drift zone thickness W_v. For example, γ_p and τ may be reduced, while β_{PNP} and W_v may be increased, but as a drawback for static performances. Figure 2.37 shows two curves formed from the following numerical values:

$$\gamma_p = 0.4,\ W_v = 220\mu m,\ \beta_{PNP} = 0.4,\ \tau = 10\mu s,\ N_D = 10^{14}.cm^{-3}$$

$$\gamma_p = 0.4,\ W_v = 120\mu m,\ \beta_{PNP} = 0.4,\ \tau = .5\mu s,\ N_D = 10^{14}.cm^{-3}$$

The current density allowed by the dynamic avalanche decreases when the voltage increases, this limitation is more severe when the drift zone is at its narrowest (in the case of PT-IGBT). Current tail evolution is slower when the voltage increases. Therefore, avalanche, if it is possible, can spread out. Figure 2.37 shows the switch-off safe operating area on an inductive load (RBSOA).

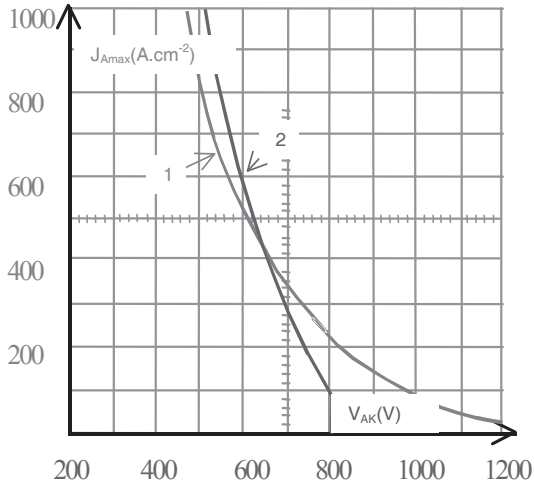


Figure 2.37. *Current density limit tied to the dynamic avalanche, at switch-off, on an inductive load*

In this section, theoretical density limits were studied versus V_{AK} voltage, following two criteria: parasitic thyristor switch-on; and dynamic avalanche, by overpass of the critical field limit. They are very complex phenomenons making their study quite difficult. Some results were shown and experiments confirmed them to be at least a tendency. IGBT are weaker than MOSFET, in over-constraint operations, due to the hole current. Now, the portion of hole current in the total

current is less inside the NPT-IGBT than the portion inside the PT-IGBT: this means NPT-IGBT are stronger in over constraint operations. Parasitic thyristor switch-on occurs at high current density; therefore it cannot be achieved if the gate voltage is maintained under the specified value, except in the case of a high transconductance parameter, K_p. The reverse safe operating area is the main limitation for short circuit current density. During short circuit, or during inductive load switch-off, the reverse safe operating area becomes smaller and smaller when the anode voltage V_{AK}, the static gain β_{PNP}, and the dynamic gain β_{PNPdyn} increase.

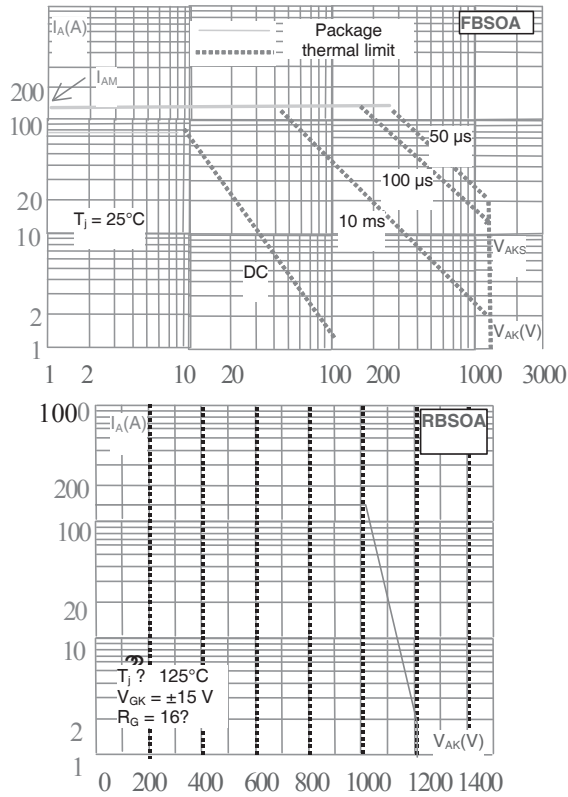


Figure 2.38. *1200 V, 75 A PT-IGBT*

2.8.3. *Manufacturer's specified safe operating areas*

All manufacturers give, for the over-constraint operations, a forward safe operating area, FBSOA, and a reverse safe operating area, RBSOA (or SSOA). Inside theses areas, current density is much lower than what was seen in the

previous chapter. The main explanation for this difference is that in the former study only physical criteria were used, while thermal and assembly constraints were forgotten. As with the I_{DM} MOSFET in the manufacturer data sheets, a maximum pulsed current I_{AM} is set, by case temperature, and it is around two to four times the operating current. Figures 2.38 and 2.39 show safe operating areas for a PT-IGBT and an NPT-IGBT, with 1,200 V, 75 A ratings. The PT-IGBT reverse safe operating area is restricted over 1,000 V, while, for the NPT-IGBT, it remains quite rectangular. These areas show three types of constraints:

– maximum sustaining Voltage V_{AKS} (V_{CES});

– junction thermal limit (around 150°C);

– maximum current I_{AM}(I_{DM}), mainly set by the internal connections.

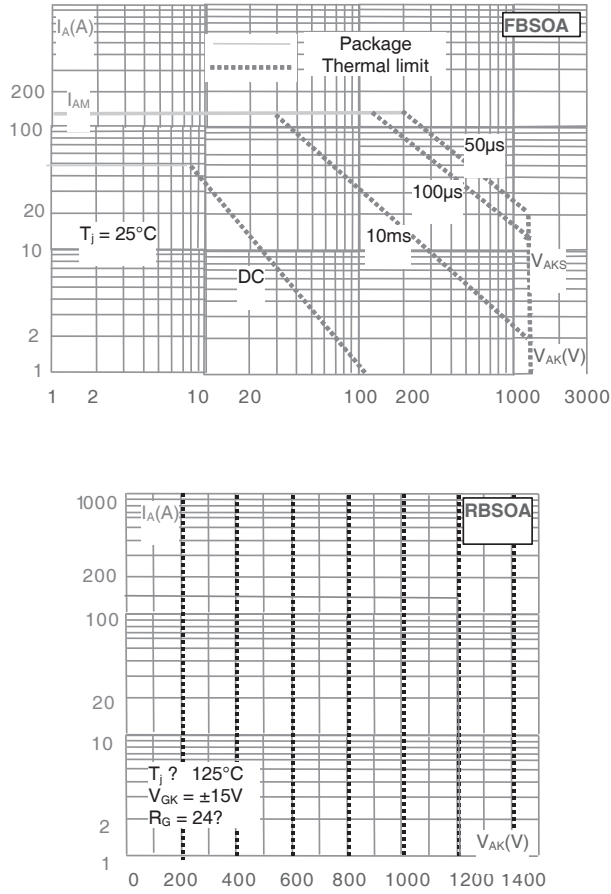


Figure 2.39. *1,200 V, 75 A NPT-IGBT*

For the short circuit, the main parameters are: initial temperature, drive voltage V_{GK} and short circuit duration t_{sc}. Most of the specifications give a maximum short circuit duration, t_{sc} = 10 µs, with an applied voltage V_A (or V_{CC}) between 50% and 70% of V_{AKS} (or V_{CES}), with a case temperature of 125°C, and a drive voltage V_{GK} = ±15 V. Several manufacturers also give a Short Circuit Safe Operating Area (SCSOA). Figure 2.40 shows two examples.

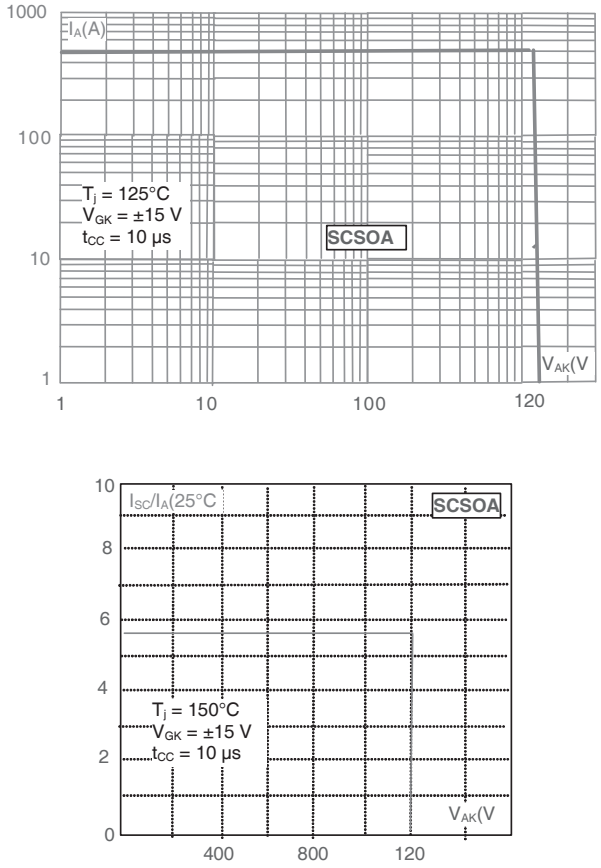


Figure 2.40. *Short circuit safe operating areas for NPT-IGBT, 1,200 V, 75 A and 25 A*

2.9. Future of IGBT

2.9.1. *Silicon evolution*

All devices under 1,500 V are built with epitaxial wafers. For IGBT, with voltages between 600 V and 1,500 V, and with a P+ substrate, this is difficult because substrate thickness is more than 100 µm, which means a large hole injection. The manufacturer needs to make a lot of particular operations in order to control the stored charges, such as N+ buried layer and electronic irradiation. For a high voltage device, this is easier to achieve utilizing a technical process called "float zone" (FZ), a thick N- substrate (10V by micron), which will be the drift zone, can be used, and the IGBT anode is made by back P+ diffusion or implantation. Today, for IGBT voltages under 2,000 V, thin wafer can be used, which allows for good control of drift zone thickness and the P+ anode diffusion layer, thus limiting the use of irradiation. Thin wafers also allow much better V_{AKsat} control, this being the main parameter for controling losses in a high current IGBT (see Figure 2.41).

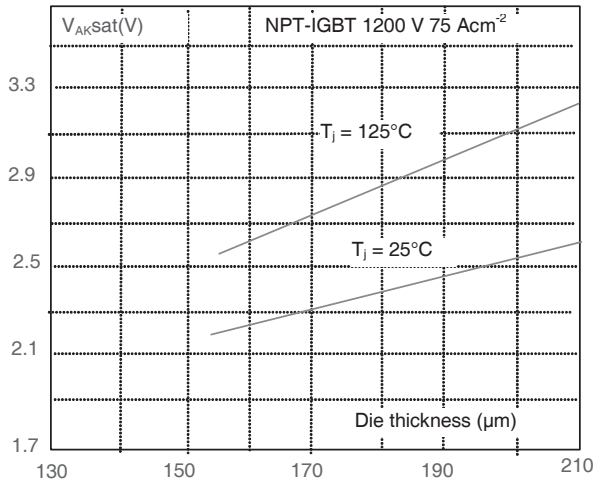


Figure 2.41. *Voltage drop versus die thickness*

Figure 2.42 shows all the IGBT technological evolutions, beginning around 1990. First, was the NPT (non punch through) technology with an epitaxial N- drift zone, and a die thickness around 300 µm, less and less used today. Second, came the PT technology, starting with the FZ technology (thin wafer for low voltage devices). This was the cheapest technology, being without N layer and irradiation, and also less sensitive to temperature. Finally, came "soft punch though" technology, again

with a buried N layer, however, this time with a good compromise between switching speeds and drop voltages, V_{AKsat}.

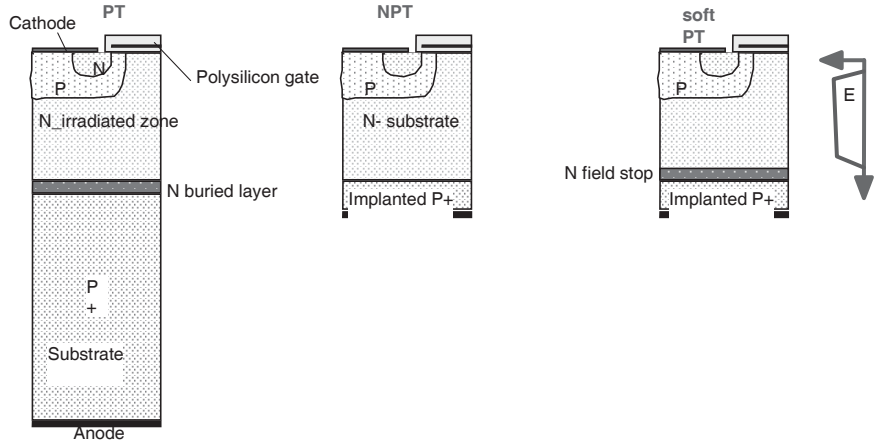


Figure 2.42. *The three IGBT technologies with the same scale, for low voltage devices (600 V to 2,000 V)*

2.9.2. *Saturation voltage improvements*

During the conduction state, electron injection is significant, so the channel resistance must be as low as possible. The solution is very well known: increase the cell number or, today, use the "trench gate technology" shown in Figure 2.43.

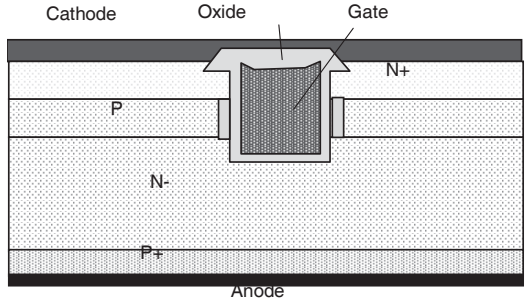


Figure 2.43. *Trench gate technology*

Saturation voltage can also be improved by using an old technology, used for GTO devices: non-connection for several gate digits. This way, the concentration of holes in the upper part of the IGBT is increased. This technology is called "IEGT: injection enhancement gate transistor", and can be seen in Figure 2.44.

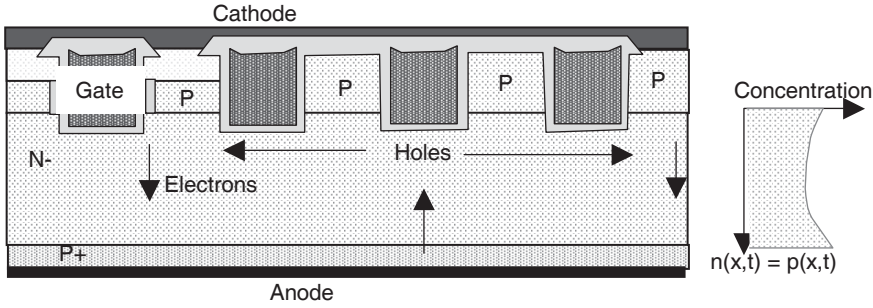


Figure 2.44. *IEGT technology*

This technology allows for an increase of current density by a factor of ten, for the same V_{AKsat}, in high voltage IGBT devices. From this same idea, Hitachi uses a technology called "hole barrier" (HiGT): this barrier consists of a N diffusion close to the Pwell. It stops the holes in this layer, making it highly modulated and lowering the saturation voltage (see Figure 2.45).

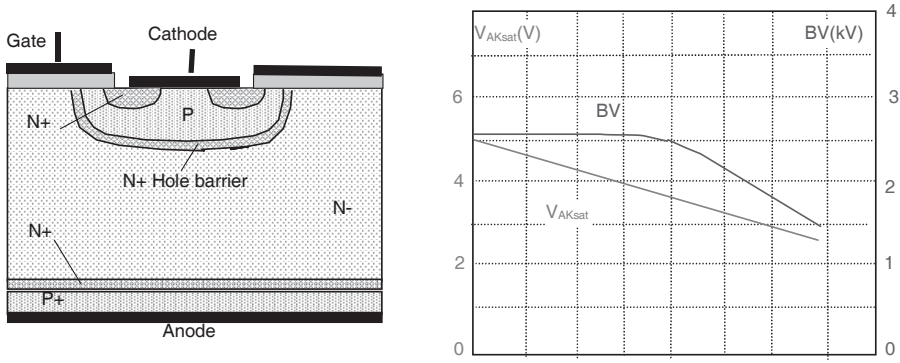


Figure 2.45. *HiGT technology*

2.10. IGBT and MOSFET drives and protections

2.10.1. *Gate drive design*

MOSFET or IGBT have combined input impedances: first a fixed capacitance made by the internal oxide between emitter and gate (or gate and cathode), and second a variable capacitance between gate and drain (or anode). They are non-linear, depending on sustained voltage and maximum current. The main design compromise is: a fast drive in order to reduce switching losses, or a slower drive to account for parasitic noises (EMC). Anyway, the drive loop must have a very low parasitic inductance to allow for both a fast drive and very low parasitic oscillations. After that comes the choice of R_G. It must be as low as possible to avoid any Miller capacitance drawback, but high enough to control the device speed. In terms of designing the gate drive, the chart of gate charge versus gate voltage is helpful (see Figure 2.13).

Switching time is $t = Q_G/I_G$, where Q_G may be divided into three parts (see Figure 2.46):

– Q_{GS} stored charges in C_{GS}, before the Miller capacitance, given by the charges produced by the gate on the upper part of the drain when $V_{GD} = 0$,

– Q_{GD} stored charges during the “plateau”,

– and $Q'_{GS} + Q'_{GD}$ charges, to charge the Miller and the geometrical capacitances in series.

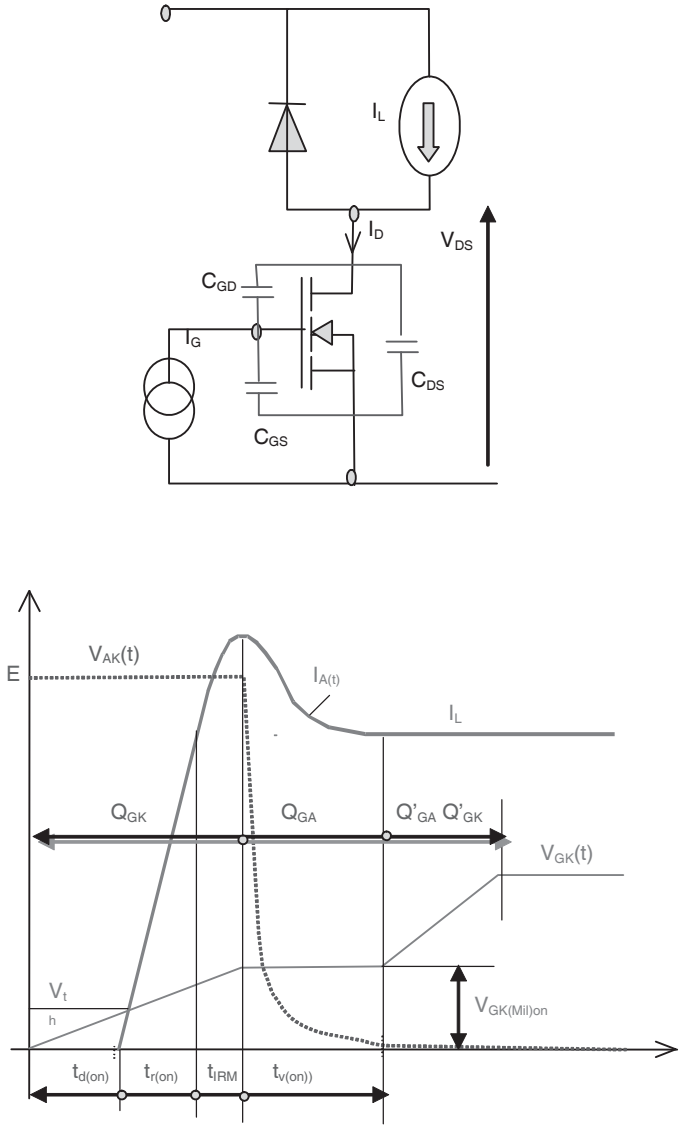


Figure 2.46. *Switch-on for an inductive load*

The Miller effect depends on switching conditions. Switching a higher current and a higher voltage increases the Miller effect (see Figure 2.47).

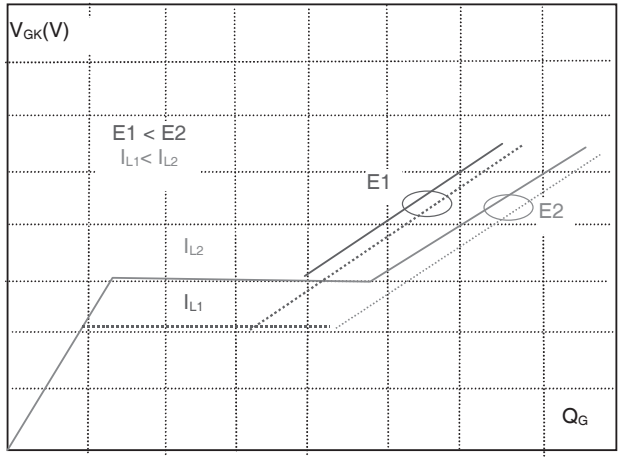


Figure 2.47. *Gate charge versus loads*

For instance, if the gate charge of the MOSFET shown in Figure 1.30 is considered: total charge quantity Q_G is 64 nC, for a gate voltage of 12 V, in a power circuit with a V_{supply} of 400 V and current of 8 A. To get to the end of the Miller effect, $Q_{GS} + Q_{GD}$ are around half, so 32 nC. The gate peak current is:

$$I_{G\max} = \frac{Q_{GS} + Q_{GD}}{t_{d(on)} + t_{r(on)} + t_{IRM} + t_{v(on)}} = \frac{Q_{GS} + Q_{GD}}{t_{on}}$$

For a switch-on time t_{on} of 100 ns, a gate peak current of 0.32 A is needed.

For a working frequency of 100 kHz, the drive power is:

$$P_G = Q_G.V_{GS}.F = 64.10^{-9}.12.10^5 \approx 77 \text{ mW}$$

This is very low compared to the power controlled: 400 V with 8 A.

2.10.2. *Gate drive circuits*

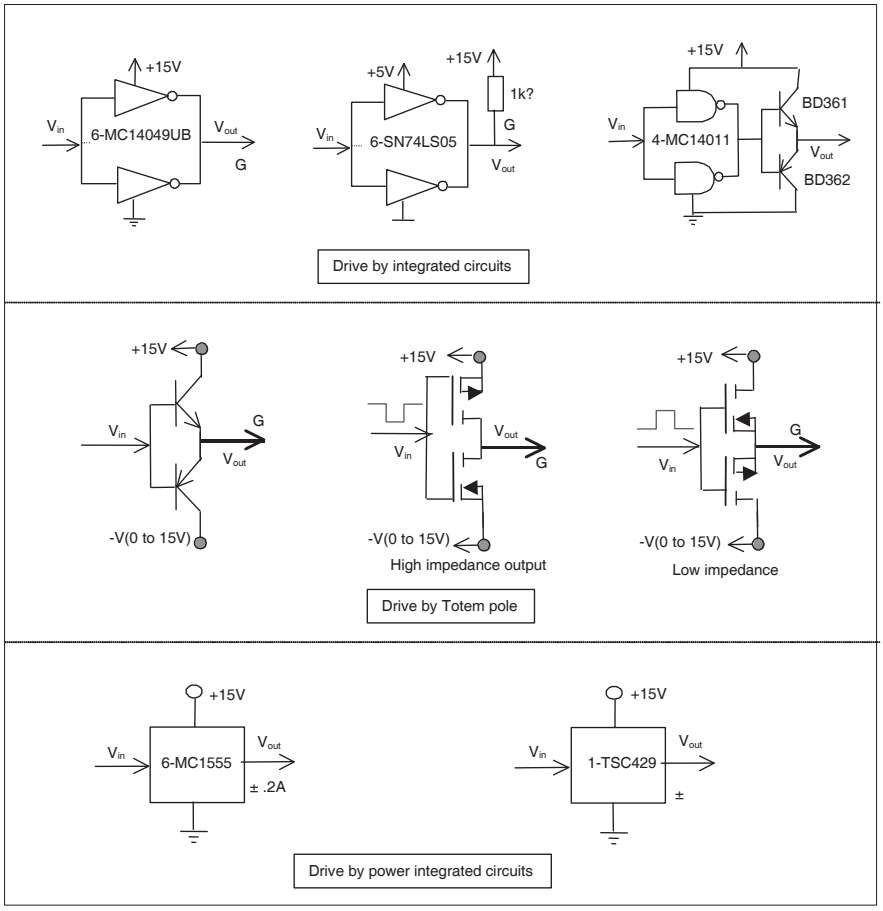


Figure 2.48. *MOSFET and IGBT discrete drives*

MOSFET and IGBT gate drives are the same. Only for high current IGBT might it be better to use $V_G = \pm 15$ V in order to protect the device against the counter reactive drawbacks of the Miller capacitance, and against high dV/dt. There are numerous gate drive circuits with a choice of criteria:

– speed with working frequency;

– load current driven;

– negative voltage drive; and

– galvanic insulation.

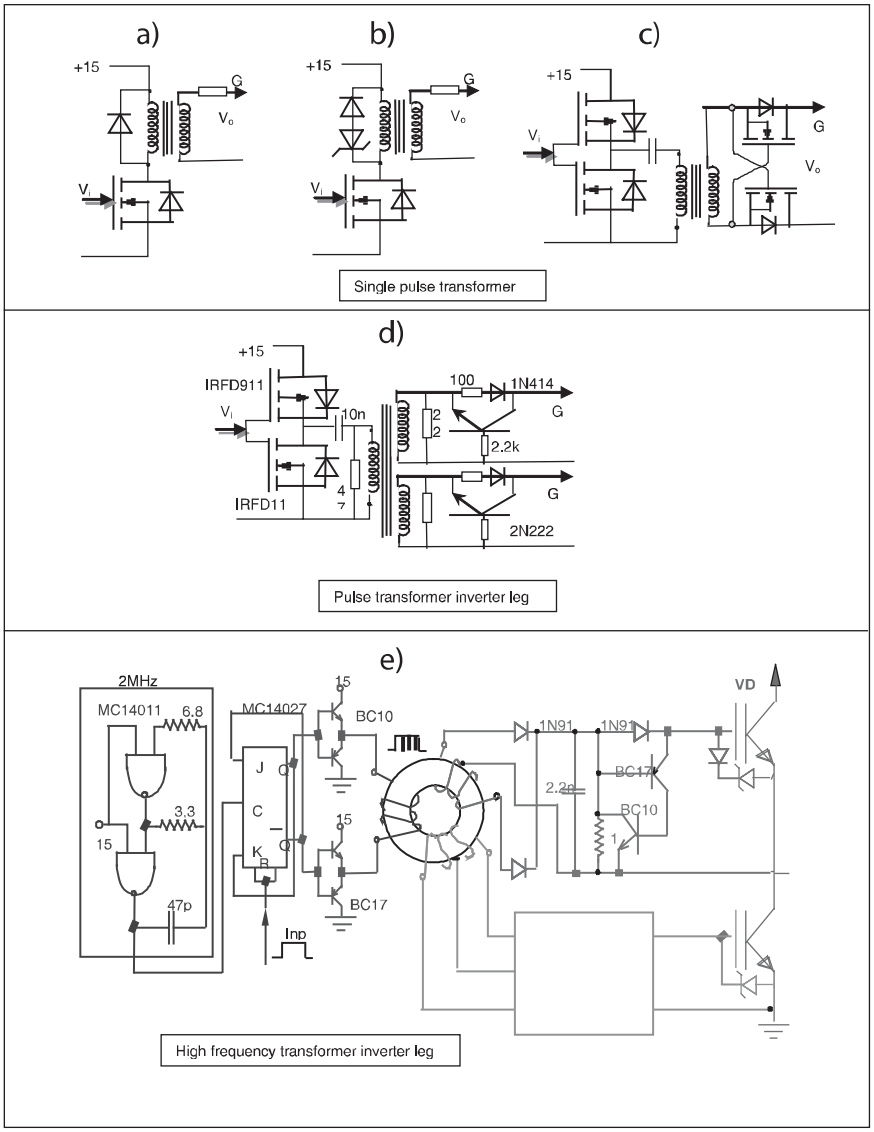


Figure 2.49. *MOSFET and IGBT transformer drives*

Figure 2.48 shows some classical drive circuits, made of various low power drive components. When integrated circuits are used, parallel connection of several integrated circuits is required most of the time (sometimes in a same package), in order to produce enough current to efficiently drive the MOSFET or IGBT. TTL

circuits are faster than the CMOS circuits, but their output voltage is, most of the time, too low (≤5 V) to directly drive the power device, but their open collector output allows for a direct connection to the auxiliary source (10 V to 15 V), through a "pull up" resistor, in order to obtain enough energy to drive the power device (this product family is normally used to drive low power devices). The resistance must be quite high in order to keep the TTL internal current low enough. This reduces the switch-on switching time.

The discrete drive circuit family is mainly represented by three "totem pole" types: first, with complementary bipolar devices; and second, with complementary MOS devices. The third can be divided into two other types: one with the emitter connected for a low impedance output, and the other with the drain connected for a high impedance output. It is very easy to drive these circuits with only one signal, because each of them excludes the other one when it is in the on-state. The drive reference could be the common connection, but due to the MOS or bipolar voltage drop, it is difficult to be less than the power device V_{th}, and it may be better to use a negative source for the bottom device connection. Some "push pull" drives also exist, made of MOS or bipolar. They are similar to the previous ones, however, they use the same polarity devices, and so need two opposite drive signals. Totem pole circuits are commonly used as they are very simple and efficient. Sometimes, they are used at the output of integrated circuits to directly drive the power device. Some power integrated circuits also exist to drive the power MOS or the power IGBT, with an output gate current of several amperes peak.

At the beginning, a lot of designers tried to use pulsed transformers (see Figure 2.49). The main advantage of these circuits is the galvanic insulation, which allows a lot of possibilities, mainly for floating references. It can also manage the drive signal, and gives enough energy to the gate.

Two basic elements must be taken into account for the pulsed transformer. On the primary side, applied voltage (assumed constant), multiplied by the time, must be under the magnetic saturation of the magnetic circuit. On the secondary side, conduction time, multiplied by the positive voltage, must be equal to the negative voltage, multiplied by the off-state time. This makes a strong limitation on the duty cycle. A lot of "tricks" are used to overcome this limitation. In Figure 2.49a, the basic principle is shown: if a zener is added (see Figure 2.49b), the duty cycle can be larger, however, it remains limited to 50% if $Vz \leq 15$ V. Figures 2.49c and 2.49d show two possible improvements for the duty cycle: adding a small capacitor on the primary side of the transformer (to avoid any transformer saturation); and using a memory circuit on the secondary side, which keeps the stored energy on the capacitance when the pulsed drive signal disappears. Nevertheless, transformer design is still difficult, due to the parasitic capacitances between transformer coils, which limit the dV/dt. Figure 2.49e shows a solution which provides a large duty

cycle with good immunity against dV/dt, by using a high frequency ring transformer. This allows few transformer turns, and so a low parasitic capacitance. A high frequency clock (for instance at 2 MHz) is cut off by the drive frequency (of for instance 100 kHz), in such a way that the transformer is designed for a 2 MHz frequency, while the secondary side of the transformer integrates and memorizes the drive signal.

Floating drive circuits are mainly requested for inverter leg drives, while the upper switch has a floating reference between zero volt and the applied voltage.

Combined with transformers, opto-electronic devices are good solutions. They make a very good insulation between drive and output. Figure 2.50a shows a basic opto-drive circuit. The optic fiber, in Figure 2.50b, has the same function as the transformer, however, if this optic fiber passes through a shield a good EMI insulation is obtained. Figures 2.50c and 2.50d show two double opto-drive circuits for large IGBT or MOS devices.

Figure 2.50e shows a voltage doubler (or charge pump) drives the upper side of the inverter leg, but this design is mainly limited to low power voltage and is quite slow (automotive applications by example).

Figure 2.50f is a resonant drive circuit. Resonance occurs between the input gate inductor and the internal MOS capacitances. This design provides an overvoltage, between 10 V and 15 V, from an auxiliary source of only 5 V.

A non-galvanic-insulated upper side drive circuit, may be created with two complementary drive devices (see Figure 2.51a). This design produces large duty cycles and is easy to make. The main limitations are the need for an auxiliary voltage of 15 V, other than the power voltage, and that the drive circuit is not protected against the power voltage by galvanic insulation.

A drive circuit is commonly used today for inverter legs: the “bootstrap” drive circuit. Figure 2.51b shows the principle. The energy needed to drive the upper side is stored in the external capacitor. When the lower switch is ON, a little diode is used in series in order to avoid any reverse current when the lower switch is off. An integrated high voltage logic circuit is used to translate the drive signal from the ground to the upper side.

Figure 2.51c shows the low voltage possibility of bootstrap. As MOS Q1 and the capacitor sustain the power voltage, an emitter follower, BD361 for instance, may be added to the basic circuit.

In conclusion, many high voltage integrated circuits are available on the market, to translate the signal and to charge the capacitor. Some of these HV-ICs can drive a three-leg inverter. The duty cycle is limited, in order to let enough time to charge the capacitor.

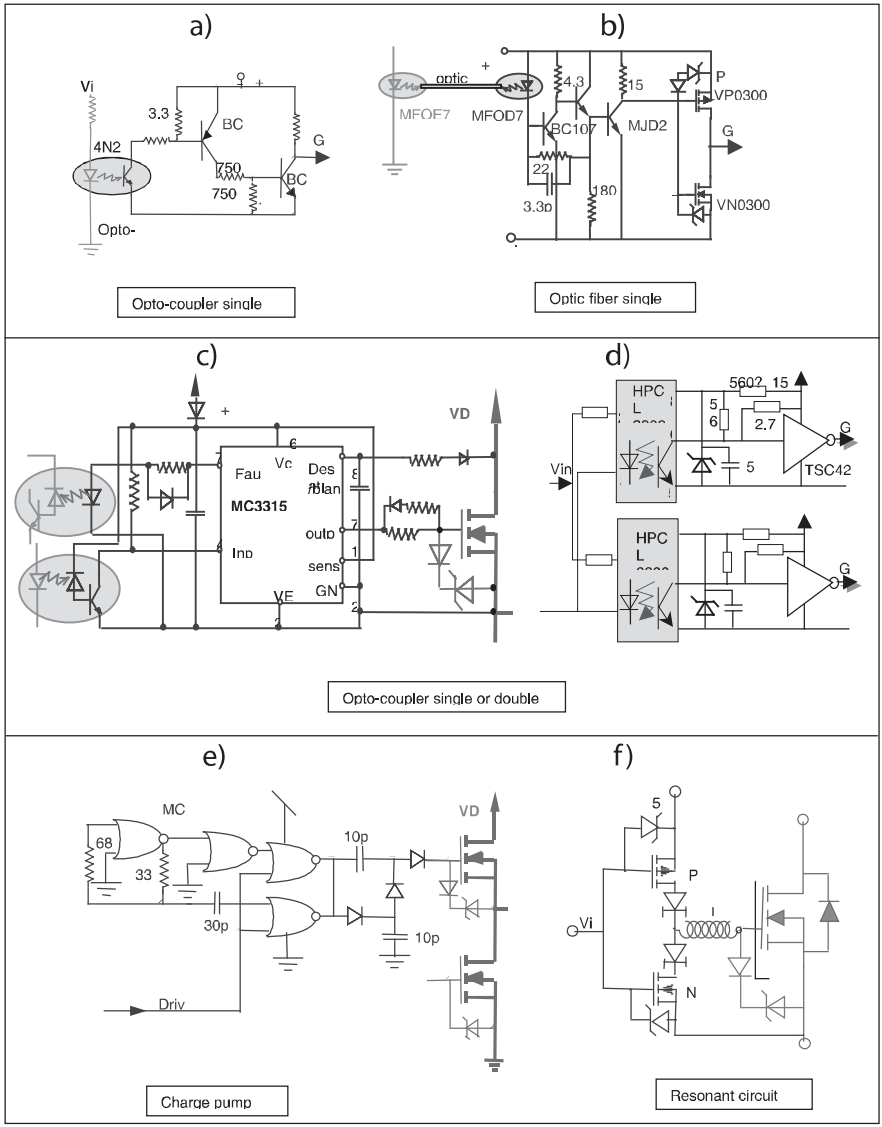


Figure 2.50. *MOSFET and IGBT special drive circuits*

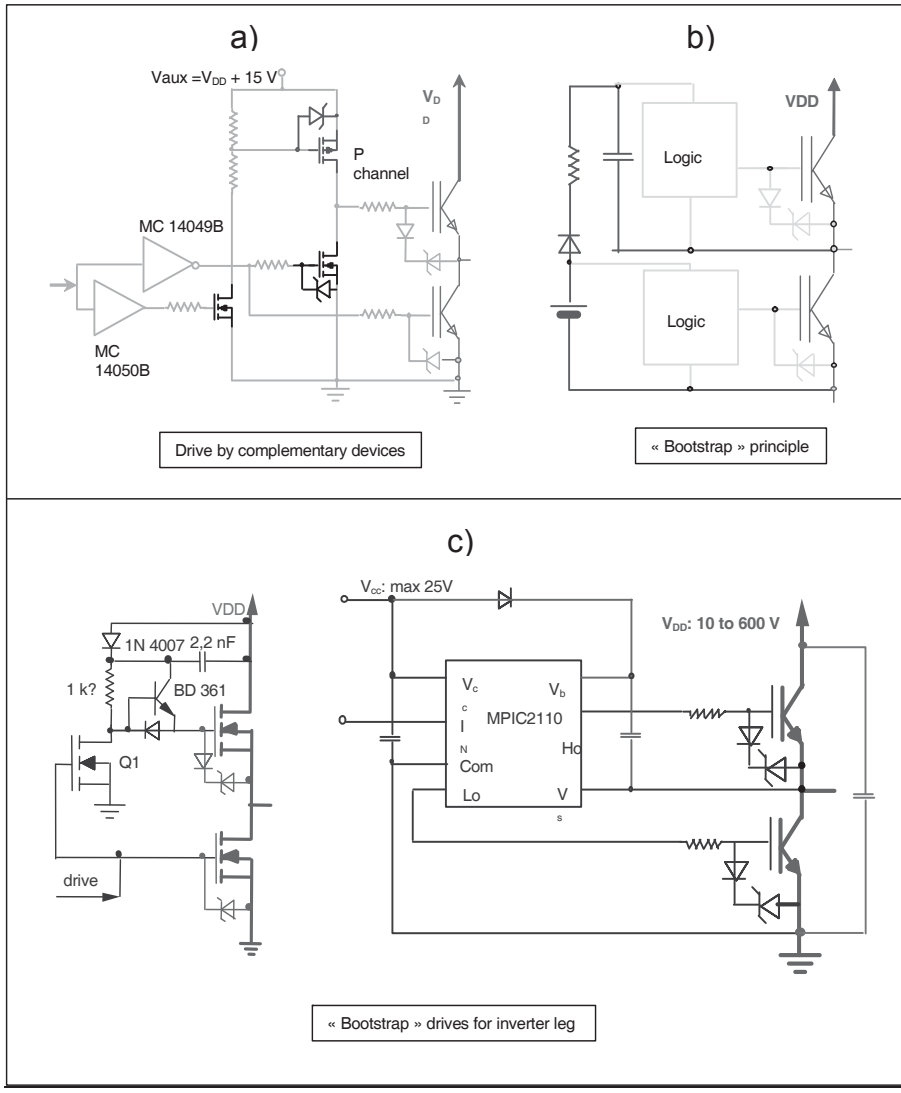


Figure 2.51. *MOSFET and IGBT upper side drive circuits*

2.10.3. *MOSFET and IGBT protections*

2.10.3.1. *Over-current protections*

Current or voltage measurements are needed, for over-current protections (see Figure 2.52). The current transformer is a very simple measurement system, however, due to the volume of the device, it is mainly used for high magnituded currents.

Voltage drop on a resistor is also a very simple idea, but this resistor must have very low resistance to have low losses, and be non inductive to avoid any ringing. This is an expensive resistor, mainly used for very low currents.

A non-dissipative solution is to measure the drain or anode voltage. Over-current on the IGBT means de-saturation and an increase of the anode voltage. A threshold comparator connected between anode-cathode of the IGBT detects this voltage and a switch-off signal can be issued.

For high current circuits, turning off the short circuit current (several thousands of amps) is very difficult, due to the high dI/dt, and overvoltage, LdI/dt. So, the best solution, when a short circuit current is detected, is to decrease V_{GSC} to a value $I_{SC} = G_{fs} \times V_{GK} \approx I(\text{rated})$, with a zener such as $Vz = V_{GSC}$. If the defect is still present after a few micro seconds (5 to 10), the system is switched off with only the rated current.

2.10.3.2. *Overvoltage protection*

The MOS or IGBT “Achille heel” is the gate oxide protection, because, with a thickness of around 100 nm and a rated voltage of 20 V, the device lifetime mainly relies upon the gate oxide stresses. So, it is mandatory to use a fast zener between gate and source or cathode (see Figure 2.52e).

MOSFET or IGBT can sustain accidental avalanches, but the lifetime of these devices is also limited by the avalanche stress. So, an avalanche diode (or a zener) is sometimes used between drain and source, or anode and cathode, to absorb the avalanche energy. The diode must be large enough to support this energy, making it an expensive device. For the same purpose, a small zener could be connected between drain and gate, or anode and gate, to drive the power device on, before the device avalanche. This will absorb the energy, not in avalanche, but in conventional operation. A standard diode must be connected in series to avoid any current running from the gate to the drain in on-state.

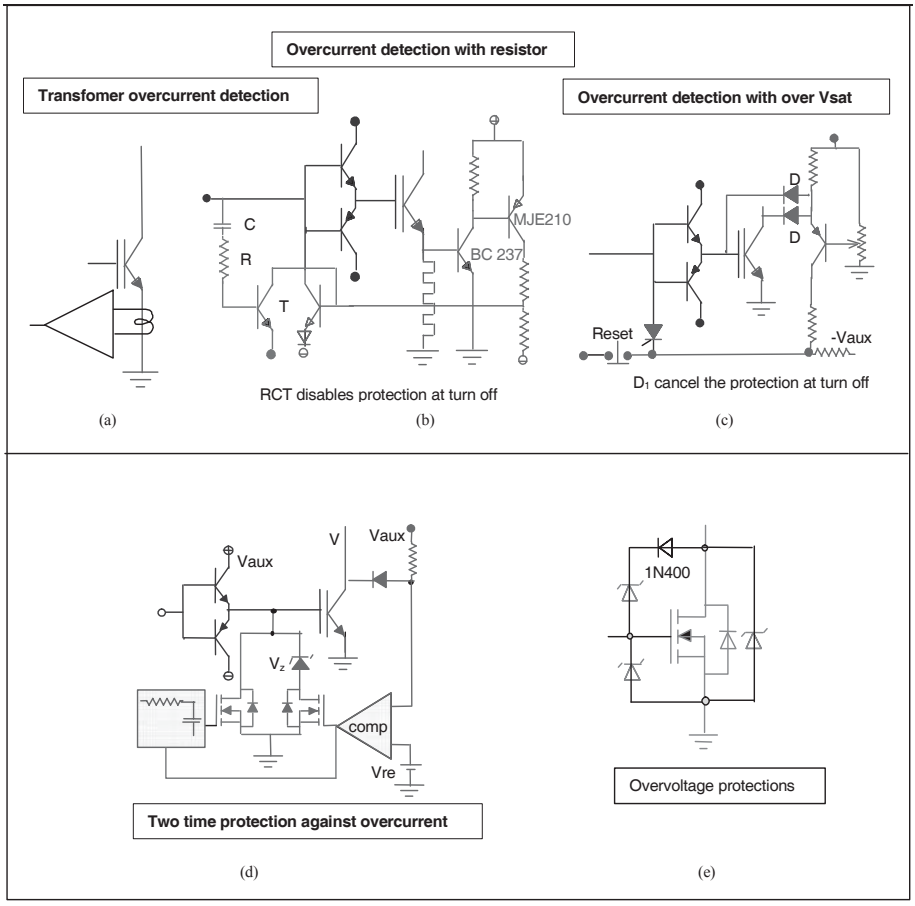


Figure 2.52. *MOSFET and IGBT over-current and overvoltage protection*

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Chapter 3

Series and Parallel Connections of MOS and IGBT

3.1. Introduction

The development of power applications leads to increasing power requests on the electronic switches, used in power converters. These converters are able to flexibly control electrical power actuators, and are more frequently used in industrial applications than in consumer applications. Equipment powers are increasing, while costs for a given switched power are reduced (in pounds per Kilowatt), and the quantities produced are strongly enhanced.

In order to face these new challenges, engineers are focusing on:

– improvement of power components performances, especially on current and voltage ratings, together with speed ratings; and

– combined use of components, in order to increase capacities and the performance of these switches. This is a spontaneous idea, arising from the beginnings of power electronics. It may be applied to components, as it is applied to commutation modules, and whole converters.

This chapter focuses on the association of power components; however, these same methodologies may be used in a more general context.

Chapter written by Daniel CHATROUX , Dominique LAFORE and Jean-Luc SCHANEN.

3.2. Types of associations

Association of components is used in order to increase performances in two ways.

3.2.1. *Increase of power*

This may be achieved by increasing commutated voltages or currents. In practice, increasing commutated power may be achieved by increase of the number of associated components. Three methods for increasing power are:

– *parallel* connection of components, to increase current ratings;
– *series* connection of components, to increase voltage ratings;
– *matrix* connection of components, which is a combination of the two former associations.

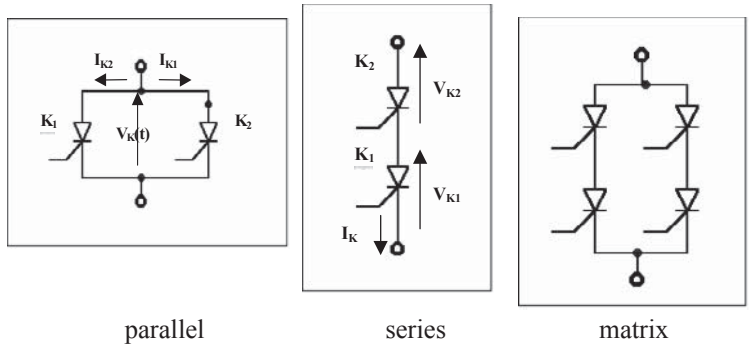


Figure 3.1. *Types of associations.*

These are *homogenous* associations: the spontaneous goal is an effective "sharing" of constraints between the associated components.

In all cases, the challenge for a good design is the effective control of the sharing of constraints between the different associated elements, in order to reach, as an ideal result, an equal distribution of constraints. Nevertheless, associations may be designed in order to simply maintain components inside their own domain of security (safe operating area), rather than to make a strict sharing. Associations may also have very different behaviors when facing overloads during fault operations: this is an important aspect for analysis of the different types of associations.

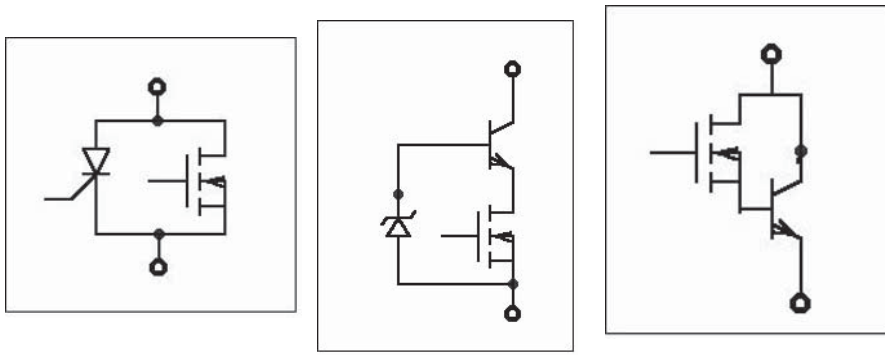
3.2.2. *Increasing performance*

This may be achieved by the association of components that have different characteristics, in order to take advantage of only the strong features of each one. Some cases to be mentioned are:

– parallel connection of a fast component (MOSFET) together with a low saturation voltage component (bipolar);

– series connection of a high voltage rating component, together with a low voltage but very fast component (Cascode design); and

– Darlington connection, which may be homogenous, like bipolar-bipolar, or heterogenous, for instance MOS-bipolar. This kind of association allows a self-supply of the drive current from the power.



Parallel Cascode Darlington

Figure 3.2. *Heterogenous associations of components*

These are *heterogenous* associations, where each element plays a specific role, corresponding to its strong feature.

In this chapter, we will study only homogenous associations.

3.3. The study of associations: operation and parameter influence on imbalances in series and parallel

3.3.1. *Analysis and characteristics for the study of associations*

The study of component associations has led to the knowledge of specific variables (currents and voltages), as a function of time, for each element of this

association. In the field of power electronics, commutation cells are analyzed using two aspects:

– static operation, including two states: opened or closed (conducting); and

– dynamic operation, which occurs during commutation phases: closing and opening.

These studies require an internal approach, similar to that of a single component, taking into account different types of external conditions (imposed on the switch by its environment). For a simple approach, a presentation is made of the association of two switches, but conclusions may be applied to several elements [GUI 95].

3.3.1.1. *Parallel association*

Two basic relations may be written for parallel associations. The first relates to voltage:

$$V_{K1}(t)=V_{K2}(t)=V_K(t)$$

and ensures that the lowest voltage is imposed on the association.

The second equation relates to current sharing inside the association:

$$I_{K1}(t)+I_{K2}(t)=I_K(t)$$

Current sharing depends only on components and is the main study parameter for parallel connection.

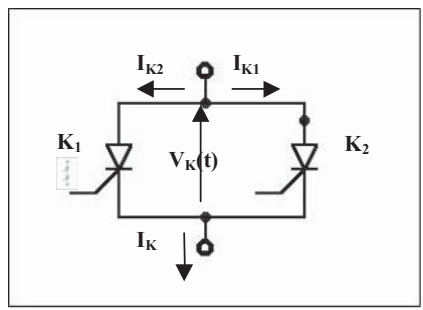


Figure 3.3. *Electrical laws for parallel association*

3.3.1.2. *Series association*

Series connection is dual in contrast to the parallel connection, this means the basic relations are also dual.

The first relates to voltage sharing inside the association:

$$V_{K1}(t)+V_{K2}(t)=V_K(t)$$

Voltage sharing depends only on the components.

The second relation involves currents:

$$I_{K1}(t)=I_{K2}(t)=I_K(t)$$

This means the lowest current is imposed on the association. Voltage sharing is the main study parameter for series connection.

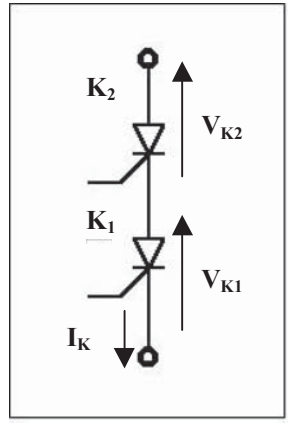


Figure 3.4. *Electrical laws for series association*

3.3.2. *Static operation*

There are two static states:

– during opened state, IK(t)=0 is defined by the switch, and VK(t)=Vext(t) is defined by the outside circuit; and

– during closed state, VK(t)=0 is defined by the switch, and IK(t)=Iext(t) is defined by the outside circuit.

3.3.2.1. *Parallel connection*

For this association, only the closed state must be analyzed, while, during open state, there is no mismatch of voltages by principle, and no mismatch of current because the current is zero.

The static characteristic of each component on closed state I(V), and the basic relationships, define the sharing of current between the two components, as is clearly depicted in Figure 3.5. We can see that the component with better (K_1) takes more current. In other words, the stronger component helps the weaker component.

Using a linear model like $V_K=V_0+RI_K$, the operating point of the association is defined by:

$$V_K(R_1+R_2)=(V_{01}R_2+V_{02}R_1)+R_1R_2I_K$$

The current imbalance is due to dispersions of static performances of components. This generally leads to the requirement of component selection, in order to limit dispersal of voltages at the current rating. The choice of components inside a single batch is a positive point in order to reach a better balance.

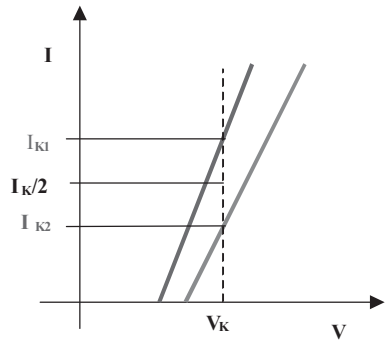


Figure 3.5. *Effect of different static characteristics on voltage sharing in a series association*

In order to take into account these unbalances, it is generally well suited to apply a reduction coefficient on the usable current rating, let us say a “derating”, which depends on the number of components connected in parallel.

3.3.2.2. *Series connection*

For this association, only the open state must be analyzed. As a matter of fact, at zero voltage, there is no mismatch of current by principle, and no mismatch of voltage.

The static characteristic on open state I(V) of each component defines the sharing of voltage between the two components, as seen in Figure 3.6. Here we can see the component with better voltage strength (K_1) takes more voltage; in other words, helping the weaker component.

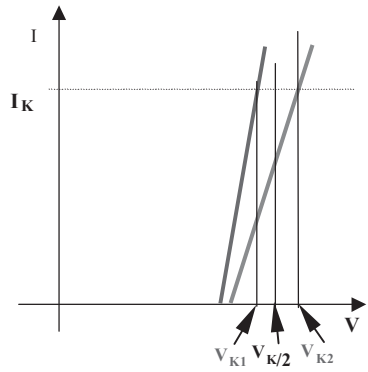


Figure 3.6. *Series connection*

Voltage imbalances in the open state are due to the dispersion of the characteristics of the components. It should be noted that the imbalance of static voltage occurs mainly at the start of the converter. This condition usually does not occur during operation, due to long time constants governing the passage of transient dynamic imbalance to the static imbalance. Figure 3.7 below shows this time constant is greater than 20 ms. In normal operation, this leads to a negligible imbalance of static voltage, of over a few hundred hertz, for a series connection.

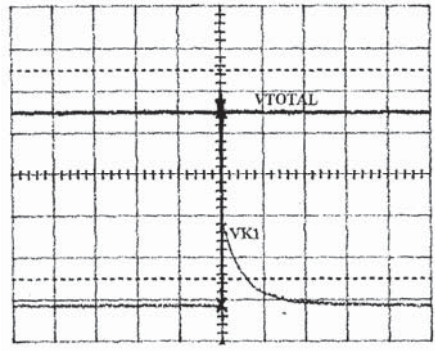


Figure 3.7. *Time constant from dynamic imbalance to static imbalance, for a large leakage current MOS, series connected with a low leakage current MOS. V: 100 V/div, t: 20 ms/div*

The classic solution achieves this balance with resistances connected in parallel on each component, reducing or eliminating this imbalance of voltages. An alternative solution is to use voltage limiters in order to maintain individual voltages within the safe operating area. In this case, balance is not achieved, but imbalance is limited in such a way as to ensure each component remains in its own safe area. We should note that most of the switches and diodes used in power electronics are able to support an avalanche with a low current, and therefore assure themselves this clamping function safely.

3.3.3. *Dynamic operation: commutation*

During dynamic operation phases, two main parameters drive the current imbalance (respectively voltages) in parallel connections (respectively series connections):

– on the one hand, delay time; and

– on the other hand, commutation speed. This speed is current speed (respectively voltage speed) for parallel connection (respectively series connection); while voltage (respectively current) is the same.

These two parameters are defined by basic relationships during dynamic phases. Commutation is analyzed in classic conditions of an elementary “hard” commutation cell.

3.3.3.1. *Closing process*

The initial conditions, applied on the switch before closing, are:

– a voltage defined by the external circuit (E);

– a zero current, while the switch is still opened.

During the closing process, while the switch is able to manage its own current, voltage is still applied on the switch, as soon as the diode of the cell is closed. Opening of the diode makes a change of mode: external current is then limited and voltage depends on the cell: this is the current external mode.

3.3.3.1.1. Influence of the delay time difference

For series, parallel and matrix connections, components must commutate synchronously, in order to limit imbalance of the electric parameters. There are two possible causes of delay between commutation orders. One is due to components (dispersion of characteristics), the other is external from components (dispersion of commutation orders delivered by drive circuits). It is assumed the two switches have the same speed, dI_K/dt, and a lack of synchronization, Δton.

Parallel connection

Lack of synchronization Δton makes an advanced overload on the switch, and an underload on its delayed partner. Overload is given by the relation:

$$2\Delta Ion=\Delta ton(dI/dt)$$

This phase is over at switch-off of the diode.

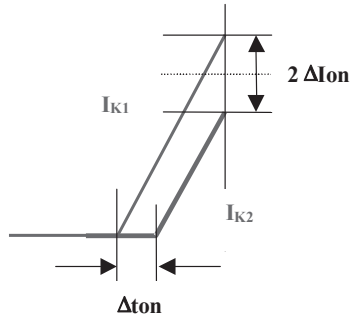


Figure 3.8. *Effect of a delay at turn on for the same current commutation speed in a parallel association*

Series connection

A voltage balance is assumed at initial time. The lack of synchronization Δton makes an overvoltage, which occurs before the current is able to increase.

Indeed, voltage of the switch in advance decreases; and in order to comply with voltage law, the voltage of the delayed switch increases. Current, except for capacitive current, will be able to increase when the two switches are closed. The overload value is given by the relation:

$$2\Delta Von=\Delta ton(dV/dt)$$

Speed of dV/dt depends on the internal capacitances of the components.

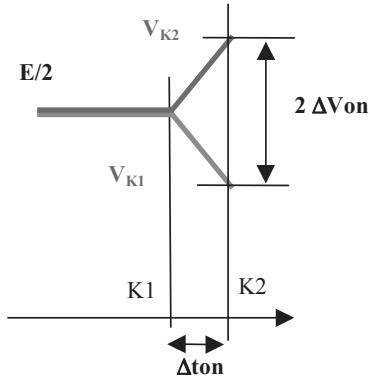


Figure 3.9. *Effect of a delay at turn on for the same voltage commutation speed in a series association*

MOS voltage depends on the delay Δt of the control (from 20 to 80 ns). The two other components are synchronous.

Figure 3.10 depicts the series connection of a three MOSFET switch-on where the scales are 100 V/div, 100 ns/div.

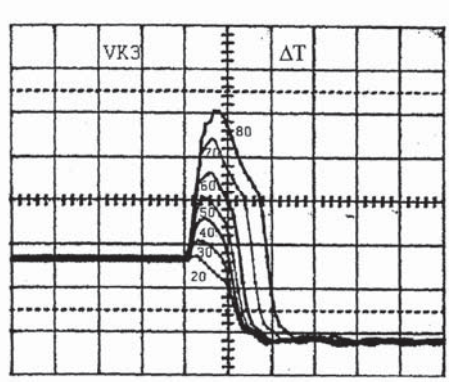


Figure 3.10. *Series connection of three MOSFETS – turn on*

3.3.3.1.2. Influence of speed dispersion

Dispersion between the characteristics of the components leads to differences between speeds current evolution and transient voltage. This leads to imbalances in constraint sharing. There is assumed to be a perfect synchronization and an initial sharing of constraints.

Parallel connection

As each component is free during current increase, it is able to define its own speed.

Difference of speed leads to an overload on the fastest switch and an underload on its slower partner. The overload value is given by the relation:

$$2\Delta Ion=Iext(\alpha_1-\alpha_2)/(\alpha_1+\alpha_2)$$

where $\alpha 1$ and $\alpha 2$ are current speeds of K_1 and K_2

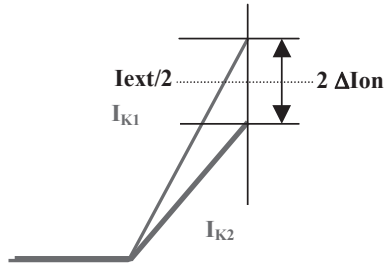


Figure 3.11. *Effect of a mismatch in current commutation speed at turn on in a parallel association*

Series connection

Here an initial balance of voltages is assumed. While this is a decreasing phase, speed difference between the two components does not lead to overload, however commutation losses will not be the same.

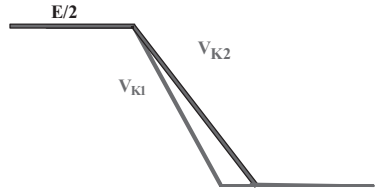


Figure 3.12. *Effect of a mismatch in voltage commutation speed at turn on in a series association*

3.3.3.2. *Turn off*

This is a dual commutation study which enables us to foresee results, by applying the rules of duality to former results. The initial conditions applied to the switch, before opening, are defined by the cell:

– a current applied by the external circuit (Iext);

– a zero voltage, since it is still not opened.

During opening, as current is imposed, the switch manages its own voltage as long as the diode of the cell remains opened: this is an external current mode. Closing of the diode makes a change of mode, thus external voltage is limited and the current depends on the cell: this is external voltage mode.

3.3.3.2.1. Influence of the difference in the delay time

The following assumes the two switches have the same speed, dV_K/dt, and a lack of synchronization Δtoff.

Series connection

Lack of synchronization in Δtoff leads to a voltage excess on the advanced switch, and an undervoltage on its associated partner. Value of the overload is given by the relation:

$$2\Delta Voff=\Delta toff(dV/dt)$$

This phase ends at switch-on of the diode.

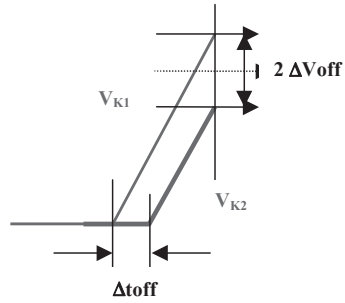


Figure 3.13. *Effect of a delay at turn off for the same voltage commutation speed in a series association*

Parallel connection

Here there is assumed to be an initial current balance. Lack of synchronization in Δtoff leads to an excess current before the voltage is able to increase. Indeed, the current inside the switch decreases in advance and, in order to respect nodes law, the current in the delayed switch increases. Voltage will be able to increase only when the two switches will be are opened. The value of the overload is given by the relation:

$$2\Delta Ioff=\Delta toff(dI_{K1}/dt)$$

Speed dI_{K1}/dt depends on the component and also on its command**.**

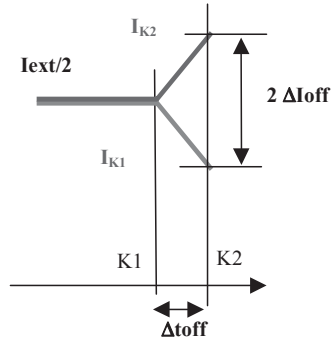


Figure 3.14. *Effect of a delay at turn off for same current commutation speed in a parallel association*

As shown below in Figure 3.15, MOS voltage depends on the advance Δt of its drive (from 15 to 40 ns); two other components are synchronous. Scales: 100 V/div, 2 A/div, 100 ns/div.

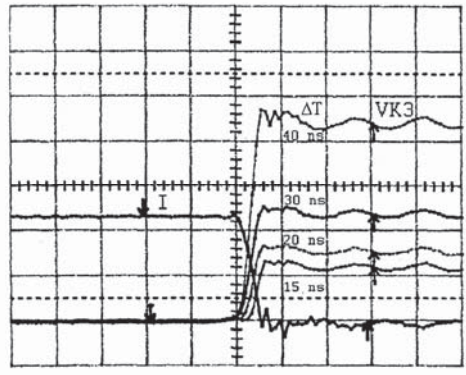


Figure 3.15. *Series connection of three MOSFETs – turn off (scale: 100 V/div, 2 A/div, 100 ns/div)*

3.3.3.2.2. Influence of the difference of speeds

Dispersion of component characteristics leads to varying speeds of current and voltage evolution during transient phases. This leads to imbalances in shared constraints. We assume synchronization is perfect, and the initial conditions are balanced.

Series connection

As each component is free during voltage increase, it defines its own speed.

Difference in increasing speeds leads to an overload on the fastest switch, and an underload on its slower partner. The overload value is given by the relation:

$$2\Delta Voff=E(\alpha_1-\alpha_2)/(\alpha_1+\alpha_2)$$

where $\alpha 1$ and $\alpha 2$ are voltage speeds of K_1 and K_2.

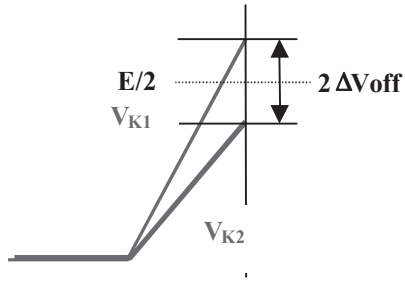


Figure 3.16. *Effect of a mismatch in voltage commutation speed at turn off in a series association.*

Parallel connection

Here an initial state of current sharing is assumed. Difference of speed between the two components does not lead to overloads, since this is a decreasing phase; but commutation losses are not the same.

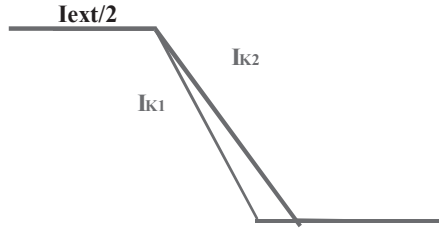


Figure 3.17. *Effect of a mismatch in current commutation speed at turn off in a parallel association*

3.3.3.3. *Synthesis*

	Parallel	Series
Turn on	– the anticipated switch is overloaded in current, helping the delayed one. – the voltage speed at turn on is the one of the slowest switch (algebraic value); – the fastest switch is overloaded in current, and it helps the slowest	– the anticipated switch is helped, overloading the other switch in voltage – current speed at turn on is the one of the slowest switch –the fastest switch (absolute value) is helped, overloading the other switch in voltage.
Turn off	– the anticipated switch is helped, overloading the other switch in current – voltage speed at turn off is the one of the slowest switch – the fastest switch (absolute value) is helped, overloading the other switch in current.	– the anticipated switch is overloaded in voltage, helping the delayed one. – the current speed at turn off is the one of the slowest switch (algebraic value); – the fastest switch is overloaded in voltage, and it helps the slowest

Table 3.1. *Summary of dynamic unbalance: delay and mismatch in commutation speed*

The following chart shows a more synthetic representation.

		Parallel		**Series**	
		K1	**K2**	**K1**	**K2**
Closing (opening)	**Synchronized**	Advance	Delay	Advance	Delay
	Current	Overload (Helped)	Helped (Overload)	Zero (+ capacitive)	
	Voltage	Vext (-V inductive)		Helped (Overload)	Overload (Helped)
	Speed	Fast	Slow	Fast	Slow
	Current	Overload (Helped)	Helped (Overload)	One of the slowest	
	Voltage	One of the slowest		Helped (Overload)	Overload (Helped)

Table 3.2. *Synthetic view for effects of delays and mismatch in commutation speed*

Duality may be seen from the points of view of:

– opening and closing;

– series and parallel;

– advance and delay;

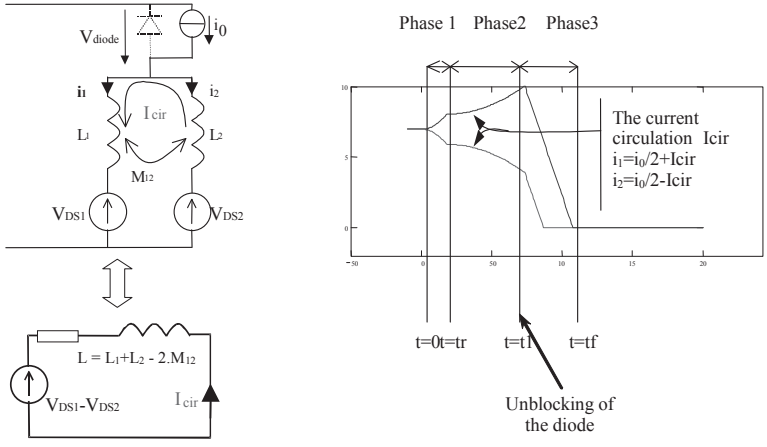
– fast and slow.

Advance and fastness have the same effect, as, by duality, delay and slowness have the same effect. Thus, results are the same for the advanced or the fast components, and, by duality, for delayed or slow components.

3.3.4. *Transient operation [JEA 01]*

Inside a parallel association of components, during a commutation, occur phenomena which lead to transient imbalances, due to causes other than different commutation speeds of current. Indeed, during evolution of voltages across semiconductors, if they are different, an internal current inside the association is generated, due to the difference of voltages between the semiconductors.

During opening, this phenomenon is strong because the voltage commutation occurs *before* the current commutation. A loop current is added to the power current defined by the load [JEA 01]. Even before the beginning of the current commutation, this transient voltage leads to an imbalance, (see Figure 3.18).



(a) : Equivalent schematic for a loop current

(b) : Theoretical waveforms for currents i1 and i2 at opening.

Figure 3.18. *Loop current during opening*

Despite what is seen above in the equivalent schematic, this current is not limited by the "inter-switches" wiring inductance, because it compensates for the difference of voltages. As a matter of fact, with no wiring inductance, there is no voltage difference, and thus no loop current.

This is supported by Figure 3.19, which shows the evolution of the loop current amplitude at opening, as a function of "inter-switches" inductance.

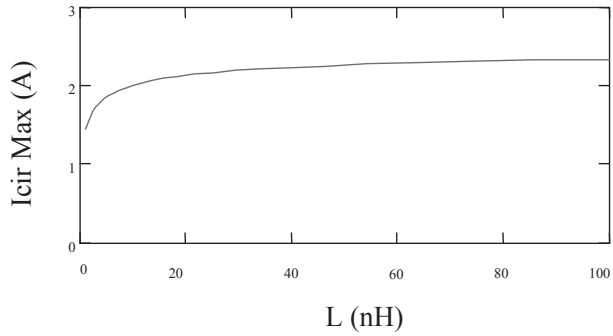


Figure 3.19. *Evolution of maximum value of loop current as a function of L , with r_{G1}=9.9Ω, r_{G2}=10.1Ω, Crss1=130pF and Crss2=140pF*

During closing, current evolution takes place before voltage evolution; thus the above mentioned phenomenon has less importance. But now, after a commutation which makes a given imbalance, a new imbalance occurs, corresponding to a static operation (closed/opened). This transient corresponds to a transient of the imbalance.

In the case of a parallel connection, this transient takes place after closing; and depends on the loop impedance between the parallel connected components, mainly inductive and resistive. Depending on wiring, the time constant is in the range of a few microseconds.

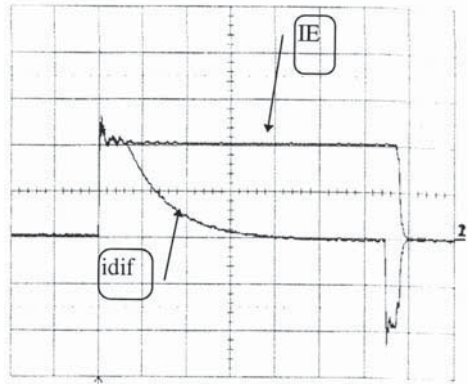


Figure 3.20. *Parallel connection of two IGBTs, with a large delay between drives. IE is the global current, Idif is the differential current IK1-IK2. Scales are: 10 A/div, 2 µs/div*

In the figure above we can notice full imbalance in favor of K1 during closing, and full imbalance in favor of K2 during opening.

3.3.5. *Technological parameters that influence imbalances*

A lot of important parameters influence the sharing constraints inside associations. These are mentioned according to their origins.

3.3.5.1. *Component [LAF 00]*

3.3.5.1.1. Internal parameters [LET 92]

Internal parameters are: V0, drive voltage of the grid circuit; R_G, resistance of the grid circuit; Vth, threshold voltage; tranconductance and input and output capacitances. As formerly mentioned, delays and commutation speeds hold great importance. Delays are mainly managed by charging the grid circuit up to the threshold voltage Vth. Thus, internal parameters are:

– non-linear value of input capacitance (Ciss);

– value of internal resistance of the component;

– value of the threshold voltage Vth (very sensitive to temperature).

3.3.5.1.2. About speeds

– During closing, current speed depends on transconductance and on the evolution speed of the grid to source voltage.

– During opening, voltage speed depends on the internal capacitances (Cgd – Miller capacitor-, Cds for MOSFET), and on external currents, power currents as control currents.

3.3.5.1.3. Temperature [RAE 96]

Most component parameters have a sensitivity to junction temperature. This creates a strong potential sensitivity to junction temperature imbalances of the components involved. In the case of a parallel connection, a cooler treatment is required in order to decrease the temperature differences between components: to obtain a strong coupling, the chips must be located on the same heatsink, within a short distance from each other. For a series connection, a single heat sink is generally not possible, due to the required electrical insulations, and due to parasitic capacitances: cooling technology will be adapted accordingly (for example oil may be used).

3.3.5.2. *Drive circuit*

General features are included to ensure as great a synchronization as possible, and the correct balancing of the drive currents. Options vary depending on the type of association, because the reference order of each element of the association is not the same for a series connection, although it is the same for a parallel connection. Inductance of the drive circuit is another dispersion factor causing imbalances.

3.3.5.3. *Power circuit*

The physical design of different associations of components leads to wiring between power connections (collectors, emitters, drains, sources, anodes, cathodes). Their impedances (inductances, capacitances, static and dynamic resistances) are the parameters influencing the internal balance. Once more, their relative importance depends on the kind of association, and on the operating phases.

3.4. Solutions for design

3.4.1. *Parallel association*

3.4.1.1. *Selection criteria for constitutive components selection [LAU 98]*

As we have seen, component association is highly dependent on the specific characteristics of each component, and more specifically on the dispersion of those characteristics. Here, we must distinguish MOS from IGBT. The former are only resistive (RDSon), with a positive temperature coefficient, which allows for self-balancing. In some areas, the latter have a negative apparent resistance temperature coefficient, so situations of conflict may occur, and a selection procedure may be required to limit internal imbalances.

The designer has two options:

– Selection of components; this prioritizes components from the same production batch. A further step is to associate components whose characteristics are nearby. The classic test, generally sufficient, sorts by classes of VCE voltage drops, at the current rating. As an indication, diodes should be within a VF(IN) characteristic in the range of 0.1 V, to reduce the static imbalance down to 15%. For IGBT, 0.15 V provides the same result. Figure 3.21 is an example of this selection at 25°C and shows its influence on the distribution of currents. An increase of temperature reduced the imbalance.

– "Derating" of the current capacity; depends on the number of elements involved. Usually, manufacturers provide some guidelines on this point.

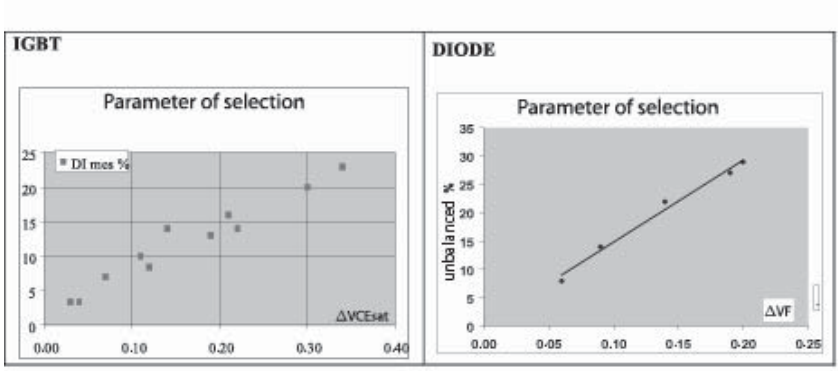


Figure 3.21. *Effect of selection on current imbalance*

3.4.1.2. *Grid drive circuit*

3.4.1.2.1. Grid circuit

The electric schematic for the grid command of one component is synthesized on Figure 3.22. The calculation is simple (second order). L_G is the parasitic wiring inductance.

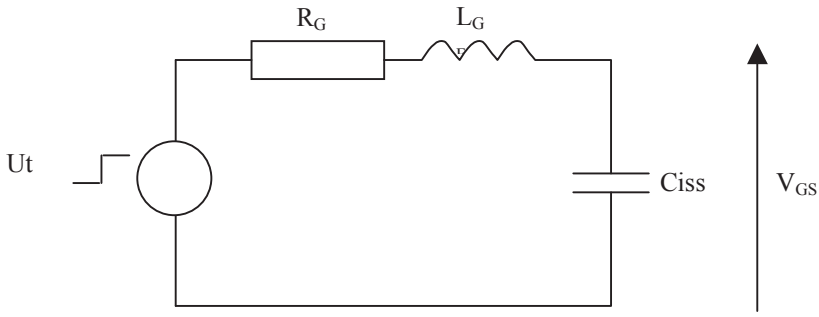


Figure 3.22. *Equivalent circuit for grid charge*

During switch-on, Ciss must be charged up to the threshold voltage, Vth. The circuit elements are:

– Ut, is a positive step; and

– Ciss, which may be approximated by Cgs, since Cgd is very low (large drain-source voltage).

During switch-off, Ciss must be discharged down to a voltage level close to the threshold voltage, Vth+Idrain/g (where g is transconductance). Here:

– Ut, is a negative step; and

– Ciss = Cgs + Cgd

Calculation of this second order circuit is simple, and determines the delay. The important parameters for charge and discharge are total grid resistance, and parasitic wiring inductance.

3.4.1.2.2. Influence of delay inside an association

For a parallel connection, with a unique command, a circuit may be synthesized as shown in Figure 3.23.

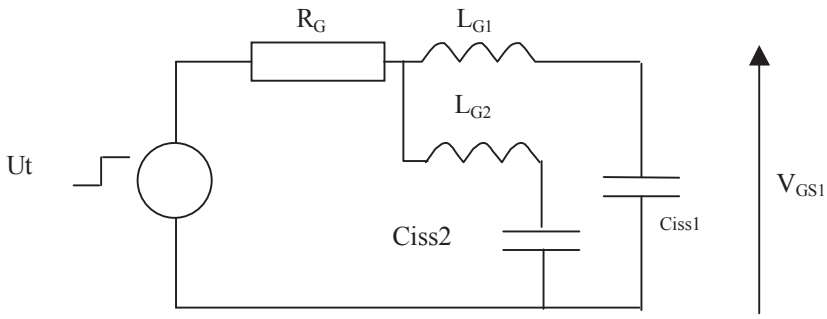


Figure 3.23. *Schematic of grid circuit for a parallel connection*

Difference of delays, the parameter which induces imbalances, depends, for a given Rg, on the difference ΔLg = Lg1-Lg2 between the two wiring inductances of the different grid circuits.

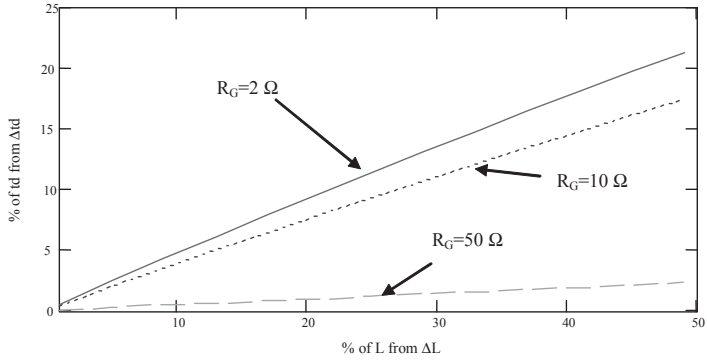


Figure 3.24. *Additional delay time due to a difference of grid inductance*

Figure 3.24 shows an increase of time when the grid inductance increases, for a given value of the grid resistance [JEAN 01]. Here, numerical calculations were done for various values of R_G (2 Ω, 10 Ω, 50 Ω), while L_G equals 50 nH as a basic value, and *Ciss* equals 1nF.

For large values of R_G (50 Ω), the variation of td is very small (as a relative value). This is about two times smaller than the value of L_G (a 20% deviation of L_G makes a 10% deviation of *td*).

3.4.1.2.3. Speed evaluation

– Closing: during the operation at threshold voltage, as a first order, current speed is proportional to grid current, i_{gth}. If the second order circuit is sufficiently damped (large R_G), i_{gth} is not influenced by the inductance. Thus, speed depends only on R_G. For low grid resistances, V_{th} is reached with a i_{gth} current defined by resonance. Then, speed depends also on the L_G value.

– Opening: during the operation at voltage level (V_{th}+Idrain/g), as a first order, voltage speed is proportional to grid current. Thus, speed depends mainly on R_G. Drain current also plays a role, via the drain source capacitance charge.

As a conclusion, important parameters for voltage speed commutation are (with decreasing importance):

– R_G and Cgd; then

– Idrain and Cds.

3.4.1.2.4. Technological solutions

A classic design, for parallel drives, includes a single command, making an initial synchronizm, associated with individual and identical grid resistances Rgi, for a better sharing of grid current. Usually, a common resistance R_G is added to control the global speed (Figure 3.25).

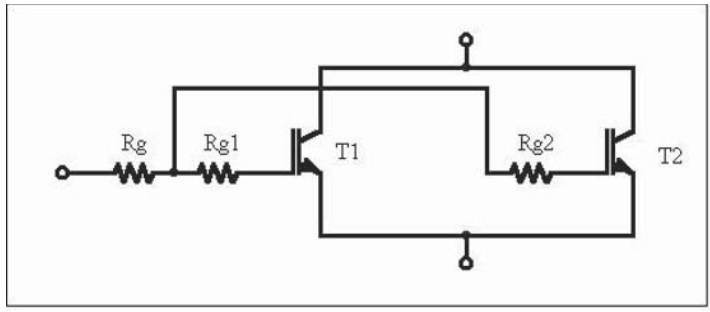


Figure 3.25. *Use of balance resistances Rgi (Rg1=Rg2)*

Additionally, these resistors prevent the high-frequency oscillation of paralleled components (the circuit consists of the two components, their internal parasitic capacitances and parasitic wiring inductances between grids, between drains and between sources; this is a high frequency oscillator, which must be strongly damped).

These resistors can also reduce the speed of commutation of the components, for the purpose of electromagnetic compatibility, or for control of switch-on speed at a tolerable level for the associated diode (powerful IGBT modules for example).

With regard to wiring inductors, remarks of the preceding paragraphs led to the use of low inductive wiring, and in particular the use of equal inductors.

3.4.1.2.5. Active balancing [HOF 99]

With very high power modules, with high costs, individual commands may be implemented for each module. In this case, a design may be implemented, with a command for each element, including sensing imbalance, in order to actively balance the currents (Figure 3.26).

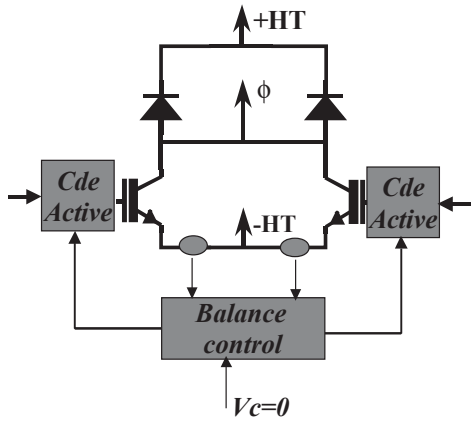


Figure 3.26. *Active control of current in two paralleled cells*

3.4.1.3. *Influence of wiring inductances on the power side*

3.4.1.3.1. Introduction

Connections between associated components are necessarily numerous, and must be properly designed in order to get the appropriate distribution of current between the elements. Connections show complex impedances (inductance, resistance and coupling).

Nowadays, power wiring is made using the busbar technology, which greatly reduces inductance. However, only a good design ensures the sharing of currents.

The main layout rules are as follows:

– for one switch, connections must be done on opposite faces. Such a design takes into account resistive and inductive issues, but not coupling issues;

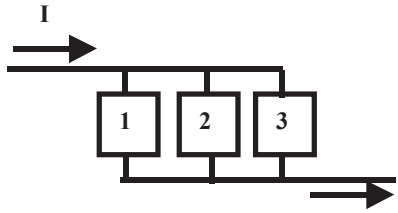


Figure 3.27. *Ladder disposition for a better current balance*

– there must be a minimal connection length in order to limit wiring inductances, which make overvoltages at switch-off. This requires a busbar between cells and decoupling capacitors;

Figure 3.28. *Use of busbar topology to reduce interconnection inductance (links high side switch H, low side switch L and DC bus capacitor)*

– individual connections with an important resistive influence must be well designed, with soldering or with screws, especially for high current rating modules.

3.4.1.3.2. Detailed analysis of the influence of wiring [JEA 01], [JEA 99]

In order to better understand the effects of coupling, a more accurate analysis of current sharing between several parallel components must include not only inductances and resistances, but also coupling between wiring inductances.

Figure 3.29 shows the model used in the case of paralleling two switches.

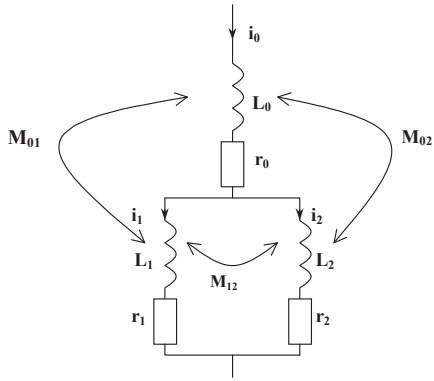


Figure 3.29. *Wiring model for evaluation of current imbalance between two parallel MOSFETs*

Detailed theoretical studies show [JEA 00] that the ratio between branch current and global current is:

$$\frac{i_1}{i_0} = \frac{r_2 + (L_2 + M_{02} - M_{01} - M_{12}) \cdot p}{r_1 + r_2 + (L_1 + L_2 - 2 \cdot M_{12}) \cdot p}$$

At low frequencies, the obvious condition of balance is: $r_1 = r_2$.

At high frequencies, the condition of balance is: $\frac{L_1 - L_2}{2} = M_{02} - M_{01}$.

The solutions are to comply with the former equation, or obtain a negative $|M_{12}|$ value as large as possible. The most favorable case is: $M_{12} = -\sqrt{L_1 \times L_2}$.

This shows that a symmetric structure, which is not possible to achieve in some cases [CLA 96], is not required in order to get identical currents i_1 and i_2. Only compliance with the above mentioned conditions is required:

– Switch-on: with up-to-date systems of components and wiring, in most cases, the drivable component defines its the switch-on speed, whilst parasitic inductances play a second order role. However, for components that do not control their speed (like diodes, or thyristors, etc.), current sharing is directly dependent on wiring inductances, and on their coupling.

– Switch-off: section 3.6 mentioned additional possible imbalances of the current, due to the differences of voltage commutation speeds (loop currents). A design rule is – in addition to obtaining equal voltage speeds – to try to design in order to get the component with the largest dV/dt to be the most delayed. This is illustrated in Figure 3.30.

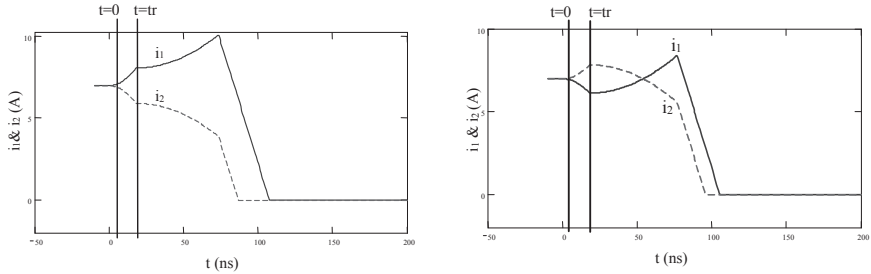


Figure 3.30. *Opening*

3.4.1.4. *Design examples*

Figure 3.31 shows the design of a 400 A, 600 V module by paralleling the height of plastic packages, standard TO 247, for each commutation function, on SMI support. Components are selected according to proposed criteria [LAF 01].

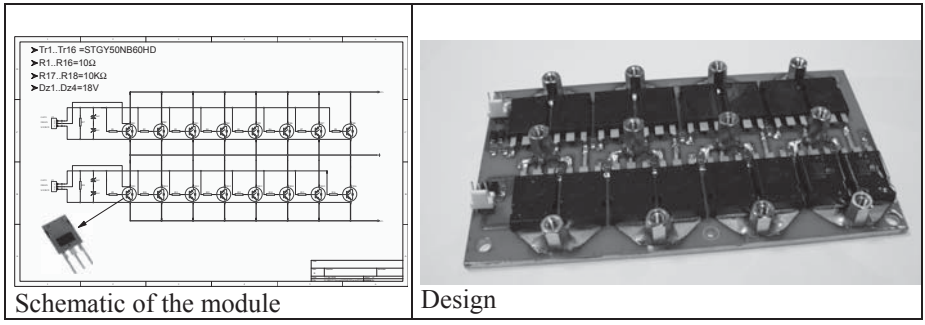


Figure 3.31. *400 A module by paralleling height components*

3.4.2. *Series associations [LAU 00b]*

On one hand, semiconductors are more sensitive to voltage overloads than to current overloads. On the other hand, series connection makes voltage imbalances. While voltage evolution speed is much faster than current evolution speed (10 kV/μs compared to 1 kA/μs), the importance of a delay on one component compared to another is much more important in series than in the case of parallel connection.

3.4.2.1. *Selection of components*

The semiconductor parameters that influence delays and commutation speeds were previously mentioned for parallel connection, and remain the same.

Two solutions available are:

– selection of components (same batch, same wafer); and

– choice of robust components against avalanche.

3.4.2.2. *Grid drive circuit*

In series associations of components, parallel or matrix, components must commutate in the most synchronous way, in order to reduce differences in the sharing of electric constraints. There are two origins for the delays possible between commutations: one is from dispersion of the internal characteristics of components; the other is from external causes, including dispersion of orders of commutation delivered by the drive circuits.

For series connection of switches, the most frequently used drives are:

– cascade commands;

– optical commands;

– commands by transformers.

3.4.2.2.1. Cascade commands

These commands use the commutation of the lower switch in order to generate the commutation of the superior switch, by means of the capacitor. A delay occurs between commutations of the different switches of the series connection, and thus a lack of synchronization by principle. This has to be taken into account for the voltage definition of switches. In practice, cascade commands are usually used for series connection of switches, but for no more than three or five elements.

3.4.2.2.2. Optical commands

These commands only transmit the drive signal and require an additional source of energy. For low switching frequencies, this energy may be obtained from the power connections of the switches to be driven. A very important feature is the great sensitivity of optical receivers to perturbations. This is well known for photo-couplers; this is also the case for optic fibers. The optic fiber itself is not sensitive to electromagnetic perturbations, but the optical receiver at the end of the fiber is extremely sensitive. For a series connection operating with large dV/dt, the optical receiver and its proximity command must be implemented inside a local faraday cage, connected to the voltage of the switch to be driven.

For example, very high voltage converters, connected to the grid, and operating at relatively low frequencies, are designed this way. In this case, the association of the optic with the self-supply of drive boards is a good technological solution.

3.4.2.2.3. Transformers

The strong advantage of transformers is the ability to deliver together the drive order and the required energy. We must pay attention, on one hand, to the strength on the voltage insulation which supports the dV/dt and, on the other hand, to the parasitic capacitance of the transformer.

For fast high voltage applications, a classic drive is made of a pulse transformer, whose primary is made of a high voltage cable passing through a ferrite tore (which is indeed the magnetic core), and whose secondary is made of a few turns of wire, with low voltage insulation, wound around the core. The primary of this transformer is thus made of only one turn. The ferrite core must be connected to the switch to be driven. This kind of transformer has very good performances, and is well suited for industrial applications. Drive pulses transmitted by the transformer are used directly, or memorized, according to the drive requested by the switch.

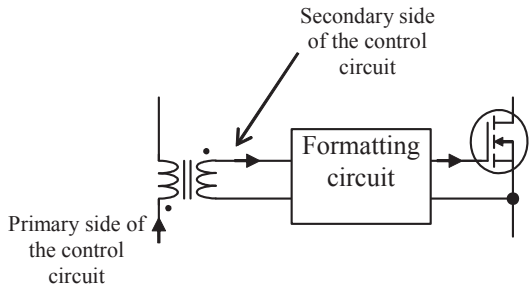


Figure 3.32. *Drive by pulse transformer, which ensures the galvanic insulation*

Synchronization between stages may be achieved by series connection of the primaries of these transformers, which in this design have the same current flow, supplied by the drive circuit. This way, all the stages of the series connection have the same current.

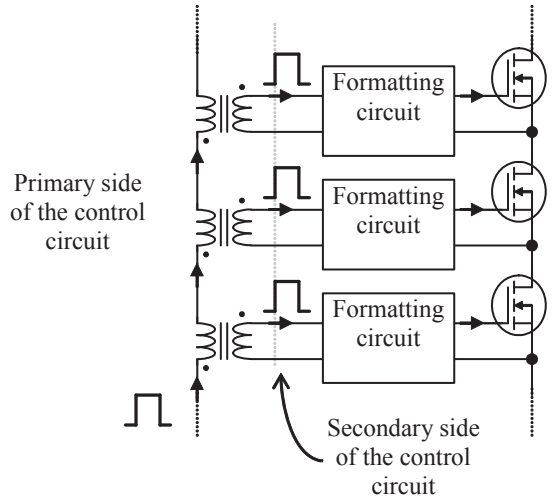


Figure 3.33. *Synchronized command of stages by series connection of the drive circuit primaries*

The ferrite core does not need insulation, but requires a connection to the voltage of each stage. When commutation dV/dt occurs, capacitive currents between commutating components and the primary cable must not flow through the proximity drives of the components, but instead must flow throughout this voltage connection.

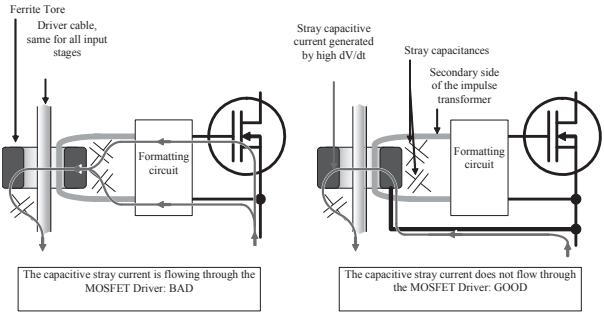


Figure 3.34. *Voltage connection of the core, which allows the circulation of parasitic capacitive currents during dV/dt*

The central hole of the core must be large enough to allow sufficient space for a drive cable of large diameter. Indeed, the voltage strength between the command and the power is permitted by a high voltage drive cable.

The drive cable is mounted in parallel position along the power board, for its entire length. To avoid inductive coupling with the power circuit, which could generate a parasitic current during power dI/dt, the return pass of the drive cable is mounted close to the ferrite core. This way, mutual inductance between drive and power is reduced.

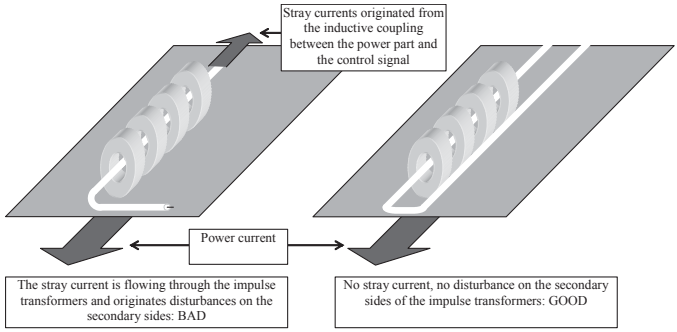


Figure 3.35. *Mounting of the drive cable: the way and the return pass are close together in order to reduce the mutual inductance between the drive circuit and power circuit*

3.4.2.3. *Importance of parasitic capacitors*

With series connection, high levels of voltage are reached, this leads to specific constraints on interconnections of the converters elements. The following text gives some indication of the issues related to high voltage:

– A filer wiring exhibits a linear inductance of about one microHenry per meter, and a linear capacitance of about one hundred microfarad per meter.

– In classic applications of power electronics, with low voltages, engineers are facing parasitic inductances of the wiring. In order to reduce these inductances, classic solutions lead to use of large conductors, with a return pass as close as possible to the way paths; see [JEA 01], in particular the chapter on wiring models.

– When there are high voltages, for the same commutated power, currents and dI/dt are much smaller, and issues with wiring are related to parasitic capacitors. This means an important part of the switched current is used to charge parasitic capacitors, and does not participate in the energy transfer.

On the other hand, physics does not allow for the creation of high voltage wiring with very low capacitances. It is possible to make very low inductance wiring with very large conductors, with conductors close together for the way and return currents. However, a wiring with very low capacitance would correspond to wires very far away from each other, with a very thin section. In this case, the electric field in the air or in the insulating layer has exceeded the maximal allowable field, and partial discharges occur around the cable.

In conclusion, very low inductive wiring may be achieved, but it is impossible to create very low capacitive wiring, at least with high voltage.

For a series connection, series connected elements show parasitic capacitances with external parts: for instance with mechanical mounting; and with command. When components under voltage are closing, the discharge of these capacitors, through the series connected elements, leads to a change in the current shared between these components. Figure 3.36 shows the series connection of switches and the influence of the environment on parasitic capacitors, and current sharing between these switches.

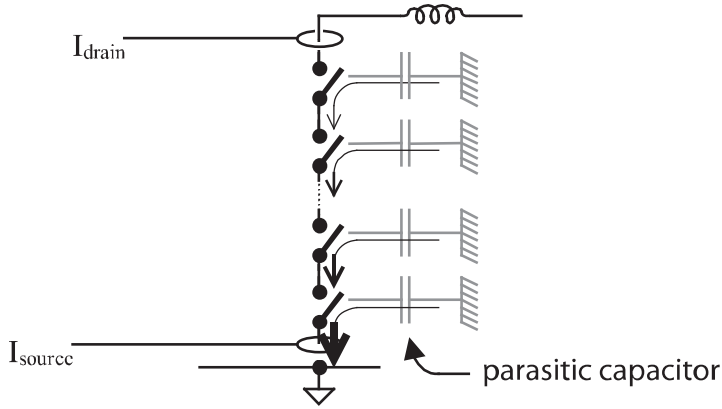


Figure 3.36. *Series connection and the influence of parasitic capacitor current sharing*

The "hot points" of a switch refers to the parts of this switch stressed by a voltage change compared to ground. In turn the "cold points" of a switch are the parts of this switch that have a constant voltage compared to ground, and therefore are not stressed by a dV/dt compared to the ground and environment.

Thus, components connected to a cold point are stressed by a current overload. The following curve, from [GUI 95], shows currents at a hot point (drain of a

superior MOS in the series connection), and currents at a cold point (source of the ground connected MOS), in a series connection of 40 MOSFET, supplied under 10,000 V, and flowed by a nominal current of 1.6 A.

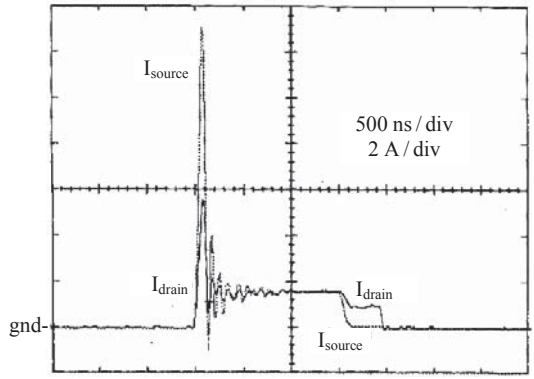


Figure 3.37. *Waveforms of currents sharing at switch-off in a 40 MOSFET series connection*

During commutation, the current imbalance of 10 A may be compared to the nominal current of 1.6 A. These current imbalances come from the discharge currents of the parasitic capacitances of the switch.

During commutations of a matrix, between stages and mechanical grounds, parasitic capacitors generate currents during the dV/dt. Parasitic capacitors of the stages stressed by the highest dV/dt compared to external parts must be reduced in order to reduce over-currents. Where distance increases from the ground, and where successive stages make electrostatic screens from one to the next, structures in the orthogonal direction, are well suited, compared to structures utilizing small distances from the ground plan.

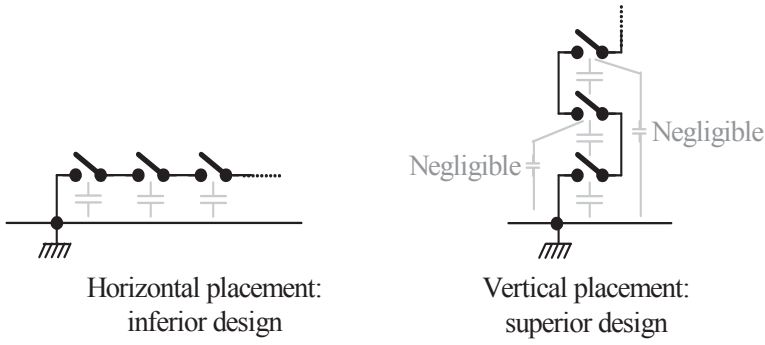


Figure 3.38. *Series connection: vertical implementation of elements, in order to reduce dV/dt applied to parasitic capacitors during commutations*

With an horizontal implementation, all parasitic capacitors are in the same range of magnitude, but dV/dt increases in the region of the hot point. Thus giving parasitic capacitive currents more importance.

With a vertical implementation, the screen effect made by the lower stage minimizes the parasitic capacitor with the mechanical ground, this, can be compared with the capacitor of the inferior stage. All dV/dt are thus of the same order of magnitude (the magnitude of the commutation of a stage) and parasitic currents flowing through parasitic capacitors and components are reduced.

For series connection, vertical implementation of the elements under voltage is well suited, in order for the low voltage stages to take advantage of the screen effect of the high voltage stages. The dV/dt seen by parasitic capacitors are those of only one stage. The influence of parasitic capacitors compared to the mechanical parts and the environment is minimized.

3.4.2.3.1. Soft commutations

Resonant circuits may be designed, so that parasitic capacitors are integrated into resonant capacitors [LAP 98]. This way, parasitic capacitor energy is not wasted during commutations. This allows for the design of high voltage converters with very good efficiencies that are able to operate at higher frequencies.

3.4.2.4. *Voltage management*

As components are sensitive to the power voltage, it is necessary to design protection circuits, and perhaps balancing circuits. Some strategies for this are presented in the following sections.

3.4.2.4.1. Voltage balance

In a series connection, we must take care not to apply a voltage to components that they are unable to support. Assuming this feature, in addition to very well synchronized commands, a traditional solution was to obtain every time an equal balance of voltages at any given time. For this reason, components are connected in parallel with a resistor for static balance (flowed by a current ten times larger than the leakage current of the switches, or ten times larger than the maximum deviation of the leakage currents of the switches), with a RC circuit for commutation help (which minimizes the imbalances during switch-off of the components), and maybe with a clamping circuit in order to limit the maximum voltage [FRE 01]. This is a very heavy solution, due to the number of additional components, and their cooling constraints. Nevertheless, this is the well suited solution if the safe operating area for the components is reduced. The equal balance may also be achieved by a command including a closed loop control for active balancing.

3.4.2.4.2. Clamping of voltages

Voltage balance is not always a strict requirement. An alternative strategy does not look for balance at any cost. Rather, the minimal requirement is to operate the switches of the series connection inside their safe operating area. Nowadays, as components of power electronics have vastly extended safe operating areas, series connection of these components may be achieved with a clamping device on each stage, or even with no additional protection if the components are able to support intrinsic clamping by the avalanche.

They are three types of voltage limitations for semiconductors components:

– Use of the possible ability of protection against voltage, appropriate for the component to be protected. This is an *intrinsic clamping* of the component (by the avalanche). One must pay attention to the word avalanche, as it may be understood not only as clamping, but also as destruction of the device.

– Protection by an added device, implemented in parallel on the component to be protected. This kind of protection is traditionally called *passive clamping*.

– Action on the drive electrode of the component to be protected when a given voltage is exceeded. In linear operation, the component regulates the voltage across its connections. This is called *active clamping*.

3.4.2.4.3. Intrinsic clamping

The intrinsic clamping ability is well known for components such as transils and Zener diodes. Other components such as diodes, MOS and IGBTs may include manufacturing quality that can confer to them, in addition to a very good reproducibility of their characteristics, a good ability for clamping. Nowadays, few devices are specified to support a clamping intrinsic avalanche. For MOS transistors, a classic specification is a tolerance of their direct forward current rating as an avalanche clamping current. This specification of a current is well suited for power electronics. For some components, an energy is specified, corresponding to tests under a low current over a long period of time. This specification does not inform the designer of the behavior of the component when it is brought to clamp during a switch-off commutation. When using the clamping avalanche of the component, it is necessary to compare the current to be clamped in the worst case to the clamping current tolerable by the component.

In the case of diodes, the worst case current is difficult to determine. A good selection criteria of diode technologies is the ability to support their nominal current as an avalanche current. In this case, these diodes are used in a series connection or matrix connection without any unitary selection. Conversely, as long as the

manufacturer does not specify the avalanche current rating of the diodes, any change may occur in the characteristics, due to a change of the diode.

For example, here is a comparison on avalanche clamping tests between two generations of 500 V MOS: IRF840 and IRFB11N50A. The latter being a last generation transistor.

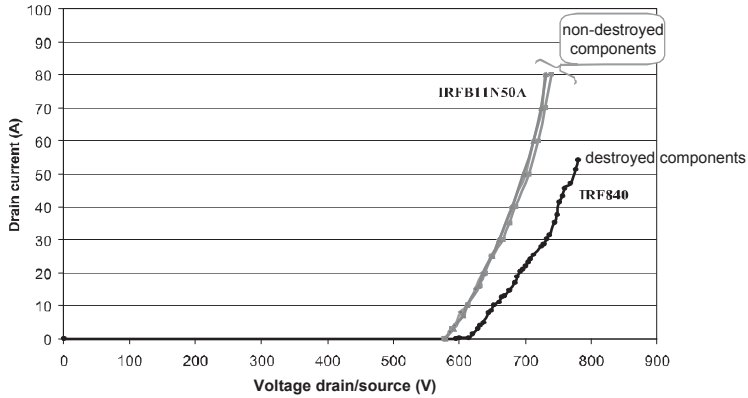


Figure 3.39. *Dynamic characteristics of two types of 500 V MOS during avalanche condition*

IRF840 is destroyed for an avalanche current of 60 Amps, while the IRFB11N50A component operates with a 80 Amps current. Additionally, during avalanche operation, the dynamic resistance is smaller for the IRFB11N50A component, and this allows the voltage across the component to remain smaller for the same current.

Manufacturers guarantee an avalanche current of 8 A and 11 A respectively, in other words the specified nominal current.

3.4.2.4.4. Passive clamping

Specific components are used for passive voltage protection, as transils or varistances, connected in parallel to the semiconductors to be protected. This kind of protection requires a clamping voltage, for the protector component, lower than the avalanche voltage of the component to be protected (e.g. a 440 V transil for a 500 V MOS). Figure 3.24 gives the voltage characteristics of transils 1.5KE 350 and 1.5KE 440 Volts.

The dynamic resistance of protection systems leads to an increase of the voltage across the protection component, the clamping current increases. It may reach the maximum voltage rating of the component to be protected, which then clamps or is destroyed (according to its ability to support the clamping by avalanche).

In order to obtain a voltage lower than the voltage rating of the MOS, three classic solutions are used:

– Choice of a transil with a lower voltage rating. Drawback is "derating" of the voltage rating of the protected components. For example, the 500 V MOS must be used under 350 V.

– Series connection of transils with lower ratings (which have a lower dynamic resistance).

– Parallel connection of several transils. This way, dynamic resistance is reduced by the same factor as the number of associated diodes. Dynamic resistance ensures a good balance of current between diodes. Drawback is the cost of this method, and its volume.

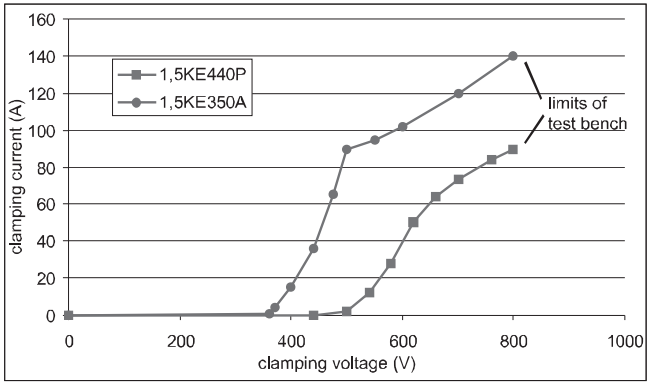


Figure 3.40. *Dynamic characteristics of 1,5KE350 and 1,5KE440 transils, during clamping operation, at a very high current*

3.4.2.4.5. Active clamping

Active voltage protection of driveable semiconductor components is achieved via feedback, on the command electrode, from the protected component. The operating mode of such a protection against overvoltage is similar to that of a closed loop voltage control [LAU 99].

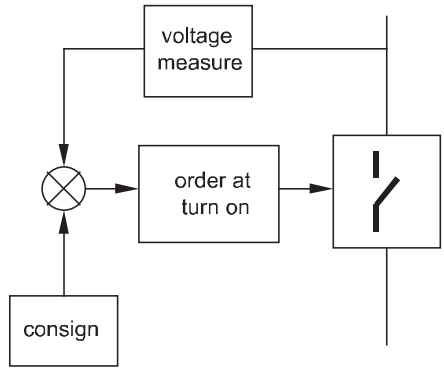


Figure 3.41. *Active voltage protection: closed loop voltage control*

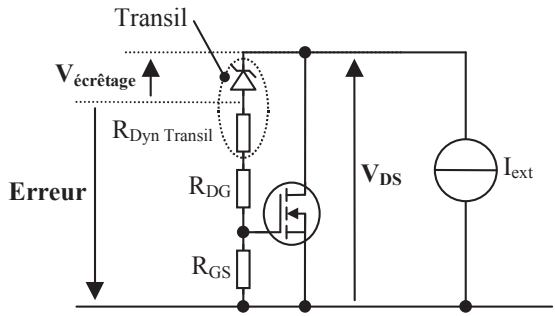


Figure 3.42. *Basic schematic of a MOS, protected by active clamping*

The apparent resistance of the clamping circuit may be a very low benefit from the loop gain. As the component is used inside its safe operating area, it may be used at high current and absorb high energies. This way, active voltage clamping protection of semiconductor components appears to be an efficient and robust solution (very low dynamic resistance, very high current rating).

Now, as for any classic closed loop control, a large gain may lead to instabilities of the control. This occurs for operation at low power current, and with low drain-grid resistance (R_{DG}), as seen in the following example.

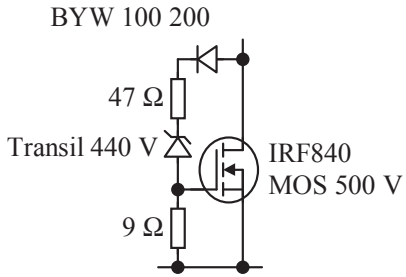


Figure 3.43. *Test circuit for the study of closed loop voltage control instabilities, at low current*

For parallel and series connections, the design of the closed loop control must take into account oscillatory modes between components.

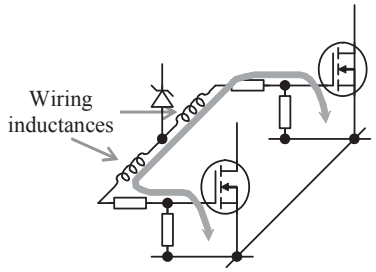


Figure 3.44. *Instabilities due to exchange of charges between grids of parallel connected components*

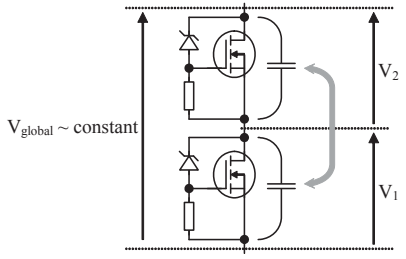


Figure 3.45. *Instabilities due to exchanges of charge between drain-source capacitances of series connected components, during operation under a defined exterior voltage*

Active voltage clamping protection of semiconductor components appears as an efficient and reliable solution, which makes a very low dynamic resistance and very

high current rating. On the other hand, stability of the closed loop control must be achieved. This stability is more difficult to achieve when component commutations are faster, and when load variations from the exterior are stronger.

3.4.2.5. *Reliability of series connections* [LAU 00a]

Series connection of components may be used to make a switch with very high reliability [CHA 00]. Indeed, the first consequence of the failure of a component is the components inability to support a voltage. Thus, a parallel connection of components is less reliable than a single component. Only one failing component is necessary to cause failure of the global switch. Repairing requires isolation of the failing component.

With a series connection of components, failure of one component may be tolerated. If the series connection includes a sufficient number of components, a voltage security margin of some stages allows a tolerance of the corresponding number of failing components. For this, other components have to share the voltage between them; and command must not be interrupted by the failing component. In a practical sense, the failing component is always conductive, and does not disturb the good operation of the switch.

With series connection, reliability is improved. The global switch is more reliable than the stages it is made of. Moreover, the system is no longer in danger of a random failure. A random failure may appear, but it will not put the switch into default. The series connection offers a possibility of natural redundancy that allows a certain tolerance of failure improves reliability and allows for a possible preventive maintenance. For example, a preventive control may be run every three years to verify the presence or absence of defects on stages, and the correction of these defects.

Similarly, matrices may be tolerant to failure if all components continue to be controlled despite the failing component, and if the design of the matrix is planned accordingly. Thus, the 25 kV – 1,600 A switch presented at the end of this chapter should have a 20,000 hours MTBF, if failure of one component would lead to failure of the switch. Actually, following the tolerance of failure provided by the series connection, it offers a lifetime of 200,000 hours if there is no preventive maintenance. With a preventive maintenance, it enables us to perform an availability rate of 99.99%. In actual fact, the switch is more reliable than the command board that drives it.

3.4.2.6. *Design: Specific features of high voltages*

3.4.2.6.1. Perturbation aspects

As voltages are added along the series connection of switches, the dV/dt, compared to the environment, from the top (hot) point of the switch, may become very important. From a circuit point of view, we can say that this dV/dt generates currents in all parasitic capacitances with the surrounding elements. From an EMC view point, we have a generator of electric field in the air. Although levels change (20 kV switching within 20 ns matches 1MV/μs), design rules relating to EMC are the same in high voltage as in classic power electronics. If necessary, Faraday cages, made judiciously, can provide very effective solutions. The signals and power supplies may be distributed by common mode inductors, in order to avoid perturbations from high frequency voltages, on the so-called "cold" points, during commutations.

3.4.2.6.2. Security area at switch-on and security area at switch-off

The minimal requirement to comply with, in a series connection or a matrix connection, is to maintain the components in their areas of security. As a matter of fact, the high voltage switches, operating in thyristor mode (ZCS), are much easier to achieve than those operating in dual-thyristor mode, or hard commutation. There are two physical reasons for this:

– Firstly, for most of the components, the security area for switch-on is larger than the security area for switch-off. This phenomenon is already well known for bipolar transistors. It is possible to make an excellent synchronization at switch-on by strong command currents. For example, with a three amperes current trigger on thyristors packaged in TO220 cases, voltage on the component terminals drops within 50 ns [CHA 01].

– Wiring inductances help commutation. That is why the voltage drop is used as a criterion in the case of a strong switch-on of the component (MOS, thyristor). This switch-on is so fast that all the voltage is applied to the terminals of the wiring inductances: this last reason defines the dI/dt.

3.4.2.6.3. Partial discharges and the Paschen curve

The Paschen curve is a bathtub shaped curve, which reflects the voltage strength of a gas blade, as a function of its pressure. For normal pressure or higher pressures, the voltage strength increases between the two parts, by enlarging the distance between the parts, or increasing the gas pressure. In the first case, the electric field decreases. In the second case, the average trail of ions and electrons is reduced, and therefore the trip, during which they will be accelerated by the electric field. With a low pressure below the millibar, the voltage strength increases by reducing the

distance between parts. In this case, ion or electron will have little probability of hitting a molecule before reaching the attracting electrode. This way, gas pipes hold 20 or 30 kV with a distance of a few millimeters between electrodes. Thus, there is a minimum Paschen voltage, below which the dielectric breakdown can not occur, regardless of the distance between parts: this minimum is around 300 volts in the air.

Let us now consider the breakdown voltage at the interface between two different dielectrics. Consider two electrodes, isolated from each other by two superimposed dielectrics: the equivalent schematic seen by the electrodes is a series connection of two capacitors, in parallel with two resistors. Under a continuous voltage, voltage sharing involves the resistivity of the areas. For example, in the case of a solid polymer type insulator superimposed on an air space, we can observe that the solid dielectric holds most of the voltage, due to its very high resistivity. With alternative or pulsed signals, the voltage sharing involves the inverse values of capacitances. The main voltage appears on the terminals of the smaller capacitor. In the case described above, the electric field is now mainly in the air. Also, the material has a high permittivity, the electric field is weak inside it, and the field is important in the air. When the maximum field in the air is exceeded, there are egrets that correspond to a micro-arc, which discharges the capacitor made of the air space and the local charge of the insulating layer. This is not a complete short circuit, as the solid insulator is not destroyed. This phenomenon is called a partial discharge. If the insulator is a polymer, partial discharge punctures it gradually. Mineral insulators are stronger against this phenomenon. In 50 Hz high voltage transformers, the phenomenon of partial discharges is measured by the high frequency noise generated. This physical phenomenon is also used industrially to generate ozone.

With pulsed or alternative high voltage, we obtain a better insulation using air alone, rather than by adding an intermediate insulator, which increases the field in the air and causes partial discharges. Otherwise, it is better to use materials that have weak permittivities, such as Teflon. Every dielectric casting between two parts must be free of air bubbles, under penalty of partial discharge in the bubble, and then gradual degradation of the insulation.

Because of the above-mentioned Paschen law, there are no partial discharge problems for conventional power electronic voltages, i.e. below 1,000 volts. However, for study of higher voltage systems, these physical phenomena impose different design rules.

In power supplies, while the voltage does not exceed the minimum of Paschen, transformers do not mandatorily require vacuum impregnation. Now, partial discharges appear and are heard when the power supply runs an alternative dielectric test. This explains the questions raised by supply manufacturers between continuous or alternative power supply dielectric test results. As mentioned above, the physics

of these two tests is not the same. With alternative voltage, the test degrades the transformer by partial discharges, resulting in a limited duration of the test. The shape of parts is important for the electric field in the air around these parts. An edge makes a strengthening of the local electric field, and a partial discharge may occur at that point.

For high voltages, liquid insulators such as mineral oils are still commonly used. These are high-performance solutions in terms of dielectrics and cooling. Mineral oil is a very good dielectric. As a liquid, it tolerates partial discharges by the edge effect, due to the renewal of oil at the point of strong electric field. No air bubbles can be created, and residual bubbles are naturally removed, by gravity or by filling oil under vacuum conditions if air bubbles can be blocked, as in a transformer. A circulation of cooling oil may be used and allows a very efficient cooling, as with all liquid cooling systems.

3.4.2.6.4. Design examples

Figure 3.46 depicts a MOS board for 5,000 V, 1,000 A, driveable at switch-on (thyristor mode), and a 25 kV 1600 A module allowing for a voltage drop within 20 ns and a lifetime of 200,000 hours.

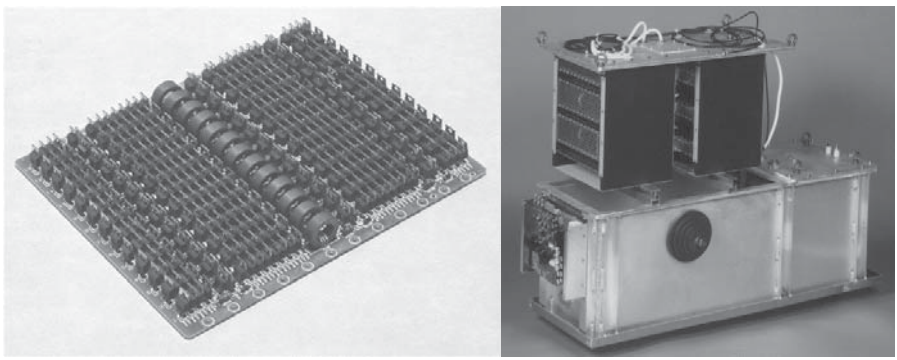


Figure 3.46. *MOS board and module*

Figure 3.47 is a 5,000 V 500 A board driveable at switch-on and switch-off, holding short circuits without any additional series inductance, and able to open under short circuit.

Figure 3.47. *Board of MOS ON OFF CC, 5 ,000 V, 500 A*

These boards are used for the generation of square power waveforms with strong front edges (+30 kV and -30 kV maximum, with 500 A, within 100 ns), able to support perfectly arcing short circuits (no dI/dt limitation by additional inductance [CHA 00]).

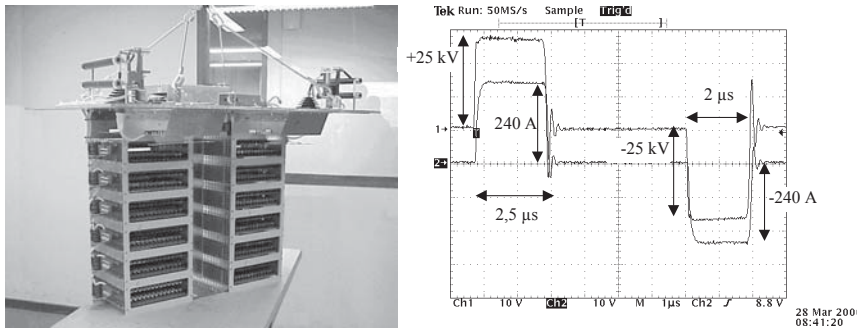
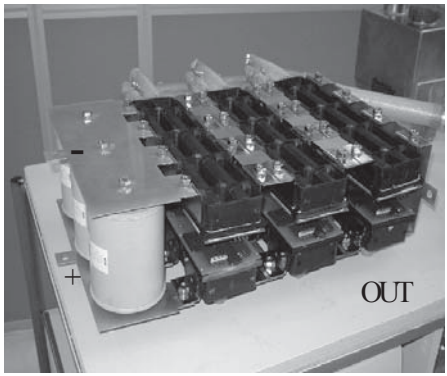


Figure 3.48. *Half bridge made of two 60 kV switches, and output signals*

A further design example is the IGBT inverter: 5,000 V 400 Amps (ALSTOM – European contract HIPO) [FRE 01].

This is a high power inverter for traction application, including modules with high current and voltage ratings (3,300 V 400 A in the example shown, 6,500 V in the final application). The series connection is thus reduced to a smaller number of more expensive items, which clearly prohibits redundancy. It is therefore vital to ensure not only protection but also voltage balance in the association. A specific

control board was developed and integrated into the modules, allowing this dual function of balancing and protection.



Electrical Properties :

5.5kV DC Bus

Output : 4kAC-300Arms
Power : 700kW
Size : 500 X 350 x 160 mm

Weight : 15kg

Figure 3.49. *Traction inverter (ALSTOM-HIPO). Electrical properties: 5.5 kV DC Bus; 4 kAC-300 A output; 700 kW power; 500x350x160 mm size; and 15 kg weight*

A board of diodes, another example, is depicted below in Figure 3.50. This matrix of diodes does not use any balancing system, and components are not selected. The diodes involved support their nominal current as an avalanche current.

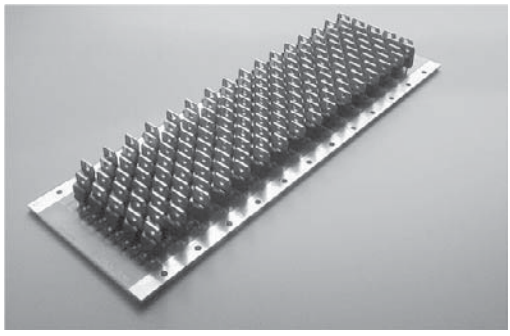


Figure 3.50. *Diode board: 12 kV, 800 A peak, made of a matrix, 10 series - 16 parallel*

The final example is a thyristor board. To meet the needs of commutation of high pulsed currents during large times (several dozen microseconds), a board made of thyristors was developed. It is made of a matrix including five components in series, and ten in parallel.

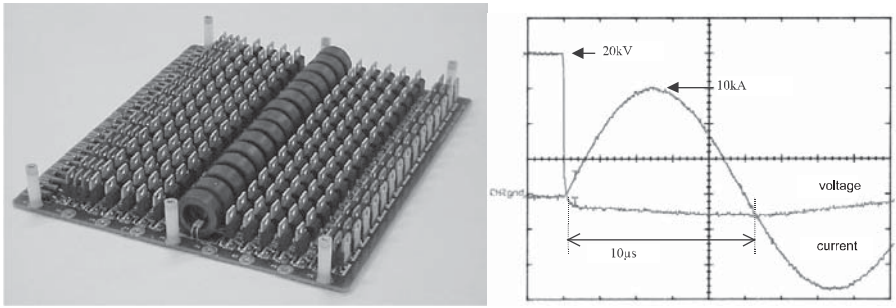


Figure 3.51. *Thyristors board and commutation under 20 kV with two series connected boards*

Synchronization is made by a strong gate current to reduce spreading at switch-on. The curves in Figure 3.51 show a commutation of a 20 KV module, made of two series connected boards, on a RLC circuit. There is a voltage drop of 20 kV within 20 ns, so dV/dt = 1 MV/µs; and an increase of current from zero, dI/dt = 12 kA/µs.

3.4.3. *Matrix connection of components [CHA 99]*

Series connection is an association which may be defined as follows:

"Series connection of components is a kind of association where, during static operation, all components flow by the same current, and where the global voltage is shared between them" [LAU 00a].

In turn, parallel connection may be defined as follows:

"Parallel connection of components is a kind of association where, during static operation, all components are under an equal voltage, and where they share the global current between them" [LAU 00a].

In the case of high voltage and high current components, the number of associated components may be high. The components may be series connected to support a high voltage, and these series may then be associated in parallel. We call this association *a parallel connection of series associations.*

Components may be parallel connected to commutate important currents, and these parallel connections may then be associated in series. We call this association *a series connection of parallel associations.*

Figure 3.52 illustrates these two associations for diodes.

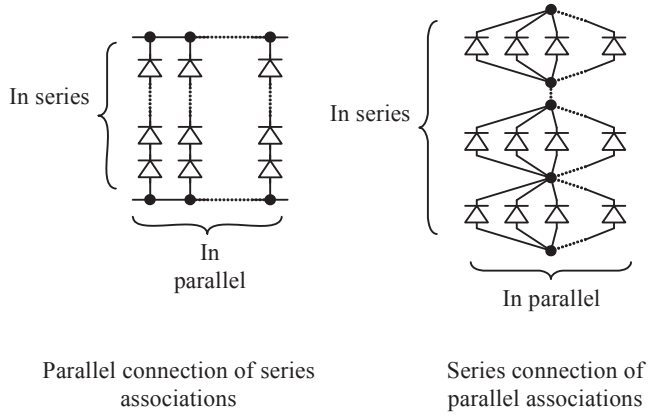


Figure 3.52. *Parallel connection of series associations and series connection of parallel associations*

It should be noted that a series connection of large power IGBT modules (for instance for traction) is, as a matter of fact, a series association of parallel connections; because any IGBT power module is usually made of a parallel connection of several dies of IGBT and diodes.

Let us call the structure of Figure 3.53 a matrix, which shows both the series connection of components and the parallel connection of the same components.

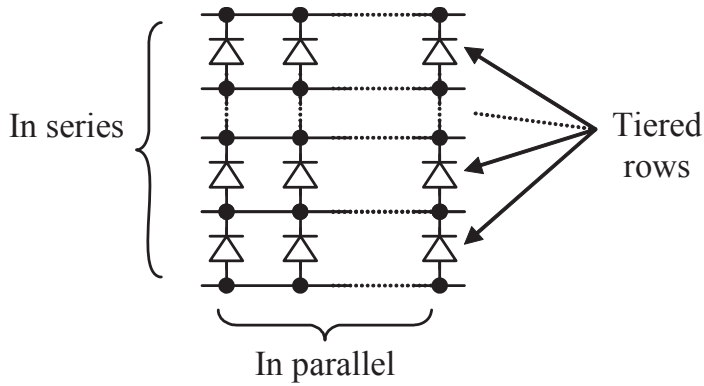


Figure 3.53. *Matrix*

The matrix is different from the series connection of parallel connection because the current of each stage is not flowing to a single point. In practice, this leads to the design of switches with very low parasitic inductances, since the current remains

distributed over the entire width, in other words, between the paralleled components. When there is no current concentration, switch inductance remains minimal.

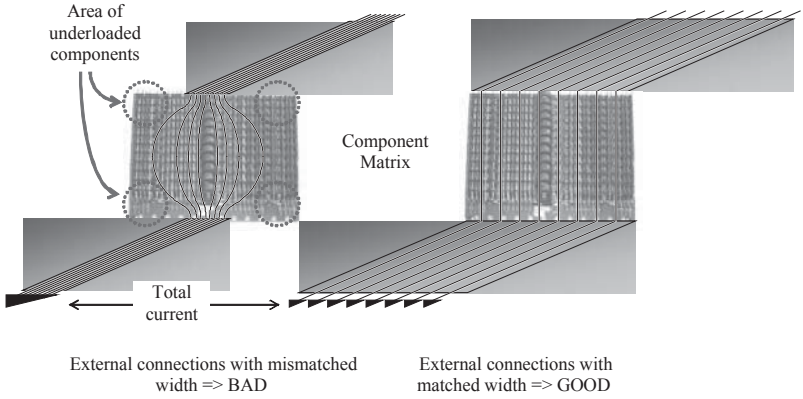


Figure 3.54. *Recommendations for external connections of the component matrix*

Nevertheless, connection impedances between components, still physically present, make the matrix more complex. The matrix includes two dimensions, series and parallel, and it is impossible to determine the kind of association (series or parallel) which was at the foundation of the structure. Figure 3.55 shows the general matrix.

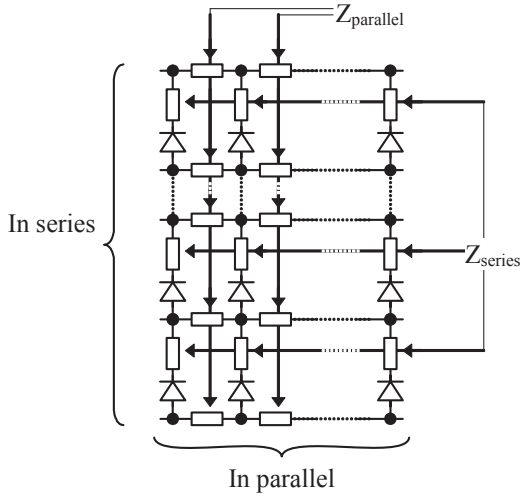


Figure 3.55. *Matrix schematic including parasitic wiring inductances*

Impedances Z_{series} and $Z_{parallel}$ between stages and between lines are part of the matrix. In practice, these impedances represent the matrix component connections. Resistive or inductive, these series impedances (Z_{series}) modify current and voltage levels seen by components, and the parallel impedances ($Z_{parallel}$) suppress the equal voltage concept between the different stages of the matrix. Additionally, couplings of mutual inductances may occur.

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Chapter 4

Silicon Carbide Applications in Power Electronics

4.1. Introduction

Despite its extreme rarity in the natural state, silicon carbide was one of the first semiconductors discovered: J.J. Berzelius (the "father" of silicon) was the first to study its physical properties, in 1824. The first to exploit its electro-luminescent properties was H.J. Round, in 1907 [ROU 07]). In 1955, Lely [LEL 55] was defining the first method of synthesizing mono-crystalline substrates, the dimensions were admittedly small and random, but had very good structural quality. Thus, the first period of intense research devoted to silicon carbide (in the USA, Russia, Japan, Germany) dates back 50 years, driven from the beginning by the very interesting physical properties of this material for solid state electronics.

Yet it is only recently (in 2000 and 2001) that the first ads for industrial manufacturing of power components, based on silicon carbide, were made (by Microsemi, then Infineon), in the form of Schottky diodes, with voltage and current ratings that now reach 600 V and 12 A. These initial products are the result of works revived and expanded throughout the world in the 1980s, thanks to new major discoveries in the field of manufacturing techniques usable by the industry. Despite the tremendous growth of the silicon industry and the considerable developments already achieved, the approaching of silicon's physical limits in many applications, particularly those in power electronics, also contributes to the high level of interest

Chapter written by Marie-Laure LOCATELLI and Dominique PLANSON.

being generated for some semiconductors with large prohibited broadband energy, particularly silicon carbide.

Given the potential of power components made of the emerging silicon carbide, and those of the prototypes reported by the specialized journals, this "new" semiconductor now appears to be able to:

– favorably replace silicon in certain applications by improving the overall performance of the system (remembering that silicon is the material of choice almost exclusively for the manufacture of power components);

– to expand the fields of existing applications; or even

– give rise to new areas of use previously inaccessible for semiconductor components.

Before presenting the various potential applications of new silicon carbide (SiC) power components, this chapter will become better acquainted with the material, before describing the state of the art technology. The final section will present designs already made with SiC, SiC impact on the design and performance of systems, and will indicate the likely applications of these systems.

4.2. Physical properties of silicon carbide

4.2.1. *Structural features*

Electronic applications involve devices based on semiconductor materials with crystalline structures.

The crystal structure of monocrystalline silicon is characterized by an arrangement of Si atoms along a face centred cubic network, with a mesh parameter of 5.431 Å. The structure of crystalline silicon carbide on the other hand can be described simply by stacking compact plans, each plan being a double layer of a compact plan of C atoms on a compact plan of Si atoms. The pile of a second double layer on a first one can be in two positions, different from each other and different from the position of the first level. This is obviously the same for the next level, and so on. The three possible positions for a double layer are generally named A, B and C. According to the stacking sequence (e.g. ABCB…) and its recurrence (e.g. 2 for AB*AB*AB*AB*… and 4 for ABCB*ABCB*ABCB…), the elementary mesh can be cubic (C), hexagonal (H) or rhomboid (R). Only one dimension of the grid (height, in the direction [0001] perpendicular to the plains, which is the axis of growth, axe c), is different from one pile to another. This way, several crystallographic arrangements may exist for the same chemical composition SiC.

This peculiarity of silicon carbide is named after polytypism (which is a polymorphism in one dimension).

170 to 200 crystallographic varieties or polytypes have been counted. Among them, few have been synthesized into the form of mono and stable materials (without inclusion of different polytypes). The polytypism of SiC also explains in part the difficulties historically found, and even today, for the production of substrates and homogenous SiC films, especially since it gives to each polytype physical properties whose ranges vary from one to another (as shown in the following section).

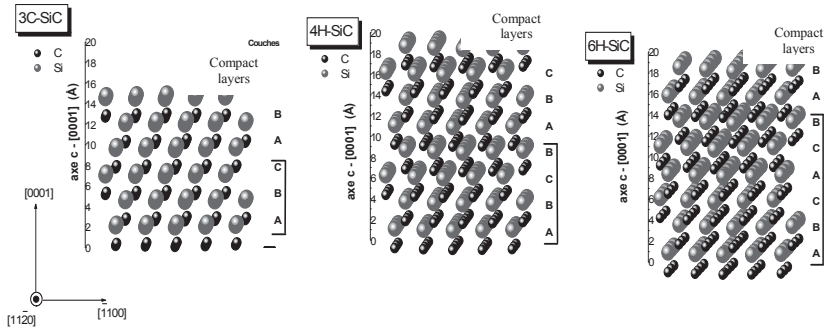


Figure 4.1. *Presentation of polytypes SiC-3C, SiC-4H and SiC-6H, and of Ramsdell notation. This allows kinds of SiC to be distinguished by a number (stacking periodicity) followed by letter C, H or R (form of the elementary mesh)*

Polytype	**3C**	**4H**	**6H**
Stacking sequence	ABC	ABCB	ABCACB
Mesh parameters (Å) **Si : a = 5.431 Å**	a = 4.349	a = 3.073 c = 10.05	a = 3.081 c = 15.12

Table 4.1. *Characteristic dimensions of crystalline meshes of SiC-3C, SiC-4H, SiC-6H and Si, at 300 K*

The most common polytypes studied for electronics are known as SiC-3H, SiC-4H, SiC-6H, according to the notation of Ramsdell. Figure 4.1 illustrates these three structures and the principle of Ramsdell notation. Table 4.1 shows for each polytype

the specific dimensions of their crystal mesh at room temperature, as well as those relating to silicon.

4.2.2. *Chemical, mechanical and thermal features*

The link between the Si atom and the C atom is strong, with an energy equal to 6.34 eV (the binding energy between two atoms of silicon is only 4.63 eV). This simple fact makes silicon carbide a resistant material from various points of view, and contributes to the interest for it, for various applications including electronics. This property, however, includes drawbacks for the implementation of the SiC semiconductor.

Firstly, SiC is high temperature resistant, breaking only at 2,830°C. Sublimating rather than melting under reasonably accessible pressure, silicon carbide cannot be synthesized from the liquid phase by conventional techniques of recrystallization. The growth of a single crystal is more delicate than that of silicon, especially as the resulting crystalline arrangement is very sensitive to the conditions of temperature and pressure.

Silicon carbide is also chemically resistant, and it is very difficult for a foreign atom to penetrate the network of this material to travel inside. An input of energy (e.g. heat, photonics, electrical, or mechanical, etc.) higher than the case of silicon is necessary. In terms of temperature stability, these features are assets for operation in hostile environments and for reliability, but they do not facilitate the steps of production of components based on chemical reactions (cleaning, engraving, oxidation) or diffusion of impurities.

Since Acheson developed the first manufacturing process of SiC, in the 19th century, silicon carbide has been well known for its mechanical resistance as an abrasive n the form of clusters of hexagonal mono crystals, impure and from various polytypes and sizes). This hardness (about three times that of silicon), which is not really a superiority for electronic applications, is reported here because it has an effect on mechanical treatments, such as cutting and polishing units in the manufacture of semiconductors for electronics.

In terms of thermal expansion, the coefficient of silicon carbide ($4x10^{-6}$ K^{-1}) is approximately two times greater than that of Si, which increases the gap with that of silica ($5.5x10^{-7}$ K^{-1}), but reduces to that of copper ($17x10^{-6}K^{-1}$), or aluminium ($22x10^{-6}$ K^{-1}).

4.2.3. *Electronic and thermal features*

As referred to in the introduction of this chapter, the attraction to the physical properties of silicon carbide for use in electronic applications is at the heart of many studies that have been, and are now doomed. The vast majority of these studies concern the three most common polytypes: 3C-SiC, 6H-SiC and 4H-SiC. Many publications present measurements and modelling parameters of these materials, and some properties are nowadays accurately determined (such as the forbidden energy band, or the effective masses, etc.). However, due to sensitivity to the purity of the material, or its anisotropy, some parameters are fairly dispersed or incompletely determined (e.g. mobility and saturation speeds of load porters, especially holes; or critical breakdown field, etc.). Table 4.2 brings together the main important features for the performance of semiconductor components. The values given are trying to account for dispersions, being an average of the main results of edited measures, for a temperature of 27°C, and for a doping of 10^{15} cm^{-3}. All three SiC polytypes, with whom structure tests were performed, are considered here along with silicon, as a benchmark. For hexagonal polytypes, the values of mobility and speeds of load porters are provided for both parallel directions ($||$ c) and perpendicular ($\perp$c) to the axis of growth c.

	Si	3C-SiC	6H-SiC	4H-SiC
E_g (eV) Forbidden bandwidth	1.12	2.2	3.02	3.26
E_c (MV/cm) breakdown electric field	0.28	1.5	2.2	2.2
ε_r dielectric constant	11.8	9.66	9.7	10
μ_n (cm^2/Vs) intrinsic mobility of electrons	1350	900	400 ($\perp$c) 90 ($||$ c)	800 ($\perp$c) 1,000 ($||$ c)
μ_p (cm^2/Vs) intrinsic mobility of holes	480	40	100 ($\perp$c) 20 ($||$ c)	110 ($\perp$c) 140 ($||$ c)
v_{sat} (10^7 cm/s) saturation speed of carriers	1	2.5	2 ($\perp$c) 0.2 ($||$ c)	2.2 ($\perp$c) 0.33 ($||$ c)
n_i (cm^{-3}) intrinsic concentration	$1.4x10^{10}$	6.9	$2.3x10^{-6}$	$8.2x10^{-9}$
λ_{th} (W/cm.K) thermal conductivity	1.5	4.9	4.9	4.9

Table 4.2. *Main physical properties for components performances: comparison of most common SiC polytypes and silicon (values at 300 K for doped materials at 10^{15} cm^{-3})*

4.2.3.1. *A large forbidden energy bandwidth*

Silicon carbide is part of the family of semiconductors known as "big gap" because of its *prohibited energy bandwidth* E_g, which is higher than that of silicon (2 to 3 times according to the polytype). Two other important properties follow on from this, which are a higher *breakdown electric field* E_c (almost multiplied by 10), and a lower *concentration of intrinsic* n_i *load carriers* (9 to 19 orders of magnitude depending on the polytype).

4.2.3.1.1. Improvement of the voltage and temperature strengths

With such features, silicon carbide makes it possible to increase the range of blocking voltages allowed by the semiconductor components, and this includes at high junction temperatures. Indeed, breakdown voltages, exceeding 10 kV in volume, can be supported by layers with doping levels between 10^{14} cm^{-3} and 10^{15} cm^{-3}, and thicknesses as low as 70 µm – 80 µm, as shown in the charts presented in Figure 4.2.

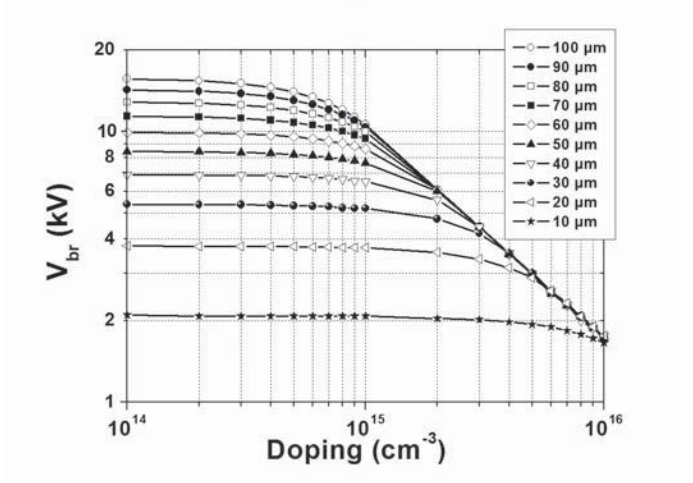


Figure 4.2. *Breakdown voltage* V_{br} *(V) as a function of doping* N_D *(*cm^{-3}*) and thickness* W_N *(µm) of the voltage submitted layer, providing numerical calculation of the inverse characteristic, and taking into account ionization coefficients per impact provided [KON 97]*

Recall that the breakdown mechanism is the ionization of an atom of the network, by impact with a free carrier greatly accelerated by the local electric field. If the kinetic energy gained by such a carrier is enough, it can "obtain" an electron from the top of the valence band to the bottom of the conduction band, leaving a vacancy in the valence band called a hole. A new electron-hole pair is created, which will be able to participate to the increase of the reverse current through the

structure (possibly generating, in turn, an electron-hole pair by ionizing collision, thus contributing to the increasing number of load carriers).

Charts in Figure 4.2 provide the breakdown voltage in volume of a plane structure P^+NN^+, with dissymmetric and abrupt junctions. The breakdown voltage is calculated numerically and corresponds to the voltage where the multiplication factor of holes or electrons becomes infinite along a line of maximum field in the structure. The calculation is made according to the slight doping of the central layer slight N doped (the "voltage held layer"), for different thicknesses, and at a uniform temperature of the semiconductor equal to 300 K; having retained as a coefficient the values of ionization of electrons and holes published by Konstantinov *et al.* [KON 97].

Calculations of leakage currents through the P^+NN^+ structure in the opposite polarization, as a function of temperature, also show that the leakage currents associated with the thermal generation assisted by inherent pitfalls porters in the deserted area (J_{gen}), and with the diffusion of minority carriers from the adjacent neutral areas (J_{dif}), remain low in the case of silicon carbide up to a very high temperature.

Concentration of intrinsic carriers in a semiconductor of gap E_g: where N_C and N_V are state densities in conduction and valence bands, and where T is temperature	$n_i = (N_C.N_V)^{1/2}.\exp(-E_g/2kT)$
Thermally generated current in the state charge area: in which width is W_N, with τ rate of generation, and q elementary charge	$J_{gén} = q.n_i.W_N/\tau$
Diffusion current of holes from N zone: with doping N_d, with μ_p and τ_p mobility, and lifetime of holes	$J_{dif} = (qk.T)^{1/2}.(\mu_p/\tau_p)^{1/2}.n_i^2/N_d$

Table 4.3. *Intrinsic concentration of carriers and volume leakage current through a P^+N junction (abrupt and dissymmetric) under reverse polarization*

For example, an analytical assessment (from the relationships mentioned in Table 4.3) of J_{gen}, J_{dif} and of evolution in temperature of intrinsic concentration n_i, shows that we should reach 600°C, in the case of the SiC polytype 4H, so that the density of total leakage current exceeds 1 $mA.cm^{-2}$, in a deserted layer, with a thickness $W_N = 100$ µm, which is doped at $N_d = 10^{15}$ cm^{-3}, and where the time constant of carriers generation would be equal to $\tau = 1$ µs (considered as independent from temperature).

For comparison, in the case of silicon, the purest and thickest layers produced nowadays are characterized by thicknesses and doping slightly below 1 mm and 10^{13} cm^{-3} respectively. The maximum corresponding voltage ratings (in volume) reach 10 kV maximum, as can be seen on the charts in Figure 4.3. A $P^+N^-N^+$ structure with a "voltage holding" layer with the characteristics mentioned above, considering carrier lifetime is maintained at a high value of 100 μs, must operate with a junction temperature below 150°C, so that the leakage current does not exceed a density of 1 $mA.cm^{-2}$. Note: a decrease of lifetime (including concerns about giving more rapid features to the structure during commutations between on-state and off-state) would lead to a severe reduction of this temperature (50°C less for a decrease of τ by a factor of 10 only…

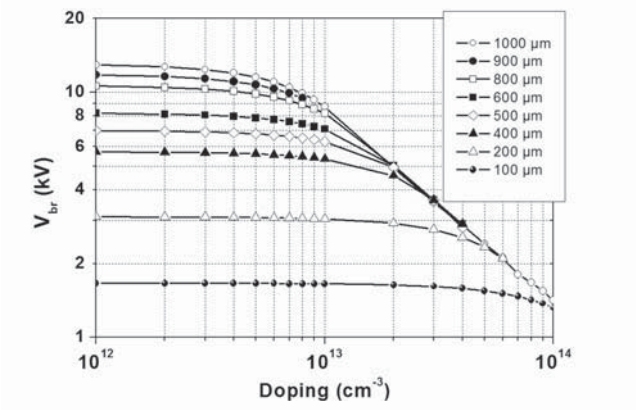


Figure 4.3. *Breakdown voltage V_{br} (V) as a function of doping N_D (cm^{-3}) and thickness W_N (μm) of the layer of Si under voltage, provides the numerical calculation of the reverse characteristic, taking into account the impact ionization*

So the progress made by the silicon carbide due to a forbidden energy band is broader (resulting in a higher breakdown electric field), and appears to be significant in terms of increased voltage ratings and the setback of the allowable operating temperature limits, if considering physical properties of the material in volume; and ideally free of defects.

4.2.3.1.2. Note about bipolar components

We should note that prohibited energy bandwidth also means a higher barrier of the PN junction. It will be more necessary to apply an extra 2 V to the terminals of a homo-junction of 4H-SiC, than to a homo-junction of silicon, to achieve the on-state. However, for applications with very high voltage, as considered in this part, this drawback will not present a drawback for bipolar components.

4.2.3.2. *Sufficiently mobile load carrier*

Let us now consider the range of voltage ratings already covered by components made of silicon, and consider the fact that the higher *breakdown field* of SiC leads to the ability to withstand a voltage under switch-off state, with a semiconductor layer whose doping is higher for a lower thickness. In addition to the reduction of the corresponding dimensions (interesting itself), this is especially relevant in terms of reducing conduction losses, all the more important since the *mobilities (μ_n and/or μ_p) of load carriers* involved in the mechanism are high.

Expressing these concepts with numbers, Table 4.4 shows the relative values of the factors of merit introduced by Baliga to indicate the interest in a new material for the design of a unipolar high-voltage component, minimizing conduction losses (with the BFM [BAL 82]), or the switching losses (with the BHFFM [BAL 89]). These values are normalized by those of silicon and allows a N-type conduction either lateral (perpendicular to the c axis), or vertical (parallel to the axis c), to reflect the anisotropy of the physical properties of 6H and 4H polytypes. (Note: the crystal structure 3C-SiC has no anisotropy in terms of its physical properties, as it is cubed). Note only the resistance of the layer of holding voltage is taken into account when calculating conduction losses.

This table shows again that significant progress is expected from the use of silicon carbide for the manufacture of high-voltage unipolar components. According to this "first order" assessment, the 4H polytype is the most promising, both for structures with vertical conduction and with lateral conduction.

We can greatly reduce the compromise between high current density in the on-state and high voltage rating, and increase the voltage range of unipolar components. From 200 V (maximum voltage rating with Si), the voltage ratings of Schottky diodes could be extended up to 3 kV. As unipolar devices (Schottky diodes such as field effect transistors) commutate faster than bipolar devices, a step forward in terms of reduced switching losses and increased switching frequencies of operating systems, which result at the same time.

Merit factor	3C-SiC	6H-SiC	4H-SiC
BFM / BFM (Si) *where* $BFM = \pi \mu_n E_g^3$	4	4.5 ($\perp$c) 1 ($\parallel$c)	12 ($\perp$c) 14.9 ($\parallel$c)
BHFFM / BHFFM(Si) *where* $BHFFM = \mu_n E_c^2$	16	15 ($\perp$c) 3.5 ($\parallel$c)	31 ($\perp$c) 38 ($\parallel$c)

Table 4.4. *Merit factors by B.J. Baliga for SiC common polytypes, divided by the corresponding values in the case of silicon (notations and values of physical parameters from Table 4.2 were used for these calculations)*

For the highest voltage ratings, the possibility of modulation of the electrical resistivity of the voltage held layer makes the bipolar device a more attractive option. In the case of bipolar components in SiC, the large voltage drop across the terminals of the PN junction (as a result of the broad band of prohibited energy) will be less of a drawback, for a given voltage class, as levels of current densities and frequency of the application will be higher. These conditions of use are promoted by both the ability of these devices to operate at high temperature, and to switch quickly.

4.2.3.3. *A high speed to saturation*

Under strong electric field (over some 10^5 V/cm), the drift velocity of electrons and holes tends towards a limit value. This *saturation speed* v_{sat}, which is twice as fast with silicon carbide, is still in its favor compared to silicon, for application on power components working at a high frequency.

Merit factors	3C-SiC	6H-SiC	4H-SiC
JFM / JFM (Si) *where* $JFM = v_{sat}^2 E_c^2 / 4\pi^2$	156	215 ($\perp$c) 2 ($\|\|$c)	260 ($\perp$c) 6 ($\|\|$c)

Table 4.5. *Merit factors by E.O. Johnson for common polytypes of SiC, divided by values for silicon (notations and values of physical parameters from Table 4.2 were used for these calculations)*

An idea of the expected gains is rendered by Johnson's figure of merit of (JFM [JOH 63]), whose values are presented in Table 4.5. These performance gains are very important, especially for the two hexagonal polytypes, when the electronic conduction is perpendicular to the axis of growth c.

4.2.3.4. *A high thermal conductivity*

Losses in the components (both during their conduction or commutation phases) are an internal source of heating. When they cannot (for one physical intrinsic reason), or should not (to meet their immediate environment) work beyond a certain temperature, the ability of the device to dissipate heat is a desired quality, starting with the semiconductor itself. The latter is also appreciated when the structure is sensitive to the presence of hot spots, to reduce the temperature deviations by spreading better heat fluxes. With a thermal conductivity about three times higher than that of silicon, silicon carbide offers prospects for improvement in this regard.

4.2.3.5. *More generally (at the system level) and abstract*

The benefits of using silicon carbide as the basic material for the manufacture of components for power, have been mentioned above:

– the rise of voltage;

– the rise in temperature;

– reducing the size;

– minimizing losses;

– the increasing frequency;

– the rising power.

These gains at the component level obviously have an impact on the performance of the system into which the component will fit. In particular, silicon carbide allows for the consideration of a greater density of system integration with smaller components, whether active or passive (including inductive elements working at higher frequencies), and the prospect of less complex systems (with fewer series or parallel connections, or simplification of the problems of adaptation of impedance, or problems of cooling, etc.).

In summary, considering the elements presented above, silicon carbide satisfies theoretically the first clauses for an alternative solution to replace an existing and already very well established solution: to obtain a significant gain on the performances of many systems. We will further see that sectors previously out of the reach of silicon may even be involved.

4.2.4. *Other "candidates" as semiconductors of power*

In fact, outside the silicon, only gallium arsenide (GaAs) is the subject of sales of slices (up to 150 mm diameter), and the market for telecommunications systems implementing GaAs components is booming. however, this material progress appears inadequate next to that of silicon, and to the needs of power systems to allow a significant place for this material.

Other semiconductor materials, such as diamonds, or some nitrides, particularly GaN, are also alternatives that are currently being researched [CHO 00], because they present the potential for a major increase in the level of performance for power electronics, sometimes earning well above what has been described for SiC. Nevertheless, they do not comply with yet another essential clause for the emergence of a new industrial application: the availability of mono-crystalline

substrates of sufficient size and quality. The major obstacles have not yet all been removed in terms of the mastery of basic techniques required for the achievement of a semiconductor component on the basis of these materials, such as control of the conductivity (type N or P) by doping, etching, metallization of contacts, filing of dielectric or encapsulation.

Instead, the maturity of the technology in the industry based on silicon carbide, especially for 6H and 4H polytypes, is already sufficient to enable the emergence of the first power components on the market. The following section gives state of the art expertise on the components acquired at various stages of manufacture, as well as on the main areas of current research.

4.3. State of the art technology for silicon carbide power components

In this section we briefly describe, as a priority, the techniques adopted by the industry, or most commonly used by research centres. The technology of silicon is mentioned to highlight the differences or the similarities between the two chains.

The characteristics able to assess the level of quality achieved at each stage of the development of a component are mentioned. Those characteristics likely to have an impact on the proper operation of the devices are primarily selected, in order to understand their performances in the final part. We are also trying to provide an overview of the derivative of progresses.

4.3.1. *Substrates and thin layers of SiC*

Three among many identified polytypes of silicon carbide, were able to be synthesized in the form of massive monocrystalline materials, used in the manufacture of electronic components: they are chronologically 6H-SiC, 4H-SiC, and very recently 15R-SiC. These materials are prepared to be used as substrates, on which thin films are implemented for devices realization. Only substrates 6H-SiC and SiC-4H, epitaxial or not, are commercially available. Note that 6H-SiC N-type also has a broad market potential as a GaN substrate for the production of electroluminescent components.

As this section reports, synthesis techniques of SiC are much more sensitive than those of silicon, this justifies the historical difficulties, and suggests that the cost of this type of material is likely to remain high.

4.3.1.1. *Monocrystal growth for the production of substrates*

4.3.1.1.1. Roles and qualities expected

The substrate serves mostly as mechanical support around which will be deposited the various films (single-crystal film, insulation or metal) to make the final device. In silicon technology, when the voltage rating requires a layer of semiconductor very thick and lightly doped, it can be produced by the substrate itself. In all cases, the structural properties, electrical and thermal, of this substrate are very important, as an integral part of the structure.

4.3.1.1.2. Technical production and marketing

The commercialization of the SiC material dedicated to microelectronics began in the USA in 1989. The company CREE Research proposed slices of 6H-SiC of 25.4 mm in diameter. Today several vendors ([CRE 01a], [STE 01], [OKM 01], [NIP 01], [SIX 01], [SICr 01]) of platelets of 6H SiC up to 76.2 mm diameter and 4H-SiC up to 50.8 mm diameter are present on the world market (Finland, Japan, Germany, and always the USA).

The most common growth technique is based on the vapor phase transport of the chemical species involved, obtained by sublimation of a source of SiC material in the 2,200-2,500°C range, therefore high if the reference is once again that of silicon, followed by condensation on a germ of monocrystalline SiC, introducing the polytype desired. The germ is placed near the source and brought to a temperature slightly below the temperature of the source (the pressure inside the crucible is in the order of 10 to 50 Torrs). The speed of growth by this technique is in the order of several mm/h.

A monocrystalline ingot of a few centimeters in height is obtained by this method, also known as the “Lely modified” (originally discovered by Tairov and Tsvetkov [TAI 78]). The ingot is then rectified in the form of a cylinder to provide slices after sawing and polishing (which are non-trivial steps because of the hardness of the material).

4.3.1.1.3. Current characteristics

In addition to controlling the polytype (by the nature of the germ), the growth of massive SiC by this technique allows control of the size, structural quality and electrical conductivity of the substrate produced.

In regards to the crystalline quality, which has been making constant progress in recent years, typical values and best results characterizing the major flaws existing in the marketed silicon carbide substrates are presented in Table 4.6. Only those defects inducing an impact on the quality of epitaxied films on these materials are

cited. (For example, parallel dislocation loops to the base plane of the substrate, present in very high density but which do not propagate in the epitaxial layer, are not included in Table 4.6 [NEU 00].) It is also known that the material still contains many chemical impurities.

The resistivity of the semiconductor is also controlled for the growth of the monocrystal, by incorporation of doping atoms (nitrogen for N and aluminum for P). The heavily doped substrates required for the manufacture of components for power electronics, have resistivities that vary between suppliers. We can find, for example, 15-30 mΩ.cm for the 4H-SiC N-type and 2.5-8.5 Ω.cm for 4H-SiC P-type (corresponding to the doping of some 10^{18} cm^{-3}). Several substrates 6H-SiC or 4H-SiC, semi-insulating materials, are also available from some manufacturers, primarily dedicated to the market of power microwave components. The resistivities in these cases are above 10^5 Ω.cm.

It should be noted that the thermal conductivity of the material is affected by the crystalline quality: it is typically 3 to 3.8 W/cm.K (at room temperature) for the traded substrates, compared to 4.9 W/cm.K measured for the purest substrates (produced by Lely's method).

Type, nature of defects	**Density or % of the surface of the substrate**
Micro pores (or dislocation opened screw)	< 30 cm^{-2}
dislocations closed screw	3,000 cm^{-2} to 10,000 cm^{-2}
Hexagonal form plates	< 10 %
Small growth cavities (orange skin)	< 10 %
inclusions (polytype 3C, ...)	< 5 %

Table 4.6. *Typical data from CREE [CRE 01a] for SiC substrates (50.8 mm diameter) of "Production" quality (qualified area corresponds to the whole surface of the slice, excluding a border of 2 mm width)*

4.3.1.1.4. Avenues of research

The process of growth is the subject of much research to improve the ingot's quality [ANI 99]. Further progress is required to reduce the density of defects in large-diameter substrates, in order to increase yields and reduce manufacturing costs, both of the base material and components that will use it. Diameters of up to 100 mm have been demonstrated in the laboratory, along with micropore densities of less than 1 cm^{-2}. With regard to this type of defect, Figure 4.4 [HAR 01]

illustrates the evolution of their presence in recent years, as well as the changes expected for the future: according to these forecasts, obtaining the required densities for the production of large-scale power components (for ratings in currents beyond 100 Amps) should occur around 2005.

In parallel to these studies for optimization by the "classical" method, alternative techniques provide material of good crystal quality, such as chemical vapor deposition at high temperature (HTCVD) [ZHA 01], or liquid phase epitaxy (LPE) [REN 98], are investigated, with the goal of increasing their deposit rates (which are currently in the order of several hundred μm/h). We would like also to mention that the HOYA Corporation [HOY 01] has presented at the International Conference ICSCRM 2001, a slice of 3C-SiC of 100 mm diameter, produced by hetero epitaxy on a silicon substrate, eliminated thereafter [NAG 01]. The main characteristics of this material are a thickness of 200 μm, a density of crystalline defects less than 10 cm^{-2} with no micropores, and a level of doping (N or P type) from 10^{15} cm^{-3} to 10^{19} cm^{-3}. 3C-SiC substrates are even marketed at a very attractive price.

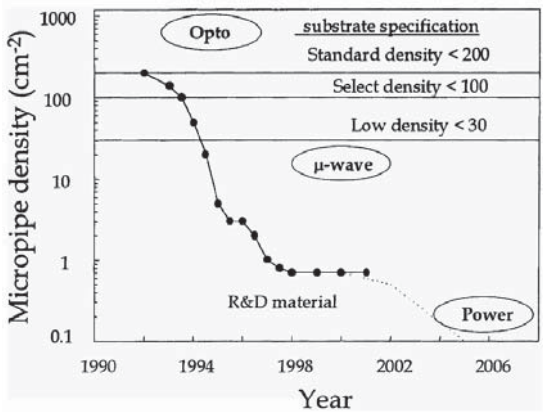


Figure 4.4. *Temporal evolution of the defect density of micropore type, in substrates elaborated in laboratories by the "modified Lely method" (figure from [HAR 01]). The authors indicate the required levels for commercialization of optoelectronic components, microwaves or power, together with specifications of substrates by the supplier CREE*

4.3.1.2. *Obtaining monocrystalline thin films*

4.3.1.2.1. Roles and expected qualities

The active parts of a component are generally in "thin" semiconductor layers filed to that effect on the substrate. This substrate typically has a thickness of 350 μm, which is necessary to give an overall mechanical rigidity sufficient for

manipulation. The N-type or P-type layers needed for the construction of the component, in fact, have a thickness which can vary over a wide range (orders of magnitude ranging from 100 nm to the nearest hundred μm). This thickness, which depends on the role of the layer within the component and also the voltage rating of the device must be controlled precisely. Another important feature if the deposited film is to be controlled finely is its resistivity. In addition to these two quantities, the quality of the crystal layer, must be uniform over the entire surface of the layer. The number of suppliers of epitaxial substrates is smaller than that of simple substrate providers. Some component manufacturers also have their own in-house source.

4.3.1.2.2. Techniques

In this section, we will consider the homoepitaxy of 6H-SiC and 4H-SiC by CVD, which is the only technique used industrially today. We also discuss homoepitaxy of 3C-SiC and the postponement of SiC films on various substrates, for the economic interest they represent, although these processes are still at the research stage.

Homoepitaxy

The technique currently used by industry is the chemical vapor deposition. The growth takes place at a temperature between 1,400°C and 1,600°C, sweeping a gas rich in species Si and C, on a substrate with a disoriented surface from the axis c [KOR 98].

This disorientation of the surface (from 3.5° for the polytype 6H, and 8° for the polytype 4H) provides an homoepitaxial layer without inclusions of parasitic polytypes (epitaxy called “steps control “). The mastery of the process also helps to prevent the increase of micropore densities and other dislocations compared to those of the starting substrate.

The growth rate is relatively low (2 to 5 μm/h) for basic systems, but heavy thicknesses are available thanks to the new hot-wall systems allowing high velocity deposition (50 μm/h).

The unintentional conductivity of the films produced by this process is N type, with a level of residual doping between 10^{13} cm^{-3} and 10^{14} cm^{-3}. The mastery of the resistivity is in a range of 10^{15} cm^{-3} to 10^{19} cm^{-3}, and is produced by the incorporation of the doping impurity in the gas source (nitrogen to get the type N and aluminum for the P-type) during the epitaxy, and control of the mechanism of site competition [LAR 97].

The commercial buildings have improved the uniformity of thickness and doping layers (typically equal to 10% for doping) by rotating platelets in the flow of gas,

while allowing for the simultaneous processing of multiple wafers [EPI 01]. It is worth noting, however, that uncertainty about the actual value of the thickness of a commercial epitaxy remains high (up to 25% if less than 1 μm, and 10% if over 10 μm), and that the constancy of doping throughout the thickness of a layer is not specified. This can be a significant source of error in assessing the performance of a component, in particular whether it should be "high voltage".

The lifetime of minority charge carriers is a highly sensitive parameter to the purity (structural, chemical) of the semiconductor, and also critical for the smooth operation of bipolar components. The maximum values published for the lifetime of holes in the thick SiC epitaxies have increased in recent years, in agreement with the simultaneous improvement of the quality of substrates and epitaxies, reaching levels in the order of several microseconds [KOR 96]. We will see in section 4.4 that these materials allow for bipolar devices (diodes) with low differential series resistance, and high speed.

The various possible consequences of the present imperfections of epitaxies (mainly induced by the substrate) on the final characteristics of power components are under investigation. Some are already well known, like the premature breakdown of the components due to the micropores, which propagate from the substrate through the thickness of the epitaxial layer. The best current densities of these defects (1 cm^{-2} for substrates of 50.8 mm in diameter, see Table 4.6) already allow for the use of some high-voltage devices sized in the order of 10 mm^2. The polytypes inclusion, or surface defects, will also affect the inverse characteristics (blocking of bipolar junctions or Schottky) or direct characteristics (channel conduction of MOSFET transistors). The frequency of these defects is already relatively low and on the decline. However, the screw dislocations present in much higher densities (also spread throughout the thickness of the epitaxy) worry today's designers more because of their impact on the current and electrical behavior in the vicinity of the breakdown voltage. While it has changed little in recent years, a dislocation density of less than 1,000 cm^{-2} would be required to obtain power components. It should be noted that the silicon wafers, which are at the foundation of existing devices, have dislocation densities within this order of magnitude.

In addition to a constant search for improving the chemical and crystalline quality of epitaxial films (but first of all through an improvement in the substrates), the concerns of scientists focus on increasing deposit rates, while preserving the control and uniformity of low doping (about 10^{14} cm^{-3}), with the main objective of meeting the needs of power electronics. The technique of chemical vapor deposition at high temperatures (up to 2,000°C), must also be mentioned, with which growth speeds as high as 800 μm/h were obtained [ELL 00].

Other techniques (at the research stage)

Because good quality substrates (6H-SiC, 4H-SiC) are expensive and small (though the latter tends to reduce grievance), or because they are still lacking (as for 3C-SiC), the search for obtaining monocrystalline of SiC films on various other substrates have continued.

Homoepitaxy by heteroepitaxy

The absence of substrates (except of small ones, mainly of 6H polytypes, obtained by the Lely method), largely contributed to research efforts into heteroepitaxy of SiC on silicon, with first interesting results appearing at the beginning of the 1980s [NIS 83]. The obtained polytype was 3C-SiC, which has the lowest disagreement mesh with Si.

The physical properties of this polytype (particularly in terms of mobility of carriers), have kept the interest of this research despite the emergence of 6H-SiC substrates onto the market in early 1990. Today, the main interest of such research into power electronics, while substrates and thin layers of 4H-SiC are available, is primarily economic (reduced cost of silicon and manufacturing stages on this substrate of "standard" size). The 3C-SiC materials owns good factor of merit (as shown in section 4.2) relating to obtaining vertical conduction, and fast devices. Applications outside the field of power electronics (particularly as sensors in hostile environments – temperature, radiation) also contribute significantly to the research efforts.

Due to differences in parameter mesh (of 20%), and coefficients of thermal expansion (8%), the films of 3C-SiC deposited on silicon contain crystalline defects in large quantities, even when a preliminary step known as "carbonization" of the silicon surface is included [MAT 88]. Some of the defects annihilate during growth, and beyond a thickness of about 5 μm, the monocrystal is homogenous, but the density of defects is still about 10^8 cm^{-2}. Growth temperatures of above 1,000°C are necessary to prevent the incorporation of micro-crystals into the layer of SiC. In addition, these films suffer important constraints that curve the substrate, or even cause cracks [CHA 01]. Thus, the electrical characteristics of the layers of SiC-3C are degraded.

Homeopitaxy by postponing thin layers

A more recent form of research, with the same economic concerns, applies the Smart-cut process (developed by LETI/CEA [BRU 95] in conjunction with SOITEC), to provide reports on the surface of a substrate A (preferably low cost and standard dimensions): a thin layer of silicon carbide cut off on the surface of a monocrystalline substrate B. This process was first tried with success from wafers of 6H-SiC on silicon substrates [DIC 96].

The process applied to the silicon carbide is, as a first step, establishing a strong dose of hydrogen on the surface of sample B (SiC), in order to create a weakened plan, to a depth determined by the energy of implantation. The established face of this sample B is then pasted (by molecular accession) to sample A. A proper separation process (e.g. thermal), generally applied, causes a cut in the B sample to the depth of implantation, separating it from the SiC thin film transferred to sample A. Sample B can then be recycled to provide a new film of silicon carbide.

When an insulating gluing interface (for instance, SiO_2 or Si_3N_4, etc.) is used, in order to form a structure called "SiCOI", the target is in addition to combine the advantages of silicon carbide and those of structures on insulator. The purpose (for power electronics) is to obtain lateral power components, or even to have an adaptive technology to achieve power integrated circuits, if the characteristics of the material transferred and of the devices which can be made permit it. The optimization of the process has now reduced the level of compensation for N-type films (resulting from the implantation of hydrogen). At the moment, 6H-SiC or N-type transferred 4H films, used for the creation of components, have a thickness between 0.5 μm and 1 μm, and a concentration of acceptor-type defects of less than 4×10^{16} cm^{-3} [HUG 00].

When a metal interface bond is chosen, the hetero structure is created in the hope of achieving power components with vertical conduction from a "quasi substrate" of cheaper silicon carbide, called "QuaSiC" [LET 01]. The possibility of obtaining a coat of mono crystalline 4H-SiC, 8 μm thick, created by homoepitaxy on a thin film previously transferred on a substrate of polycrystalline SiC (the bonding interface used is WSi_2) has been reported.

4.3.2. *Technological steps for achieving power components*

Once the required piling of thin layers on the substrate, necessary for the achievement of a component (for example: N^- epitaxial growth on N^+ substrate to get a Schottky diode, or P^+ on N^-, on N^+ substrate for a bipolar diode, or P^+ on N on P^-, on substrate N^+ for a thyristor, etc.) has been achieved, a number of technological steps are necessary to complete the chosen structure and allow it to be connected and integrated into a box or a system ensuring its operation.

Two techniques traditionally used for silicon can also be used by manufacturers creating components based on SiC: these are *wet etching* and *doping by localized impurity diffusion* through a mask. Despite these two features, it was not required, in general, to develop specific equipment: the processing of wafers of silicon carbide largely benefited from the know-how and facilities developed, and became the industry standard for silicon (for example, wet etching installation, implementers,

but also oxidation or deposition installations, photolithography, etc.). Other examples are the characterization and analysis techniques that have accompanied them. This has contributed to the rapid progress of research on the components, allowing for the early opportunity to experimentally test most of the known architectures. However, great efforts have been made to develop procedures adapted to the new semiconductor, especially with regard to temperature and duration of treatment (for oxidation and ion implantation, etc.), the chemical nature of the elements (gas, dopers, metals, insulators), which are often redefined and optimized. The small size of SiC substrates also intervened significantly in the development of these procedures. An exception must however be mentioned: the stage of post-annealing used for ion implantation doping of SiC implements specific furnaces, as high temperatures are required.

The following sections will review the key steps for the successful implementation of a power component of silicon carbide, in order to clarify the state-of-the-art features that underlie the performances of modern demonstrators (the results shown are for polytypes 6H and 4H).

4.3.2.1. *Etching*

4.3.2.1.1. Roles and qualities expected

The etching of the semiconductor is an indispensable tool, used for many purposes, such as surface treatment, the attainment of trenches, resuming buried contact, and achieving periphery (mesa), etc. Unlike in the case of silicon (or amorphous silicon carbide), the attack by wet chemistry is ineffective for a material with a high binding energy like SiC (except by molten salt at temperatures above 500°C, using unsuitable techniques for an engraving to be selective, not contaminating the structure, etc.). In the early 1980s the dissolution of this technological blockage contributed, alongside the discoveries of a method of controlled growth ("LELY amended") and a process of hetero epitaxy for 3C-SiC on Si, to renew interest in this semiconductor. This is due to the advent of plasma etching systems (developed to improve the sharpness of definition of the grounds on silicon), which were used successfully to attack SiC. Good control of the speed of etching, its selectivity towards masks and the state of the etched surface (physical, chemical and morphological) is usually required for this step.

4.3.2.1.2. Techniques and current features

The dry etching simultaneously results from a chemical attack and a physical attack, respectively caused by the presence of neutral reactive species in plasma (fluorine or chlorine, which react with Si, and oxygen that reacts with C, etc.) and ions accelerated to the surface to be etched (Ar^+, etc.). The "high density" etching systems of the latest generation (with a high concentration of ions) allow for etching

speeds of 100 nm/min. These speeds are sufficient to build most of the component structures, provided there is a material masking not eliminated (or distorted) throughout etching SiC. The etching selectivity represents this quality as the ratio of the attack speed of the material to be etched and that of the mask, as presented in Figure 4.5.

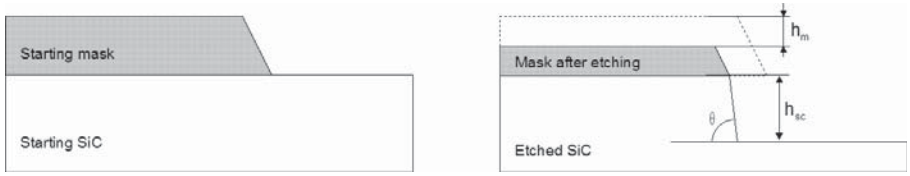


Figure 4.5. *Representation of SiC etching with an angle θ. The mask is represented in gray. After etching, the original mask is represented by the dotted line. Etching selectivity is V_{sc}/V_m, with $V_{sc} = h_{sc}/d$ and $V_m = h_m/d$, for an etching duration d*

The various natures (and *selectivities* of etching) of the most commonly used masks are: aluminum (> 20), silica (from 1 to 6 depending on the quality of SiO_2 and chemical attack process), and resins of photo litho etching (0.3 to 0.4 [MER 01]). The very low speed attack of aluminum compared to that of SiC authorizes deep engravings, with relatively vertical walls. Selectivities much lower (as in the case of SiO_2) can be restrictive in terms of depth of attack, according to the feasibility of filing a thick mask. Nevertheless; they are used for obtaining etching flanks with a slope angle (angles from 30° to 80° from the horizontal, with a depth of etching of SiC of 3 μm [LAN 96]) around 5° tested on 5 μm [MER 01]).

The research focuses on achieving deep engravings, with controlled angle and quality etching flanks.

4.3.2.2. *Selective doping by ion implantation*

4.3.2.2.1. Roles and expected qualities

Selective doping is essential to achieve planar devices (i.e. without relief from the surface of the semiconductor), whether for the creation of emitters P^{++}, grids P, N^{++} sources, contacts (N^{++} and P^{++}), or peripheral protections (P or N^{+}). For the latter aspect of peripheral protection, the ion implantation is also sometimes used to locally make amorphous the semiconductor surface. Here we will only address the application concerning doping, which is to create boosted regions in a range of concentrations ranging from a few 10^{16} cm^{-3} to 10^{20} cm^{-3}, preserving a good crystalline and chemical quality, in the volume and on the surface.

4.3.2.2.2. Current techniques and features

The ion implantation followed by annealing is the only feasible technique for localy doping silicon carbide (because of the prohibitive temperatures required for doping by diffusion of doping impurities). Typically, the bombing serves to incorporate the ionic doping impurities in the material at a depth dependent on the energy transmitted to the ions, the size of these, the density of the target, and its crystalline orientation from the incident beam. The high density of silicon carbide (see section 4.2.2) will result in shallower penetrations than in the case of silicon with a given implantation energy and impurity, when the direction of implementation is misaligned from any crystallographic axis. Note, however, that the structure of SiC promotes a secondary pipeline, which could lead to the creation of deformed and little steep junctions with a tail of the implementation profile. This phenomenon is more difficult to avoid than in the case of silicon [MOR 99].

Because of the very low mobility of doping impurities in SiC (their coefficients of thermal diffusion being very small), the spatial distribution of implemented impurities is generally not changed during the post-implantation annealing (boron is an exception, which has a circulation assisted by defects), while this phenomenon is often exploited in the case of Si (although also sometimes has detrimental effects). Multiple implantation with high energy (or more rarely intentionally channelled implantations) is usually implemented to achieve junctions or deep boxes (i.e. beyond μm) in SiC.

The post-implantation annealing is nevertheless essential to rebuild the crystal damaged during the ion bombardment, and make the implanted impurity migrate to a site for replacement of an atom of the network, so as to be an electrically active doping. In SiC, some generated defects are particularly stable. Accordingly, it is important to minimize the degree of damage of the crystal. To do so, a hot implantation is generally used when the level of referred doping requires a dose above the threshold which makes the material amorphous at room temperature. It also follows that temperatures during the consequent annealing need to be much higher than those usually used (especially for the P-type doping). These high temperatures (at least 1,700°C for Al) also require good atmospheric control to maintain a suitable surface on the samples. Specific ovens or techniques to the SiC industry are needed for this step.

	N-Type				P-Type	
Nature of impurity	**Nitrogen**		**Phosphorus**		**Aluminum**	**Bore**
Atomic mass (u.a.m)	14.003		30.974		26.982	11.009
Ionization energy (E_A , MeV)	***h***	***c***	***h***	***c***		
for 6H-SiC	81	140	85	135	200-250	285-390
for 4H-SiC	42	84	53	93	191-230	300-400
Ionized impurities at 25°C (for $N_{A,D} = 10^{19}$ cm^{-3} and $N_{comp} = 5x10^{15}$ cm^{-3})	70% (E_A=0.08eV)		#70% (E_A=0.08eV)		2% (E_A=0.2eV)	0.15% (E_A=0.3eV)
Orders of magnitude of the depth of implantation (µm). Examples for:						
– classical energy: 200 keV	0.3		0.18		0.22	0.39
– high energy: 1 MeV	0.92		0.8		0.95	1.14
Threshold to be amorphous at room temperature (cm^{-2})	4 x 10^{15}		~2 x 10^{15}		~10^{15}	5 x 10^{15}
Implantation temperature (°C)	RT – 1000		RT – 600		RT –850	RT – 700
Annealing temperature (°C)	1,300-1,500		1,300-1,700		1,500-1,800	1,500-1,800
Resistance/square (Ω/□) (examples, for 4H, at T_{amb})	285 [RAO 98] (N : 2.5x$10^{19}$$cm^{-3}$, thickness: 0.4 µm)		110 [HAN 00] (P: 1x$10^{20}$$cm^{-3}$, thick: 0.45 µm)		285 [KIM 01] (Al : 1.6x$10^{20}$$cm^{-3}$, thick: 0.25 µm)	Very high

Table 4.7. *Characteristic quantities for the doping impurity, doping process, or the layer of SiC implanted and annealed*

Table 4.7 presents the dopings which are currently used by technologists, and some characteristics of impurity, process, or either the implanted and annealed layer. Aluminum and nitrogen are respectively P-type and N-type doping, encountered in the majority of devices because they have low ionization energy compared to other impurities. While the minimum values of the N-type layers resistance implanted with nitrogen are close to the values obtained on Si [RAO 98], those of the P-type layers doped with aluminum remain very high [KIM 01].

For the P-type doping, boron is also used: its small size facilitates its incorporation. The threshold for amorphous is higher and implanted profiles are

deeper for the same acceleration energy when compared with Al, especially since during the post-implantation annealing, this impurity displays the ability to disseminate significantly, beginning at 1,400°C. However, dissemination occurs in all directions, especially to the surface (exodiffusion) [LAU 99], making the control of the incorporated dose difficult [TRO 97]. More rarely, phosphorus is used for the N-type doping, due to the improved values for electron mobility, leading to a lower resistance per square.

Finally it must be noted that an ionization energy similar to aluminum (especially that of boron) leads to an incomplete ionization of doping on a large portion of the range of operating temperatures covered. This represents an additional factor (compared to the case of silicon) and a very important consideration for the prediction or analysis of trends in temperature performance of SiC devices. The bipolar structures with a P^+-type emitter, which is dependent on an efficient injection of holes, are in particular affected by this consideration, as may be found in section 4.4.2.

4.3.2.2.3. Research avenues

The progress to be achieved thus lies in improving control of profiles and levels of doping, especially in the case of strong doping and P-type. From the viewpoint of implantation techniques, research teams work in particular on the implantations at high energy, to reduce damage to the crystal and therefore make it possible to increase the implanted doses [TAK 98]. The co-implantation is also considered to improve the incorporation of Al and B in substitute sites [OSH 01]. Finally, the channelled implantation (oriented along a preferred crystallographic axis) is a line of research seeking to increase the depths of implantation, while reducing damage to the crystal.

From the viewpoint of the annealing process, many studies are conducted to improve the electrical activation of doping and the quality of the crystal, not only in volume but also on the surface. For this, quality depends not only on that of doping, but also the success of subsequent manufacturing steps such as etching or more thermal oxidation. Different techniques (such as, induction furnaces [LAZ 00] or pulsed annealing [PAN 01], etc.) and various configurations of environment of samples were studied.

4.3.2.3. *Oxidation, and deposition of insulation*

4.3.2.3.1. Roles and expected qualities

Different functions involving the presence of an insulator in contact with the semiconductor within the components include passivation and surface protection,

insulation between the electrodes or between semiconductor areas, insulation of command grid, etc.

The silicon industry exclusively uses the product of silicon thermal oxidation, SiO_2 for insulation. The excellent properties of this insulator on silicon (also accessible by certain deposit techniques) have been one of the key factors in the development of microelectronic applications based on silicon. As the thermal oxidation of silicon carbide also produces silicon dioxide, the same functions of insulation and surface passivation are desired for SiC based components. There is therefore much work towards development and optimization, as was the case for silicon. The difficulties encountered today in obtaining good electronic properties at the interface (low charge density and interface statements) are reminiscent of those encountered at the beginning of development for the MOS on silicon.

However, specific features of SiC (its nature or future use) cause new issues to arise, which require research into new methods for making SiO_2, or investigations on other insulators. The current state of knowledge is summarized here. A comprehensive and recent review [RAY 01] on this key issue can be accessed for more details.

4.3.2.3.2. Thermal oxidation (and depositing silicon dioxide)

As with silicon, the chemical reaction (in the presence of O_2, wet or dry, activated by temperatures from 850°C to 1,150°C) leads to a consumption of the semiconductor thickness equal to 45% of the thickness of the resulting SiO_2. As on silicon too, the volume properties of that oxide are a refractive index of 1.45, a very good dielectric strength of 10 to 12 $MV.cm^{-1}$ (if obtained on dry material of good crystalline quality) and a low resistivity in the field of 10^{14} $\Omega.cm^{-1}$. We can therefore consider this technique in terms of the same goals, namely mainly cleaning and polishing the surface by sacrificial thermal oxidation (for manufacturing techniques) and creation of an insulator (at component level, as isolated grid or protection of surface or insulation cabinet, etc.).

Note however that the use of SiO_2 as insulation on SiC must take into account that the maximum values of the electric field, inside a component that are optimized to take advantage of the strengths of silicon carbide, become similar to the magnitude of the breakdown field of SiO_2. This is a new situation for the designer accustomed to the values of electric fields in Si, which remain some 20 times lower than the critical threshold for SiO_2. This will also have repercussions on the architecture or on conditions of use of components employing SiO_2 as insulation.

Among the differences affecting the technological level, the first to be reported concerns the kinetics of oxidation which is much slower for SiC than for Si (for example, in the order of 10 nm/h by dry oxidation at 1,150°C, and for Si in the order

of magnitude of 300 nm/h by dry oxidation or 4 μm/h during wet oxidation at 1,100°C), which will restrict the ability of this process to achieve preferably thin oxides, such as grid oxides or primary passivation. While remaining of the same order of magnitude, speed of growth of the oxide on a given polytype of SiC varies significantly depending on the crystalline orientation of the surface (kinetics is the fastest on face Si, slowest on face C, and intermediate on the other sides), and its level of doping. Note also that a damaged crystal (for example, by an ion implantation) oxidizes more easily than the blank crystal, in particular the oxidation of amorphous silicon carbide is much faster than mono crystalline SiC. To obtain relatively thick layers or uniform thickness over a surface with regions of different types, processes for implantation of SiO_2 previously developed for Si are used (for example, to make ion implantation masks or plasma etching).

The second difference is a current difficulty that exists when dealing with the quality of the interface between SiO_2 and SiC. This is lower than that obtained on silicon, in terms of effective charge density and the density of interface states, as well as potential fluctuations in the interface, this includes the quality of "first choice" commercial material. These three quantities (the values still widely dispersed) are indeed usually greater than those obtained today with silicon. Wet oxidations at a temperature exceeding 1000°C and some processing of the surface before oxidation, and annealing after oxidation, have recently helped to reduce them [LIP 98]. In general, it is noted that oxides on the silicon face of SiC exhibit an effective charge density lower than that of the carbon face (best value: $2x10^{10}\,cm^{-2}$). The density of interface states, remains currently higher on the 4H-SiC polytype [AFA 00] (around $10^{12}\,cm^{-2}.eV^{-1}$). And what is more, implanted P-type materials are penalized even further. Now the MOSFET in 4H-SiC with N channel inversion in an implanted P box is expected to be "flagship" structure achieving SiC transistors (as shown in section 4.2.3.2). Apart from non-ideal threshold voltages, these structures suffer from an apparent mobility of the electrons in the channel inversion, well below its theoretical value of temperatures around 150°C (the gap is reduced when temperature increases). The channel mobility of electrons is generally less than $25\,cm^2.V^{-1}.s^{-1}$ for SiC-4H at room temperature, while being two to three times greater for SiC-6H. The interface statements of acceptor type located at energy levels very close to the bottom of the conduction band [SCH 99], as well as the sharp fluctuations of the surface potential [OUI 97], seem to be recognized today as contributing to the high resistivity of the inversion channel. The deposited oxides do not solve this major problem (which is explained by, and confirms, the fact that the disorder derives mainly from the interface rather than the volume of insulation).

A third difference lies in the values of height barrier potential between the conduction bands of SiO_2 and the semiconductor, which are much lower with SiC than with Si (the same is true among their valence bands), as shown in Figure 4.6. These values, which are reduced when the temperature increases, facilitate the

injection of carriers in the presence of an electric field. The undesirable consequences manifest in terms of the reliability of MOSFET structures, which is increasingly affected while the operating conditions are expected for use at high temperatures, and while this architecture of the component does not preserve the oxide from the large electric fields, that can handle silicon carbide. In addition, the current crystalline quality of substrates and epitaxies of SiC is probably still the cause of premature breakdowns of SiO_2 on SiC, under strong field and high temperature (as was formerly the case with silicon), also leading to reduced MOSFET structure lifetimes on SiC compared with those on silicon.

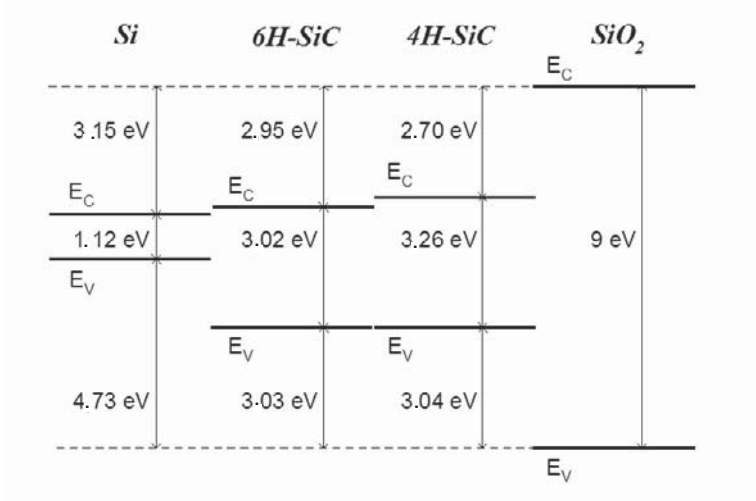


Figure 4.6. *Diagrams of energy band at 300 K for Si, SiC-6H, 4H-SiC and SiO_2 showing the reduction in height of the barrier when the gap of the semiconductor increases, facilitating the injection of carriers into the insulation [AGA 97]*

The physical nature of elements at the root of these electric events (for example, disorder at the interface, or low lifetime, etc.) is not fully clarified (for example, SiC crystal purity, clusters of carbon and surface roughness). A significant part of current research is trying to elucidate this [AFA 99] [AMY 01], and offers treatments [RAI 01] [KRA 01] in order to obtain a SiO_2 film quality compatible with the expected performance of power MOSFETs based on SiC. Without further delay, work is also focused on the architecture of the component itself, in order to circumvent this difficulty (examples will be provided later on in this chapter). At an intermediate level, some research, described below, is focused on alternative insulation that would allow the achievement of insulations for grid control or surface passivation better suited for SiC material.

4.3.2.3.3. Other insulators

A triple stack of oxide and silicon nitride (ONO) is the only insulation currently discovered that leads to both a significant improvement in the threshold voltage, and in the lifetime at high temperature (ten days at 335°C) under a grid field of 2 MV/cm for MISFETs (horizontal structure on P epitaxy, with source and drain implanted in nitrogen). The breakdown electric field of the insulation is also higher (14 MV/cm) [LIP 00].

Some groups are interested in AlN, because of its dielectric permittivity which is similar to that of SiC, and a theoretical breakdown field in the same order of magnitude as SiO_2 (very high). A1N also has a good agreement of mesh with SiC, good thermal conductivity, and a good temperature strength. The maximum electric field of breakdown is currently measured at 3 MV/cm (by MOCVD filing), however, the experimental leakage currents remain prohibitive [LEL 00].

4.3.2.4. *Metallization*

4.3.2.4.1. Roles

During manufacturing of the component, metal depositions may take place (to make etching, or implantation masks, etc.). In the finished component, metals deposited on the semiconductor are intended to provide either an electrical connection with ohmic contact, or a junction via Schottky contact. Placed on top of an insulator, they can also take the role of the grid driving the switch; field plate, for the peripheral protection of a junction; or an interconnection path. We present here only the state of the art of features of ohmic contacts and Schottky on SiC, whose properties (e.g. height of barrier and thermal stability, etc.) are dependent on the state of the interface metal/SiC, and on the nature of metals and reactions.

4.3.2.4.2. Schottky contacts and current features

As recalled in Figure 4.7a, the junction between a metal and a semiconductor produces a potential barrier, called the Schottky barrier Φ_B, which may display a rectifying behavior. A low doped semiconductor, moreover presenting a large gap, promotes obtaining a rectifier contact, also known as a Schottky contact (case of Figure 4.7b). In this way, many metals form a Schottky contact simply by layering upon SiC.

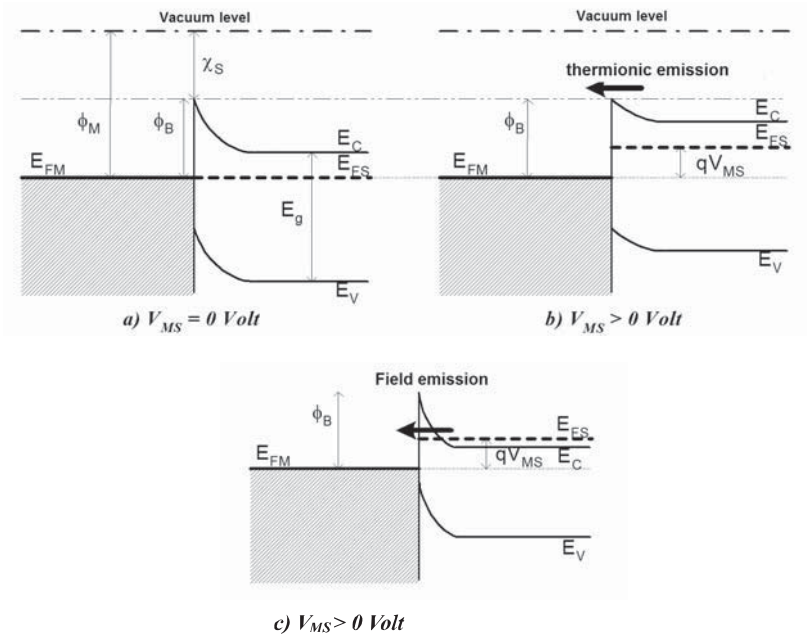


Figure 4.7. *Diagrams of energy band of a metal/semiconductor contact:*
a) Ideal case of a Schottky barrier, such that $\Phi_B = \Phi_B - \chi_S$
b) Schottky contact on lightly doped n-type semiconductor: only the electrons able to overcome the barrier height will participate to the current flow
c) Ohmic contact on highly doped n-type semiconductor: electrons flow across the thin barrier by tunnel effect

The height of the barrier Φ_B depends on the nature of the deposited metal, on the semiconductor (since ideally the barrier is equal to the difference between the work output of metal, Φ_M, and the electronic affinity of the semiconductor, χ_S, according to the Schottky-Mott relationship) and also on the chemical and structural condition of the semiconductor surface (of the polytype, its surface orientation – face C, face Si, or another face; the presence of a native oxide; or surface graphitization, etc.).

The experimental results show that Φ_B depends on Φ_M less than is expected by the theory. The summary of results on N-type, obtained in 1995 by Porter and Davis [POR 95], shows a range of values between 0.8 and 1.25 eV on SiC-6H (0001) – Si face, and between 1.0 and 1.6 eV on SiC-6H (0001) – C face, for all metals: Au, Al, Ag, Ti, Pd, Mn, Mg, Hf, Co, Ni. It was shown that the presence of surface conditions inside the forbidden energy band (intrinsic to the surface or induced by metallization) influences control of the Schottky barrier height, moderating the

influence of output work. The semiconductor surface preparation stages before metal deposit, the parameters of this deposit and the quality of the SiC material are all crucial for the result and reproducibility of rectifier contact.

Ni is the most commonly used metal for the production of prototypes based on N-type rectifier contacts in 4H SiC because it has a high output work, leading to a barrier height of 1.24-1.29 eV on a 6H-SiC silicon face (after sacrificial oxidation of the surface and pre-annealing under ultra-vacuum [WAL 93]). Barrier height is equal to 1.6 eV on 4H-SiC (after chemical cleaning and cleaning *in-situ* before filing under ultra-vacuum), this increases by 0.23 eV after annealing at 700°C for 10 min; these works also relate to an ideal ratio of 1.1 [KES 00]. Titanium is the second most commonly used metal for obtaining Schottky contact on a N-type, leading to a rectifier contact coefficient ideally close to 1. The height of the barrier is 0.95 eV on 4H-SiC face Si (for a deposit after wet chemical cleanings) [ITO 97]. A change in barrier height, from 0.88 eV to 1.08 eV, was reported on 6H SiC-N-type after annealing at 700°C for 1 hour (linked to the changing nature of the interface metal [POR 95]).

The leakage currents in reverse polarization are higher than projected in the theory of simple thermo ionic emission. In addition to the possible participation of localized defects, or suburb effect, the contribution of a thermo ionic emission assisted by the field has been researched [HAT 02].

Works on SiC Schottky contacts of P-type are infrequent, given the rare need for this type of contact by applications. Barrier heights higher than those of the N-type are reported for SiC-6H (1.45 eV to 2.56 eV for Au, Ni, Pd, Al, Co, Ag, Ti, Cs, Mg face Si [ITO 97]), with ideal rectifier contact factors of greater than 1, showing that thermo ionic emission is not the predominant mechanism for conducting the current.

Current research is focused on optimizing manufacturing processes (by monitoring influence of surface pre-treatments [MOR 00], and type of metal [HAT 01], etc.), mainly in terms of temperature stability, quality and consistency on the large surface of the interface metal/SiC of P-type.

4.3.2.4.3. Ohmic contact and current features

Achieving a metal/SiC contact with good ohmic properties requires the reduction of heights of Schottky barrier (usually obtained by annealing at relatively high temperature), and high levels of doping (in order to improve current conduction via the tunnel effect through the barrier, as shown in Figure 4.7c, with the example of a N degenerated semiconductor).

On the areas of N-type SiC, nickel is often chosen as a demonstrator. It is deposited at room temperature and annealed at approximately 1,000°C for a few

minutes, enabling the creation of a layer of silicide Ni_2Si at the interface (this reaction consuming Ni and SiC in a ratio of 1:1), and others (such as the migration of C far away from the interface), are all necessary for lowering the height of the Schottky barrier (equal to 0.35 eV on 6H SiC). The lowest specific resistance of contact for Ni/SiC-6H or -4H is about 10^{-6} Ω.cm^2 at room temperature for doping greater than 10^{19} cm^{-3} [CRO 97]. The physical and electrical stability of this contact is appropriate for long-term uses at temperatures below 500°C (Crofton *et al.* did not observe evolution of specific contact resistance after 300 hours at 650°C; instead resistance increases with temperature [CRO 95]).

On SiC P-type regions, aluminum produces both a reasonable specific resistance (about 10^{-3} Ω.cm^2 on 6H material moderately doped at $8x10^{18}$ cm^{-3} [ADA 94]) and a low depth of reaction in the semiconductor. Annealing at relatively high temperature (800°C) during several minutes of aluminum (or one of its alloys) allows Al to disseminate superficially in SiC, which increases the doping on the surface, thus promoting ohmic properties of contact. The film of aluminum must be "encapsulated" (usually with Ti, and possibly Pd), to withstand such annealing temperatures and avoid the formation of an insulating layer on the contact surface. Proper dosage of the layer and very good control of the annealing conditions are essential to control the various reactions involved, and therefore the quality and reproducibility of this type of ohmic contact [NOR 96].

The recent feasibility of higher levels of doping (above 10^{19} cm^{-3}) has reduced the specific resistance of contact on P-type SiC, down to 10^{-4} Ω.cm^2 for contacts based on annealed Al, and annealed or non-annealed Mo, Ta, Ti, and Pt [CRO 97]. Values of a few 10^{-5} Ω.cm^2 were also reported with, for example, Ti annealed at 800°C for 1 min on SiC doped at 10^{19} cm^{-3}. In publications specifically dedicated to the experimental evaluation of SiC demonstrators, metallization on anodes or P-type grids remain the most often-based annealed Al-Ti (for research into employment of annealed titanium or platinum see [SIN 01]).

Current research attempts to better understand the nature of the interface and develop processes to solve disadvantages: such as, low Al grip on SiC, SiC consumption that can be crippling in implanted or epitaxied areas with little depth (TaC is proposed on 6H SiC N-type [JAN 00]); and quite high annealing temperatures and stability in high temperature, etc. Mastering high level doping (especially by ion implantation) is also a crucial factor influencing the progress of research into ohmic contact on P-type.

4.4. Applications of silicon carbide in power electronics

4.4.1. *SiC components for high frequency power supplies*

As previously explained (see section 4.2), the physical properties of silicon carbide contribute to the simplification of the compromise between on-state low voltage drop and switching speed, that the designer has to face when choosing a switch, or a diode, when the voltage is imposed by the target application. Due to its operating principle and its relative simplicity, the Schottky diode is the first component that should succeed in demonstrating this potential.

4.4.1.1. *SiC Schottky diodes in 4H N-type*

These were the first SiC power device to lead the market. An initial marketing announcement was made by Microsemi in 2000 [MIC 00] (in association with the supplier of substrates Sterling Semiconductor [STE 01]), this was followed by a second announcement made by Infineon Technologies AG in 2001 [INT 01].

4.4.1.1.1. Marketed diode specifications

The updated basic specifications of some of these devices are displayed in Table 4.8.

Changes in the temperature of direct and reverse electrical characteristics are shown in Figure 4.8, using reference SDP06S60 as an example extracted from the publication of Kapels *et al.* [KAP 01]. The specific on-state differential resistance R_{on}, is indicated for 25°C equaling 0.9 mΩ.cm^2. We conclude that the nominal current of 6 Amps corresponds to a high current density (about 400 A.cm^{-2}) for a direct voltage of 1.5 V, at 25°C. R_{on} increases with temperature, as do leakage reverse currents.

Features	UPSC600[MIC 00]	SDP06S60[INT 01]	SDT12S60[INT 01]
Rated current (I_F)	1 A (75°C)	6 A (100°C)	12 A (100°C)
Reverse voltage (V_{RRM})	600 V	600 V	600 V
Max overload current. (I_{FSM})	10 A	21.5 A	120 A
On-state voltage (V_{on})	1.3 V (1 A / 25°C) 1.6 V (1 A / 150°C)	1.5 V (6 A / 25°C) 1.7 V (6 A / 150°C)	1.5 V (12 A / 25°C) 1.7 V (12 A / 150°C)
Capacitive charge	-	21 nC (400 V / 6 A / 200 A/µs / 150°C)	30 nC (400 V / 12 A / 200 A/µs / 150°C)
Total capacity	15 pF (200 V / 1 MHz)	15 pF (600 V / 1 MHz)	43 pF (600 V / 1 MHz)
Reverse current (I_R)	20 µA (600 V / 25°C)	20 µA (600 V / 25°C) 55 µA (600 V / 150°C)	40 µA (600 V / 25°C) 100 µA (600 V / 150°C)
Max. junction temperature (T_{jmax})	150°C	175°C	175°C
Thermal resistance (R_{th})	30 K/W (Junct-Tab) 10 K/W (Junct-Bot)	62 K/W (Junct-amb)	62 K/W (Junct-amb)

Table 4.8. *Typical electrical characteristics of marketed Schottky diodes in 4H-SiC*

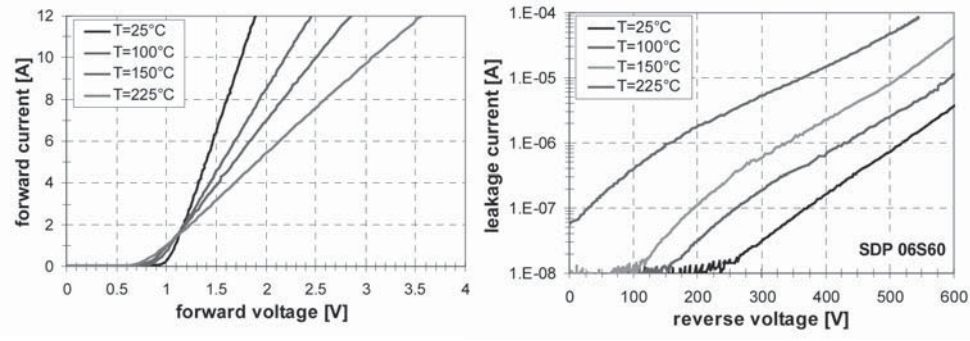


Figure 4.8. *Direct and reverse features of a SDP06S60 depending on temperature (figure extracted from [KAP 01])*

Opening switching of the Schottky diode is a mechanism of capacitive load (the capacity of the junction which switches off). The movement of the charge of desertion creates a reverse peak current at blocking, that is independent of

temperature, and at the rate of decay of the current in the diode (e.g. -3 Amps for a direct current of 4 Amps switched under -300 V).

4.4.1.1.2. Other results on high-voltage SiC Schottky diodes

Prototypes of 4H-SiC at much higher voltage than 600 V were made by different laboratories: with Infineon Technologies already planing to extend its range up to 3.3 kV.

Table 4.9 brings together a number of best results, showing breakdown voltages around 4 kV, specific on-state resistances (at 25°C) of between 2 and 6 $m\Omega.cm^2$ for structures up to 1,700 V, and between 14 and 34 $m\Omega.cm^2$ beyond. The leakage currents at 25°C, for a reverse polarization close to the breakdown voltage, are high.

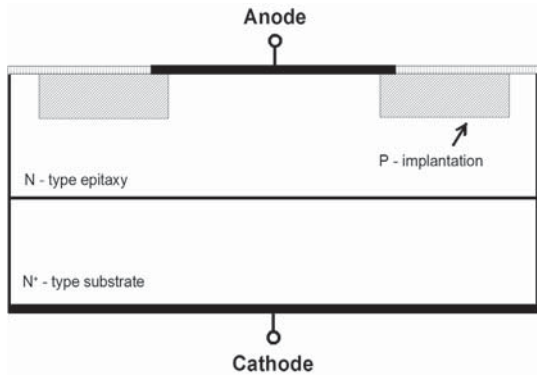


Figure 4.9. *Schematic of the structure of a Schottky diode on SiC type N, with a peripheral protection device implanted as a P-type pocket*

The peripheral protection (necessary to reduce electric field reinforcements on the peripheral of the junction) is provided by the field plate, or more frequently (on latest structures) by being implemented a P-type pocket (or junction termination extension, JTE), as shown in Figure 4.9.

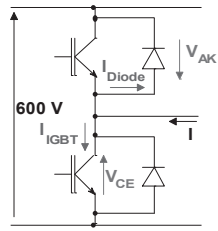
Structure passivation protection reference	**Doping / thickness of voltage strength layer** (cm^{-3}/µm)	**Anode section** (cm^2)	**Reverse voltage strength / Temp.** (V/°C)	**Direct voltage / current density / temp.** (V/A.cm^{-2}/°C)	**Specific differential series resistance / temp.** (mΩ.cm^2/°C)	**Current density / reverse voltage / temp.** (µA.cm^{-2}/V/°C)
Ti/N$^-$N$^+$ Polyimid/SiO_2 JTEepi + mesa [TEM 01]	$1x10^{16}$ /6	0.015	600/25	1.1/100/25 1.5/533/25	- / -	$6x10^3$/500/25
Ni/N$^-$N$^+$ Pl. of field [KIM 98]	$6x10^{15}$ /22	-	910/25	1.63/100/25	2,6/25	$4x10^5$/800/25
Ni/N$^-$N$^+$ Pl. of field [KIM 00]	$3\text{-}5x10^{15}$ /8-10	$7x10^{-4}$	800-1000/ 25	- / - / -	4-6/25	0.2/100/25
Ti/N$^-$N$^+$ photoimid JTE [PET 01]	$5x10^{15}$ /13	0.1	1200/25	1.7/250/25 2.3/250/125	3/25 6/125	40/1200/25 120/1200/125
Ti/N$^-$N$^+$ JTE [PET 01]	$2{,}5x10^{15}$ /15	0.1	1700/25	2.3/250/25 3.4/250/125	5/25 10 /125	1500/1700/25 4500/1700/125
Ni/N$^-$N$^+$ JTE [TSU 01]	$3x10^{15}$ /27	0.008	2400/25	2.7/100/25	13.8/25	0.1-1000/ 600/25
Ni/N$^-$N$^+$ Pl. of field [KIM 98]	$1x10^{15}$ /42	-	2800/25	- / - / -	34/25	0.7/1000/25-
Ni/N$^-$N$^+$ SiO_2 Pl. of field [WAH 00]	$7x10^{14}$ /43	$7x10^{-4}$	3850/25	4.4/100/25	30/25	1.7/2000/25

Table 4.9. *Major technological and electrical characteristics of various Schottky diodes demonstrators, at high-voltage, on SiC-type 4H N*

4.4.1.1.3. Comparison with silicon

The competing silicon structures in the 300 V range and beyond, are bipolar diodes. The superiority of the Schottky diode (even over an ultra-fast silicon diode) is due to the lack of stored charge when conducting. For this reason, there is no recovery at blocking. It is important to note that the equivalent junction capacitance of a Schottky diode is independent of the direct switched current density in the structure and is insensitive to

temperature rise (as opposed to the bipolar diode reverse capacitance, dependent on the stored charge, i.e. forward bias and operating temperature). However, it is greater than the charge of displacement of a silicon bipolar diode of the same voltage range by a factor equal to the ratio of the critical electric fields of both materials. A reduction of the section of the component is then necessary to limit the junction capacitance (to compromise with the performances for electrical and thermal conduction).



(a) With bipolar silicon diode (b) With SiC Schottky diode

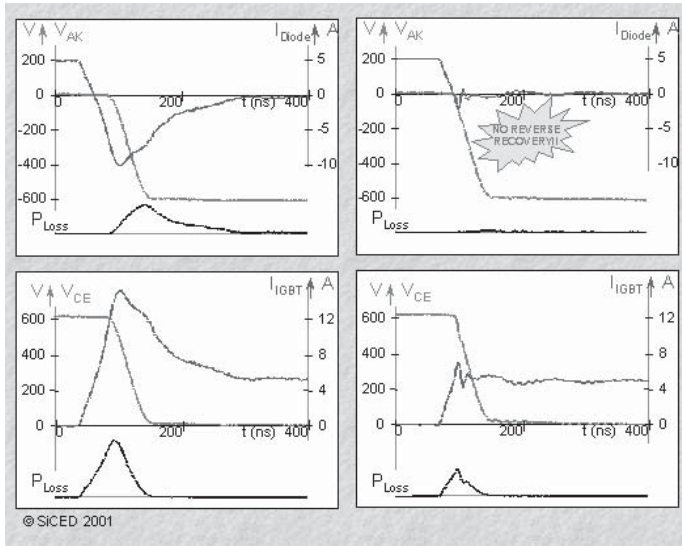


Figure 4.10. *Comparison of the current and voltage waveforms of the diode and the associated switch in assembling a chopper, powered under 600 V, providing a current load of 5 A. Diode voltage rating: 1,200 V [SICe 01]*

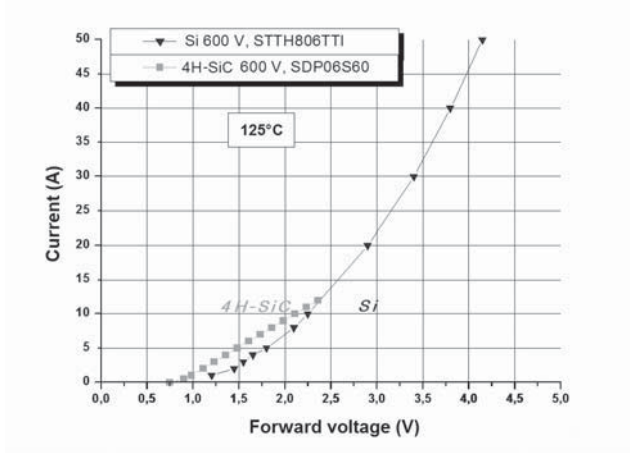
The impact of switching times, on the constraints of over-current and over-voltage, and especially on switching losses for the associated switch of the diode is clearly displayed in Figure 4.10 (extracted from [SICe 01]). This figure provides a comparison of the current and voltage waveforms of the diode and the IGBT partner switch in an inverter, powered under 600 V and providing a current load of 5 A.

The graphs on the left correspond to the result of the use of a bipolar silicon diode, while the graphs on the right display results for a 4H SiC Schottky diode. The voltage rating of the diodes is 1,200 V.

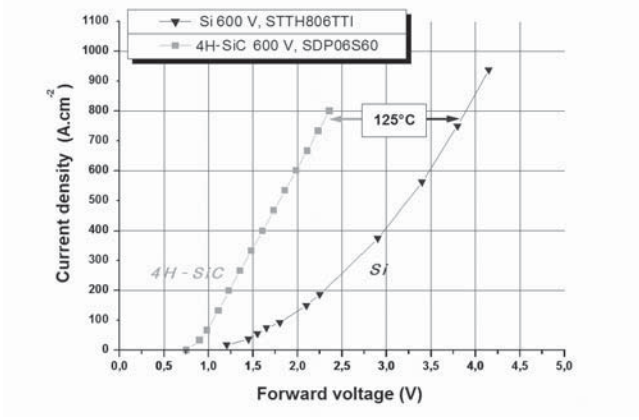
The impact on switching time and the associated losses can allow an increase in the maximum operating frequency of the power supplies, this is useful for reducing the dimensions of the inductive and capacitive elements involved.

The impact on efficiency and on the possibility of reducing cooling systems, depends on the balance between switching losses and conduction losses of the diode. Figure 4.11 compares the Schottky diode, 600 V/6 A in SiC (SDP06S60), with a silicon diode, 600 V/8 A ultra-fast (STTH806TTI); in terms of terminals voltage depending on the current, and in terms of current density. For the $J_d(V_d)$ characteristic of the silicon diode, the average current I_{Fav} of the data sheet of the manufacturer is assumed to have a current density of 150 $A.cm^{-2}$. The SiC diode is assumed to have a nominal current, I_F, density of 400 $A.cm^{-2}$. The direct characteristics $I_d(V_d)$ at 125°C reported here are rebuilt from the data sheets of these two products ([STM 01] [INT 01]). Figure 4.11 shows that at a 125°C junction temperature the voltage across the SiC diode is lower than that of its competitor for a same current. This is true until the current is less than the current I_C (point of intersection of compared characteristics), in this case equal to 12 A. Note that an increase in operating temperature of the SiC diode (T_{jmax} is equal to 175°C) to 150°C will favor the silicon diode silicon, while I_C is slightly reduced to 10 A. In contrast, a decrease in the junction temperature of the two diodes will contribute to increasing the SiC diode by the value I_C.

Therefore, improvement of conduction losses can also be obtained by the choice of a SiC Schottky diode as an ultra-fast diode, for applications where the direct current passing through the diode is less than I_C, in other words when the average current I_{Fav} and the duty cycle δ of the diodes conduction have the relation: $I_{Fav} < I_C.\delta$. This gain is highly dependent on conditions of use (T_j, δ, I_F), is less spectacular than the gain on switching losses, and will be reduced when the required holding voltage increases.



(a)



(b)

Figure 4.11. *Comparison of the typical direct characteristics of two 600 V ultra-fast diodes in competition: the Si bipolar diode STTH806TTI (from the manufacturer catalogue, assumes 8 A corresponds to 150 A.cm^{-2}) and the Schottky diode in 4H-SiC SDP06S60 (from the manufacturer catalogue, assumes 6 A corresponds to 400 A.cm^{-2}): (a) characteristics I_d-V_d; (b) characteristics J_d-V_d*

In the forward state, the high-voltage SiC Schottky diode differs from the bipolar silicon diode via its differential resistance and a positive temperature coefficient. The SiC Schottky diode is an advantage for release in parallel obtaining high current ratings (which is also an answer to the current problem caused by the small size of chips). This SiC Schottky diode is not, however, as effective as the bipolar diode when operating in a regime of over-load current: the surge of direct voltage in the

case of unipolar device leads to a self-heating of the material, which can lead to destruction (by environmental degradation of the SiC chip, including metallizations). This is a limitation on the I_{FSM} characteristic [RUP 00].

We should note, finally, that the gap between the diode in 4H-SiC 600 V and its silicon rival is much more important in terms of current density than in terms of current, for a given direct voltage drop (and a given temperature) (see Figure 4.11). The manufacturer's choice to use of the 4H-SiC diode refrains from exploiting this advantageous characteristic seriously limiting the size of the silicon carbide component, due to the already mentioned compromise between conduction performance (V_F, I_{FSM}, R_{thja}) and commutation performance (charge of desertion). The choice probably also reflects a cost constraint. The current surface price of a silicon carbide component is indeed high and increases with its size (because of substrate cost and the density of defects that they contain, both of which are very important).

4.4.1.2. *Example of application: the power factor correction*

The availability of commercial SiC Schottky diodes led to research into their implementation and their contribution at the system level. The function of power factor correction (PFC) is an example generally retained to assess the interest of a SiC Schottky diode and its field of application. This function is essential for all equipment connected to the alternative network and requiring a continuous supply, which, for example, includes computers. The "boost" circuit type in continuous conduction is the most interesting technical solution, its setback being losses caused by the opening of the diode, which is done under strong current (hard switching).

Various studies implementing the product of reference SDP06S60 in a PFC with output voltage of 380 V for a range of frequencies from 100 kHz to 500 kHz, agree on the following comments:

– At approximately 100 kHz, the PFC circuit with a 4H-SiC Schottky diode does not improve significantly in terms of total losses in semiconductors (diode + transistor) compared to the use of a (less expensive) Si ultra-fast diode, or even a slow Si diode combined with a circuit for commutation aid (snubber) [BEN 01].

– The SiC based solution is justified when using a higher frequency. Indeed, the efficiency almost does not change when the frequency increases from 100 kHz to 500 kHz for the circuit using SiC Schottky diode, although it falls very quickly when a silicon bipolar ultra-fast diode (examples: STTH806TTI or MURH860) is used. The MOSFET switch used in this study [KAP 01] is the silicon CoolMOS SPP20N60C3. The main advantage is obtained at the level of inductive components: it was shown that the operation of a 400 W PFC circuit at 500 kHz with a SiC

Schottky diode and a Si CoolMOS, compared with the same circuit at 140 kHz with a more conventional diode and switch, requires an inductance with a diameter divided by 2, and an overall cost reduced by 8% (the division by 3 of the cost of the PFC inductor erases the increased costs of the SiC diode). Note that the comparison is made with the same cooler and with comparable filters against electromagnetic interference (EMI).

Additionally, the gain in terms of switching losses in the cell can be utilized not only by increasing the frequency: but alternatively by reducing the section of the switch; by reducing the complexity of the system; by reducing the cooler; or by raising the temperature, etc. The designer is vigilant when creating the system, basing the design on the determination of losses (by simulations and/or measures). This becomes particularly difficult with the reduction of switching time (around ten nanoseconds), and the exacerbated influence of the parasitic elements of the circuit. Design tools (and measures) still require improvment in order to be able to report accurately on all the elements of this system, like current and voltage waveforms, and the various couplings (electrical, thermal and magnetic).

In the example considered above, the transistor associated with the SiC Schottky diode was in silicon, because at the moment, no silicon carbide switch is available on the market. We will present the new technology, using explanatory examples of demonstrators currently being developed by various research centres.

4.4.1.3. *High-frequency SiC power switches*

As with the Schottky diode (and following a “silicon logic”), theoretical analysis predicted the silicon carbide MOSFET with N inversion channel as the high frequency and high voltage switch (up to 3 kV at least) of the future, and research largely focused on such structures. Although prototypes have already helped to overcome the limits imposed by the silicon diode by reducing the on-state resistance for a given blocking voltage, SiC MOSFET is slow to keep its promises and to fully emerge as a commercial product. It remains a deeply researched option. Research tries to clarify and eliminate the causes of SiC MOSFETs current performance-cons (described in section 4.3.2.3). These difficulties have promoted the proposal of other unipolar structures to ensure the function of high voltage fast switching.

4.4.1.3.1. Silicon carbide MOSFET transistors with a N inversion channel

As was the case for silicon, the first published structures of power SiC are etched structures, not “V” structures (as with the first Si VMOSFETs), but “U” structures, to underline the form of trenches where the isolated grid command is located, in the UMOSFET switch, and where an inversion channel will be formed (see Figure 4.12). These trenches surround the P regions, through a layer which may have been created earlier by epitaxy on the N layer of voltage holding the component.

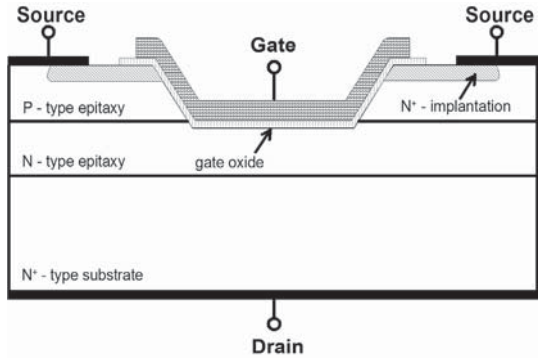


Figure 4.12. *Schematic of a silicon carbide UMOSFET cell*

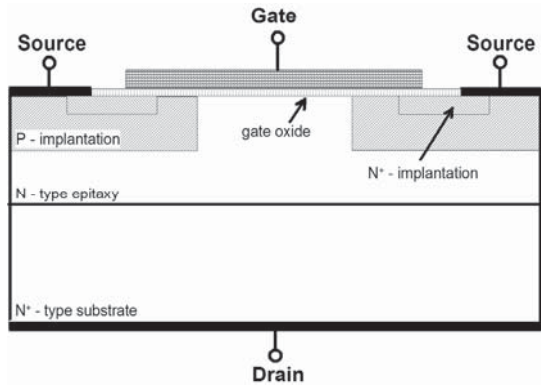


Figure 4.13. *Schematic of a silicon carbide DIMOSFET cell*

With the progress of P-type doping, plane structures (which are generalized in the silicon industry, as better suited for high voltage), have been carried out in SiC by double (or triple [SCH 00]) N epitaxy locations. Figure 4.13 shows a DIMOSFET structure, which requires a first implantation (or two) for the creation of P areas upon which the inverting canal will be induced, and a second implantation for the creation of strongly doped N^+ type sources. This last step also appears in the manufacturing process of the UMOSFET. The two architectures are also based on a heavily doped N^+ type substrate.

Table 4.10 shows results for the SiC MOSFET whose on-state specific resistance is less than the theoretical limit set for the silicon (25°C). The best performance is obtained on 6H-SiC, while the worst was obtained on 4H-SiC

(despite the fact that the latter has a lower theoretical resistivity of drain layers (see section 4.2.4.2). This indeed reflects a limitation of conduction by the inversion canal area (where the problem of an apparent low mobility of electrons has been transferred, see section 4.3.2.3).

Structure Polytype reference	**Doping / thickness of voltage strength layer** (cm^{-3}/µm)	**Section** (cm^2)	**Voltage strength** (V)	**Direct voltage strength / current density** ($V/A.cm^{-2}$)	**Specific differential series resistance** ($m\Omega.cm^2$)	**Effective mobility of channel** ($cm^2.V^{-1}.s^{-1}$)
UMOSFET 4H [PAL 96]	- / -	-	260	2.65/200	18	-
DIMOSFET 6H [SHE 97]	$1,7x10^{16}$ /10	-	510	6.5/100 at V_{GS}=30 V	66 at V_{GS}=30 V	17
UMOSFET 4H [AGA 98]	$2x10^{15}$ /12	0,0015	1400	8/100 *at 100°C* and V_{GS}=26 V	74 at V_{GS}=26 V	7 *at 100°C*
UMOSFET 4H [SUG 98]	10^{15} /25	-	1400	- / -	311	-
DIMOSFET 6H [SCH 00]	$9x10^{15}$ /12	0,0047	1800	5/100 at V_{GS}=10 V	46 at V_{GS}=10 V	15

Table 4.10. *Major technological and electrical characteristics of the best MOSFET transistor demonstrators in SiC-6H high-voltage, and 4H Channel N, at 25°C (temperature indicated if other)*

The most interesting prototype is the plane structure 6H-SiC with a direct keeping voltage 1,800 V (section equal to 0.47 mm^2), a threshold voltage of 4.8 V at room temperature, and an on-state specific resistance of 46 $m\Omega.cm^2$ (of which 36% would be induced by the channel) for a command voltage, V_{GS}, of 10 V [SCH 00].

4.4.1.3.2. Accumulation MOSFET transistors and JFET transistors

Such structures no longer rely on the control of current passage in the N inversion channel (created in a P area), instead they rely on the N accumulation channel or N pre-formed "channel" (in the N layer). The field-effect allowing control of the resistivity of this channel is induced by a MOS grid or bipolar junction. As presented in Figures 4.14 and 4.15, a layer of type P^+ delineates the

channel area. It ensures the full control of conduction in the case of JFET. It also participates in the case of Accu-MOSFET, where it helps to protect the grid insulation against the strong electric fields present in the silicon carbide. According to the depth and the doping of the superior N layer (of the channel), the device is normally opened (the usual case for users of silicon power transistors) or closed.

Table 4.11 shows the result of the main experiments recently published, showing that the specific conduction resistance, R_{on}, is lower than those obtained for silicon components of comparable voltage strength. The best current characteristics in terms of low on-state resistance and high voltage strength, correspond to a 1,800 V JFET with a R_{on} of 14 mΩ.cm^2 at 25°C [FRI 00]. This unipolar component, normally conducting, has a dependence on temperature for R_{on} proportional to $T^{2.58}$, which leads to a decrease in the passing current, under constant polarization due to self-heating.

This feature allows the setting of chips in parallel (as is the case with any MOSFET, and as previously mentioned for the SiC Schottky diode). This property is important considering once combined with the robustness of silicon carbide at high temperature, it can be used to satisfy a function of current limit.

Due to the availability of normally conductive unipolar transistors a revision of conventional electric schematics is required: this may be restricted to the component (for it to operate as a normally open-switch, such as SEJFET, for "Static Expansion JFET" [ASA 01]), or on a more global circuit level. Infineon Technologies offers such an association of "Cascode" type of a 1,800 V JFET controlled by a 60 V silicon MOSFET [SICe 01].

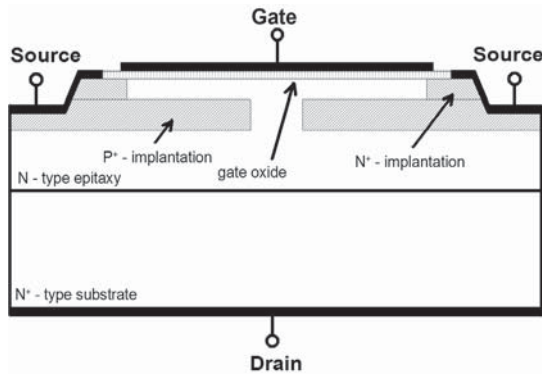


Figure 4.14. *Schematic of a cell of silicon carbide Accu-MOSFET*

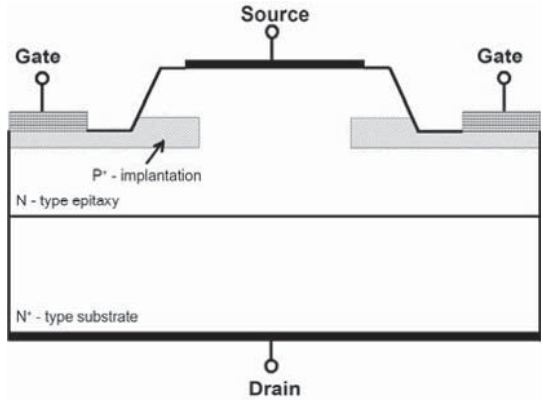


Figure 4.15. *Schematic of a cell of silicon carbide JFET*

Structure polytype protection reference	**Doping / thickness of voltage strength layer** ($cm^{-3}/\mu m$)	**Section** (cm^2)	**Direct voltage strength** (V)	**Direct voltage strength / current density** ($V/A.cm^{-2}$)	**Specific differential series resistance** ($m\Omega.cm^2$)	**Effective mobility of channel** ($cm^2.V^{-1}.s^{-1}$)
ACCUFET without 6H [SHE 98]	1×10^{16}/ 10	-	350	- / -	18 at V_{GS}=5 V	120
EC-FET 4H [HAR 98]	1.7×10^{15}/ 10	1.2×10^{-2}	450	10/0.1 at V_{GS}=10 V	11 at V_{GS}=10 V	108
UMOSFET 4H [TAN 98]	2.5×10^{15}/ 10	1.728×10^{-4}	1400	10/86.8 at V_{GS}=10 V	15.7	9-30
JFET 4H [FRI 00]	4.5×10^{15}/ 15	0.041	1800 at V_{GS}=-20 V	1/100 at V_{GS}=0 V	14 at V_{GS}=0 V	-
SEJFET 4H Mesa+JTE [ASA 01]	7×10^{14}/ 50	0.0037	4450 at V_{GS}=0 V	0,75/5,5 at V_{GS}=2.6 V	121 at V_{GS}=2.6 V	-

Table 4.11. *Major technological and electrical characteristics of various unipolar transistor demonstrators in high-voltage SiC 6H, and 4H N-type, at 25°C*

4.4.1.3.3. Comparison with silicon

The classic DMOSFETs family on silicon is marketed for a range of required voltage up to 1,200 V. For these structures, on-state resistance is essentially that of the voltage holding layer. It increases with the voltage rating according to $V^{2.3 \text{ to } 2.6}$, but also increases sharply with the temperature of silicon (by reducing the mobility of electrons). For example, the specific resistance of this layer alone is about 100 mΩ.cm^2 for a 600 V component and 700 mΩ.cm^2 for a 1,200 V component, at 25°C. Such values are an improvement on the values previously presented for the best MOSFET structures (46 mΩ.cm^2) and JFET (14 mΩ.cm^2) made with 4H-SiC and support higher voltages (1,800 V).

However, the performance of SiC structures is currently equivalent to those of the new MOSFET silicon technology, based on the principle of compensation, marketed from 1998 under the name CoolMOS^{TM} [LOR 98]: and R_{on} of 3 mΩ.cm^2 at room temperature for a 600 V component, a rating which corresponds to the limit in voltage currently available for this family.

So far, unipolar switches made in SiC already demonstrate the possibility of increasing the voltage range of switches beyond 600 V without penalizing the system by increasing conduction losses, knowing that the theoretical limit of silicon carbide has not yet been reached (located, for example, at 4 mΩ.cm^2 for a 3 kV component in 4H-SiC, with the R_{onS} characteristic), and knowing the technological difficulties to be overcome.

4.4.1.4. *SIT and MESFET power transistors in SiC for applications at very high frequency and microwaves*

Although applications in microwaves and power microwaves are a very specific area of power electronics, it is still interesting to devote a few lines to UHF and power microwave components as they constitute an important potential market for silicon carbide (as previously mentioned, see section 4.2.3.3). The first announcement of a commercial MESFET in SiC (in 1999 by CREE [CRE 01b]) is even earlier than the first Schottky diodes, the requirements of such structures on the characteristics of the material being less severe.

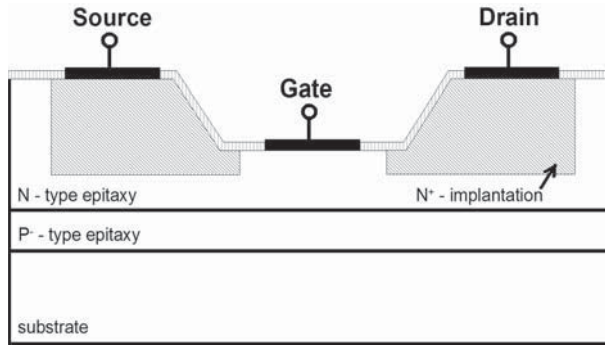


Figure 4.16. *Schematic of a silicon carbide MESFET cell*

The MESFET switch is a unipolar component with lateral conduction, where the sensitive area represents only a small surface (for example about 0.1 mm^2 for a "big" component of width 36 mm) and requires only a small epitaxy thickness with relatively high doping. The epitaxy is supported by a P-type layer that is filed on the departure substrate, preferably semi-insulator to increase the maximum frequency (the purity of the substrate must be very high). The basic layout is presented in Figure 4.16. The N-type epitaxy (with a doping of about 10^{17} cm^{-3}) is localy implemented, with N^+ type to create source and drain areas. An etching of the N layer sets the conduction channel between the two chambers. A metal grid lodged at the bottom of this etching, performing a Schottky contact with the N semiconductor, controls the conduction through the channel, by field-effect and by applying a negative voltage compared with the drain.

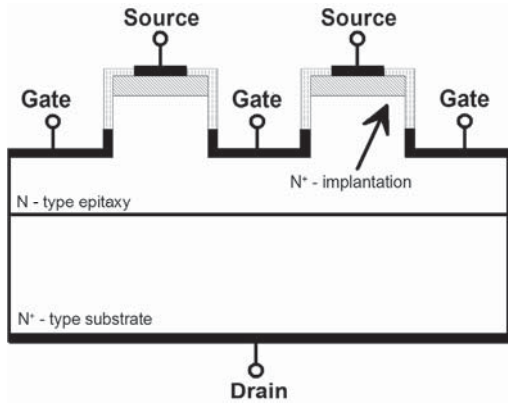


Figure 4.17. *Schematic of a silicon carbide SIT cell*

The SIT (Static Induction Transistor) switch seen in Figure 4.17 is better suited for applications under high voltage due to its vertical conduction structure [WEI 98]. The SIT switch consists of trenches, etched in an N-type epitaxial layer, coated on their sides and bottom with a metal in Schottky contact with the semiconductor. These trenches define the conduction channel of the component. The negative voltage applied between the grid and the source must allow for the pinching of this channel, which requires low doping and minimal width (respectively around 10^{16} cm^{-3} and 2 μm). Before etching, a new epitaxy or an implantation were conducted on the N epitaxy to create a strongly doped N^+ layer in order to get a good source ohmic contact on the surface.

Table 4.12 gives recent research results, including those for the commercial product of CREE [CRE 01b]. High voltage strengths are confirmed (up to 60 V, against 30 V for MESFET transistors in current silicon or GaAs) with powers of a few W/mm for total powers between 1 and 10 W at a few GHz. The latter, however, remains below the theoretical predictions.

In addition to the increase in output power supported by silicon carbide (up to a factor 4), higher levels of supply voltage (100 V are concerned) will considerably simplify the adaptation of impedance, both for passive elements to be added inside or outside of the boxes, as for very difficult settings (the removal of any system adaptation for applications of up to 3 GHz is even possible). As the MESFET SiC transistors are more linear, this simplification ensures the feasibility of broadband amplifiers that will allow the transmission of several telecommunication standards with the same equipment, thus resulting in substantial savings in terms of infrastructure (in volume, weight and cost).

Structure substrate reference	**Maximal frequency** **(GHz)**	**Small signal gain / drain current / drain voltage / frequency** **(dB/mA/V/GHz)**	**Total transconductance** (per grid width unit)**/ drain current / drain voltage** **(mS/mA/V)** ($mS.mm^{-1}/mA/V$)	**Total output RF power** (per grid width unit)**/ drain current/ drain voltage / frequency** **(W/mA/V/GHz)** ($W.mm^{-1}/mA.mm^{-1}/V/GHz$)
MESFET 1/2-insulating [CRE 01b]	4	12/500/48/2	160/500/48 *- / - / -*	12/500/48/2
MESFET 1/2-insulating [CAR 99]	20	12.5/-/60/3.5	*- /- / -* *40 (maximum)*	3.36/ - /60/3.5 *4/-/60/3.5*
MESFET 1/2-insulating [NOB 00]	-	8.4/140/80/2	*- /- / -* *- / - / -*	*- /- / - / -* *2,5/-/-/2*
MESFET conductor [MOO 97]	16	-	*- /- / -* *- / - / -*	1.1/37/50/0,85 *3.3/112/50/0.85*
SIT [SIE 97]	7-8	-	*- /- / -* *14 / - / -*	38/-/90/6 *1,2/ - /90/6*
SIT-module [SIE 99]	-	-	*- /- / -* *- / - / -*	190/500/90/2.9 (*) *- / - / - / -*

Table 4.12. *Major technological and electrical characteristics of various MESFET and SIT transistor prototypes in 4H-SiC N-type, at 25°C, in continuous wave mode (or pulsed (*))*

In summary, applications within the frequency range of 30 MHz to 10 GHz are mainly targeted: such as power amplifier systems for wireless applications (base station emitters for new generations of telecommunications systems), the digital television and radio systems, radar equipments, microwave ovens, missile detection, meteorology, etc. While the theoretical output powers of these new SiC components are not quite confirmed, research carried out over the next two years should help to discern whether silicon carbide or materials based on gallium nitride (which are better suited for frequencies beyond 10 GHz, but whose technology is less advanced) will penetrate the pre-cited markets.

4.4.2. *SiC components for switching systems under high voltage and high power*

The physical properties of silicon carbide mentioned earlier in this chapter should help to achieve very high voltage strengths from epitaxial films with very reasonable thickness and doping level. We have already mentioned demonstrators of unipolar components with high breakdown voltages close to 4 kV (see section 4.4.1). Bipolar components are theoretically better suited for very high voltage and high power applications. The demonstration of the possibility of reaching very high breakdown voltages, even higher than the limits of silicon devices, was shown by many demonstrators.

The state of the art of performances of SiC diodes and high-voltage thyristors are presented in the following sub-section. Mixed unipolar/bipolar structures of demonstrators (for example, bipolar junction diodes, Schottky diodes, and IGBT) also made in SiC, will be presented, in an attempt to extend the power of the unipolar "family" or frequency range of other the bipolar "family". Positioning of the respective areas of preferential use of the different technologies, including silicon, is proposed. This is provisional, given the immaturity of the SiC devices presented here (still at the research stage) and the progress of each chain. Currently known potential applications will also be mentioned.

4.4.2.1. *Bipolar diodes and bipolar and Schottky mixed junction diodes*

The SiC bipolar diode is made on a heavily doped N^+-type substrate, more generally of 4H polytype for the last tests. The low doped N-type voltage holding layer, is epitaxied on this substrate (often after filing of an intermediate N^+ layer with a thickness of about 1 μm). The emitter is strongly P^+-type doped and then applied either by implantation or by resumption of epitaxy. In the latter case, the termination of the junction requires an engraving (to provide protection by simple mesa, or with JTE), while plane structures can be used to protect the periphery of P^+ emitters against enhancements of the electric field under strong reverse polarization. Most often there is a lateral extension of the junction termination (JTE, itself implanted), as shown in Figure 4.18.

The goal of achieving diodes with Schottky mixed bipolar junctions (so-called "JBS"' or "MPS") simultaneously benefits the lower voltage drop at the on-state of the metal/semiconductor junction, and the lower leakage currents at reverse state of the P^+N junction, for a given voltage rating. The ion implantation of the P^+ emitter regions produces plane JBS structures on N-type epitaxied substrate, as shown in Figure 4.19. Non-plane JBS structures can also be made from a pile of epitaxies P^+ on N (on N^+ substrate), etching the P^+ layer onto the desired locations for Schottky contacts, and onto the periphery.

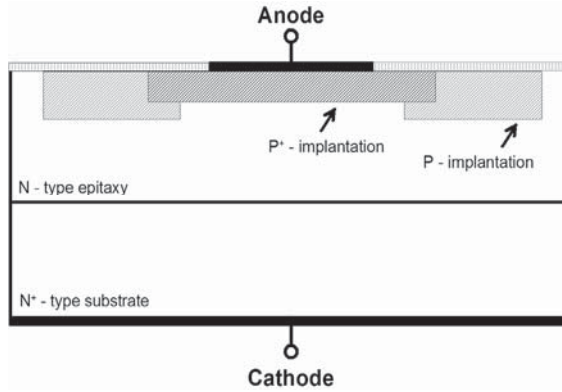


Figure 4.18. *Schematic of a SiC bipolar diode P^+NN^+ with JTE type peripheral protection*

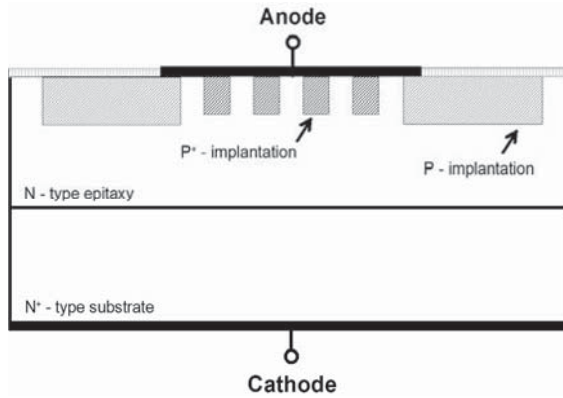


Figure 4.19. *Schematic of a SiC diode with mixed bipolar and Schottky junction with JTE type peripheral protection*

4.4.2.1.1. Performances of bipolar and "JBS" diodes

Tables 4.13 and 4.14 present direct and reverse, technological and electrical characteristics of prototypes of bipolar and JBS diodes, published in recent years.

Structure passivation protection reference	**Doping / thickness of voltage strength layer** (cm^{-3}/µm)	**Anode section** (cm^2)	**Reverse voltage strength / temp.** (V/°C)	**Direct voltage / current density** (V/A.cm^{-2}/°C)	**Specific differential series resistance / current density / temp.** (mΩ.cm^2/ A.cm^{-2}/°C)	**Current density / reverse voltage / temp.** (mA. cm^{-2}/V/°C)
P^+(imp)NN^+ JTE [MIT 98]	$8x10^{15}$ /14 $5x10^{15}$ /26	0.01 0.01	2000 3000	3/100/25 4/500/25 3.15/100/25 3/100/125 4.8/500/25	2.2/500/25 3/500/25	$3x10^{-6}$/ 1000/20 $3x10^{-5}$/ 1000/150 $3x10^{-6}$/ 1000/20 $3x10^{-5}$/ 1000/150
P^+(imp)NN^+ JTE [CEG 01]	$1.2x10^{15}$ /40	0.01	2300	5/60/25	30/60/25	$<10^{-4}$/1100/25
P^+(imp)NN^+ SiO_2 JTE multiple [LEN 00]	10^{15} /35	0.2	3000	3.4/100/25	5/150/25 3.8/150/125	$<10^{-2}$/3000/25
P^+(imp)NN^+ SiO_2 JTE multiple [LEN 01]	10^{15} /35-45/	0.2	4500	3.4/100/25 3.3/100/125 4.3/300/25	7/200/25	$<10^{-3}$/4500/25
P^+(epi)NN^+ 2 µm SiO_2 JTE bore + stop. Channel [SIN 01]	$9x10^{14}$ /50	0.04	5300/25	3.7/100/25 3.3/100/225 6.9/1250/25	3.5/200/25 4/200/250 3/600/250	1/5000/25 $3x10^{-4}$/ 2000/50 $3x10^{-2}$/ 2000/225
P^+(epi)NN^+ JTE [SUG 00]	10^{15} /50	$3.14x10^{-4}$	6200/25	4.7/100/25	7.4/150/25	$15x10^{-3}$/6200 /25
P^+(epi)NN^+ JTE bore [SUG 01]	$2x10^{14}$ /120 $8x10^{13}$ /200	$3.14x10^{-4}$ to $7.85x10^{-1}$	14900/25 19500/25	4.4/100/25 4.1/100/250 5.1/300/250 6.5/100/25 7.5/100/250	6/150/25 5.3/150/250	1/14000/25 10/14000/250 3/19000/25 25/14000/250

Table 4.13. *Major technological and electrical characteristics of various demonstrators of bipolar high-voltage SiC-4H diodes from recent literature*

Structure polytype passivation protection reference	**Doping / thickness of voltage strength layer** (cm^{-3}/µm)	**Anode section** (cm^2)	**Reverse voltage strength / temp.** (V/°C)	**Direct voltage / current density / temp.** (V/A.cm^{-2}/C)	**Specific differential series resistance / temp.** (mΩ.cm^2/°C)	**Current density / reverse voltage / temp.** (mA.cm^{-2}/V/°C)
$(Ni/P^+)_{50\%}NN^+$ SiO_2 JTE etched [TON 00]	$9.7x10^{15}$ /13	0.031	1000	1.3/100/25 2.3/100/255 3/460/25	6.4/25 15/255	0.03/800/25 0.3/800/255
$(Ni/P^+)_{44\%}NN^+$ SiO_2+1 µm Si-poly Floatting rings [SHE 01]	$1\text{-}2.5x10^{15}$ /30	$3.14x10^{-4}$ to $1.26x10^{-3}$	2500	2.9/100/25		0.4/2000/25
$(Ti/P^+)NN^+$ SiO_2 JTE multiple [LEN 01]	10^{15} /35	$1x10^{-3}$	2500	2/100/25 2.6/100/125 3.6/300/25 4.7/300/125	8/25 14/125	0.02/1000/25
$(Ti/P^+)_{75\%}NN^+$ SiO_2 JTE [DAH 01]	$3x10^{15}$ /27	$4x10^{-4}$	2800	1.75/100/30 3/100/225 4.2/500/30	6/30 20/225	$3x10^{-3}$/500/30
$(Ni/P^+)_{50\%}NN^+$ JTE [ASA 00]	$1.3\text{-}1.8x10^{15}$ /30 $1.3\text{-}1.8x10^{15}$ /50	$9x10^{-4}$	2000 3600	3/100/25 6/100/25	 43/25	10/2000/25 10/3600/25

Table 4.14. *Major technological and electrical characteristics of various demonstrators of JBS high-voltage SiC N-type 4H diodes from recent literature*

The increase in deposit speeds of films has allowed for an increase in the achievements of high voltage demonstrators in recent years. In 2001 a 19 kV voltage (approximately double the maximum value offered by silicon) was recorded, voltage for a bipolar diode in 4H-SiC with an epitaxied base, N-type, thickness 200 µm [SUG 01]. The mixed junction structures were tested for up to 4 kV voltages.

The majority of prototypes are still small. The reduction of the density of defects in the substrates, however, recently allowed the characterization of a few prototypes of relatively large section bipolar diodes (40 mm^2 positioned in pre-selected regions), with tests run under direct currents of several tens of Amps [LEN 01]. The

efficiency of manufacturing such structures remains low starting on available substrates.

The leakage currents of bipolar diodes under heavy reverse polarization are generally very low, even when measured close to the maximum voltage, and even at relatively high temperatures, also in most cases these structures are without an optimal passivation surface. The leakage currents of JBS structures seem to be generally more important, from 25°C.

These demonstrators in bipolar SiC diodes, support several thousand of volts under reverse voltage, and have differential specific resistances at on-state from as low as a few $m\Omega.cm^2$ (for direct current densities greater than 100 A/cm^2) at room temperature, but also at high temperatures (250°C), while their characterizations in commutation also reveal that they are very fast components. Indeed, the reverse-recovery charge, and hence the associated peak reverse current, which were seen at blocking, are very low for all structures studied, as in the example of Figure 4.20 for a 5 kV diode [SIN 01]. Moreover, their speed is not affected by the rise in temperature. Such performances thus make it possible to operate very high voltage systems with switching frequency beyond the range of kHz.

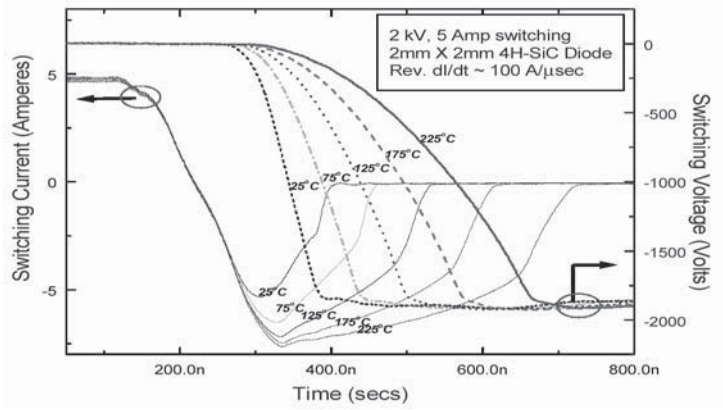


Figure 4.20. *Waveforms of current and voltage at the opening of a P^+NN^+ 5 kV diode at different temperatures. The switched current cut is 5 Amps (125 $A.cm^{-2}$), descending at a speed of 100 A/µs, under a 2 kV voltage (extracted from [SIN 01])*

Table 4.14 shows that JBS diodes keeping voltage to about 3 kV, also set a specific resistance of some $m\Omega.cm^2$ at room temperature. In terms of direct voltage these fast components confirm their interest in relation to the purely bipolar SiC structures, however, stronger voltage ratings, higher operating temperatures, and increasing values of series resistance (see also leakage current) make JBS diodes

much less attractive than bipolar junction devices for high power applications. Note also the low dependency (or stability) on temperature (in the operational range) displayed by the behavior of bipolar diodes, compared with unipolar conduction diodes.

The bipolar diodes potential for very high density current can be illustrated by the results of Dyakonova *et al.* [DYA 00] who reports on the feature of a direct current of up to 55 kA.cm^{-2}, depending on a voltage below 20 V, for a diode in 4H-SiC keeping a 5.5 kV voltage (diameter 100 μm, and N base of thickness 85 μm doped between 7 and 10 x 10^{14} cm^{-3}).

Some recent publications [LEN 01], however, reported an increase in direct voltage of certain bipolar devices subject to a polarization of long duration, which would put into question the reliability of the systems using them. This instability of the direct characteristic of the bipolar high-voltage SiC diode has not been observed for Schottky or JBS devices, and is attributed to defects in the base material (stacking faults), activated during operation (under current densities of about 100 A.cm^{-2}).

4.4.2.1.2. Comparison with silicon

We have seen that the high-voltage SiC based diodes, even when they are only bipolar type, are very fast devices. First, we will compare them to silicon bipolar diodes described as "fast", with voltage ratings between 3 and 6 kV (which is the highest rating currently offered in this category). Then we will discuss briefly, with an example, the case of recovery diodes with voltage strengths of up to 9 kV.

"Fast" silicon diodes with voltage strength between 3 kV and 6 kV

Although the active area of the semiconductor is unknown, it is possible to approximate a few orders of magnitude of performances of such products from manufacturers data sheets

– maximum junction temperatures in operation (T_{jmax}) are generally 125°C or 140°C;

– maximum leakage currents are between 10 and 100 mA/cm^2 at T_{jmax};

– specific series resistances estimated from values of differential resistance given at T_{jmax} vary broadly, within the range of 5 to 50 mΩ.cm^2;

– the maximum voltage drop in the forward state varies within a wide interval, ranging from about 3 V to 6 V at T_{jmax}, and for a current density (probably different from one component to another) around 300 A/cm^2 as a maximum.

Compared with the results presented in the preceding paragraph, we can see that the prototypes of a bipolar SiC diodes, with similar voltage strength (3 kV to 6 kV), show their superiority, including progress in terms of series resistance. The currently mastered technology has probably not as yet achieved the best results in terms of ohmic contact, efficiency of peripheral protections and surface passivation. This must also be made subject to encapsulation techniques adapted to conserve these performances.

In terms of voltage drop at on-state, the data shows that the range of values are equivalent for both SiC and "fast" Si bipolar technologies and that the extra voltage difference introduced by the SiC is not a handicap for this range of voltage strength and temperature.

For example, Figure 4.21 shows a direct comparison of the characteristics of a prototype of bipolar diode in 4H-SiC keeping a voltage of 4.5 kV [LEN 01], with those from the data sheets of a commercial product 4.5 kV (reference D911SH45T [EUP 01]), sold as a free wheeling diode for hard commutation converters based on IGBT or IGCT. To meet this function, the diode was necessarily designed to minimize its reverse-recovery charge, during its blocking. Comparison with the diode in 4H-SiC chosen itself for being fast, is very interesting.

Even if the values of current densities of the Si structure should not be regarded as accurate values (but rather over-estimated in order to evaluate the silicon carbide in a "worst case senario"), Figure 4.21 clearly shows that use of SiC is not necessarily a disadvantage from the viewpoint of the direct voltage on a fast diode: for this example at 4.5 kV and 125°C "only" (for silicon carbide, etc.) the 4H-SiC structure reduces conduction losses for current densities near or above 90 A/cm^2. This benefit will begin at a level of current density (and, therefore, power density to dissipate) even weaker than the increase in voltage rating (even as the operating temperature increases).

Thus, the power dissipated in conduction by high voltage SiC bipolar diodes will not reduce the silicon carbide drive to increase the frequency of commutations, and/or reduce cooling systems, which is allowed by the speed of these structures and their very limited switching losses. On this point, an example of comparison is also provided by Lendenmann *et al.* [LEN 00] They show that the commutation loss, measured for a module involving (in a pressed box conventional technology) the SiC diode from Figure 4.21 (actually 4 chips of 40 mm^2) and a 2.5 kV silicon IGBT (4 chips of 1 cm^2), switching 400 A under 1,250 V at a 125°C junction temperature, represents only a few per cent of a modules loss, including Si diodes of the same voltage rating. This way the switching frequency, limited to kHz by current Si devices due to the losses they suffer, partly due to the recovery of the free wheeling diode, may be increased.

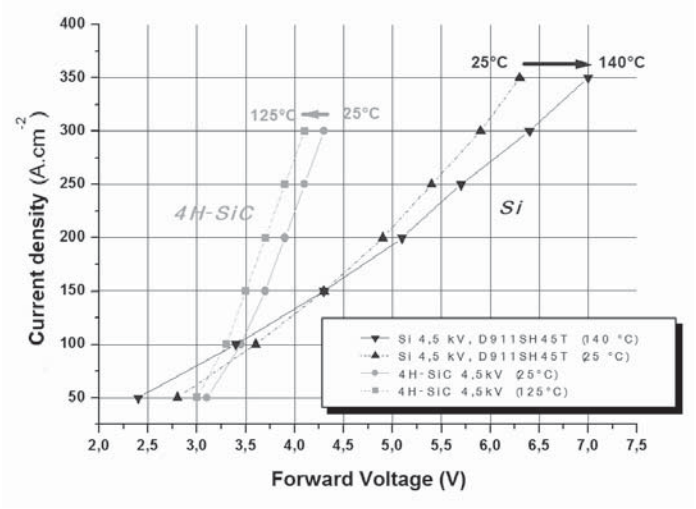


Figure 4.21. *Comparison of direct characteristics of "fast" bipolar silicon diodes D911SH45T in 4H-SiC studied by Lendenmann [LEN 01], with a voltage strength of 4.5 kV, for both provided junction temperatures. Note that, due to their size difference, the current values provided by the technical data sheet of the silicon component are converted into values of current densities. To do so, the average value of direct current $I_{F_{AV}}$ (911 Amps at 50 Hz and 85°C) was supposed to correspond to 100 A.cm^{-2}*

The on-state direct voltages of 4H-SiC JBS diodes, recorded in the preceding section as being smaller than those of bipolar diodes (in SiC as in "fast" Si) may have an interest in the lowest range of voltage considered here, for which their other performances remain very competitive. They would thus extend the scope of applications of SiC Schottky diodes. (This note would be even more important if the reliability problem of bipolar SiC diodes, mentioned above, remains unresolved). For these intermediate levels of voltage (between 2.5 kV and 3.5 kV approximately), four families of diodes should be placed in competition to meet the specification of a specific application, namely: SiC Schottky, SiC JBS, Si bipolar, or SiC bipolar (frequency-related matters, overload current, and volume are always the first criteria to be considered).

Recovery diodes for voltages up to 10 kV

When the function to be ensured is a recovery function, or a function for which the commutation speed is no longer a critical characteristic, the example seen here and shown in Figure 4.22 shows that silicon remains the best choice for applications up to 10 kV (the commercial current limit of Si).

Figure 4.22 shows the direct feature $J_d(V_d)$ of diode prototype 4.5 kV in 4H-SiC at 125°C used for the previous figure, and compares it with the same feature at 160°C for D471N80...90T diode, which has a voltage strength of 9 kV [EUP 01]. The characteristics of the SiC diode (at least up to 125°C) remain mostly to the right of the graph for the current densities considered, despite its voltage rating being lower than that of the Si diode.

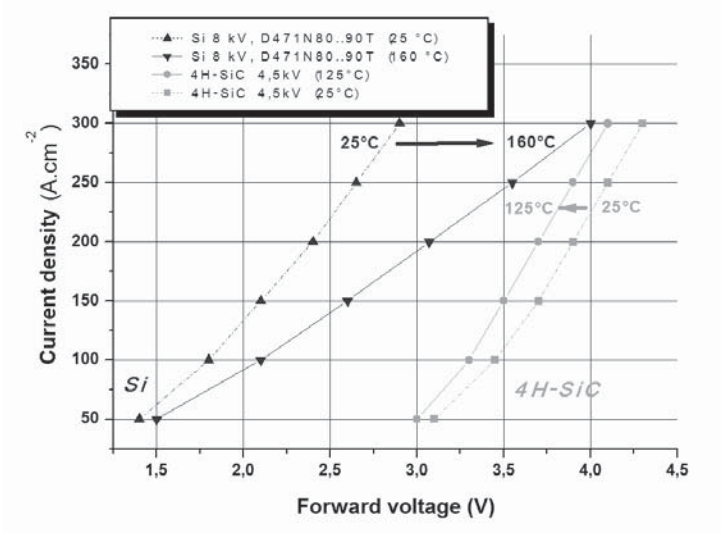


Figure 4.22. *Comparison of characteristics of the recovery silicon bipolar diode D471N80...90T keeping 9 kV, and the bipolar diode in 4H-SiC studied by Lendenmann [LEN 01] keeping 4.5 kV, for junction temperatures of 160°C and 125°C respectively. Note that, given the difference in size of these devices, the values of currents provided by the technical specification of the silicon component are converted into values of current densities, conceding that the average value of direct current I_{Fav} (565 A at 50 Hz and 85°C) corresponds to 100 A.cm^{-2}*

In this case, exploitation of the SiC junction's ability to operate at junction temperatures beyond 220°C[1], and thus dissipation of powers far beyond those possible for the silicon (theoretically limited to 400 W.cm^{-2}), may make silicon carbide rectifiers more advantageous at the limits of the voltage still covered by silicon.

1. Note: the value of this temperature is difficult to evaluate as it depends on the voltage rating. On the other hand, it will evolve according to the progress of SiC technology (control of doping profiles, carrier's lifetime, improvement of ohmic contacts and peripheral protection), which will lead to lower on-state voltage drops.

This assumes, of course, resolution of the issues raised by the feasibility of setting housing adapted to the operation under very high voltage and high internal temperature. The gain will result in the form of maximum current densities, and thus smaller or more powerful systems.

4.4.2.2. *Thyristors and IGBT*

The research onto this category of components is far less numerous than research into diodes (which are easier to build), and unipolar switches (whose theoretical benefits are more obvious and widespread). Thyristors and IGBTs (isolated gate bipolar transistors) in silicon concern more specifically the scope of applications of very high power (up to 80 MVA for thyristors and GTOs (thyristors opened by the gate) and 10 MVA for IGBTs). This specificity should be even more marked with SiC.

These components require, on the other hand, the implementation of at least four semiconductor layers (instead of the norm of three minimum), and include (exclusively or in part) a bipolar conduction, which requires a superior quality for the semiconductor and its doping. Finally, the IGBT structure inherits most of the problems of the SiC MOSFET structure (linked to the current quality of the SiO_2/SiC interface and to the strong electric field in the oxide). The first thyristor (symmetric GTO [PAL 96]) and IGBT (N-channel [RAM 96]) demonstrators date back to 1996.

The majority of structures obtained so far are in 4H-SiC and made by locally engraved and epitaxied layers, as presented by Figures 4.23 and 4.24.

In the case of the GTO thyristor (Figure 4.23), the thick layer intended to keep the blocking voltage under direct polarization is P-type. It is in most cases epitaxied on a P-type layer used to stop the electric field under direct blocking voltage in order to make the component robust against digging. (Note, the presence of this layer makes the structure asymmetric because it does not allow the switch to withstand a strong reverse polarization voltage). The P layer itself is deposited on the N^+-type substrate (or an intermediate N^+-type epitaxy to better control the quality of the material, including the PN^+ junction).

The N base epitaxy is about a few μm thick and is doped to about 10^{17} cm^{-3}. The P^+ anode emitter is from a final P^+-type layer engraved and then localy filed over its entire depth delineating the anode areas (usually fingers from 20 to 30 μm wide). The underlying N layer is thus laid bare, and can be localy N^+-type doped and metallized to make the trigger ohmic contact between each anode finger. This makes inter-digitations of the anode and the trigger (widely studied for silicon devices), which improves the performance of the switch, especially during the transitional

phases of ignition and blocking. Different techniques for protecting against the premature breakdown of the NP^- junction at the periphery of the component under heavy direct bias were used: by mesa with plasma etching of the material throughout all the P^- base, by niche etched into the N base (of slightly greater height than the thickness of the layer), which will play the role of custody floating rings, or by N-type pocket located in the P layer after plasma etching of the N layer, creating an extension of the lateral NP junction to be protect (as presented on Figure 4.23).

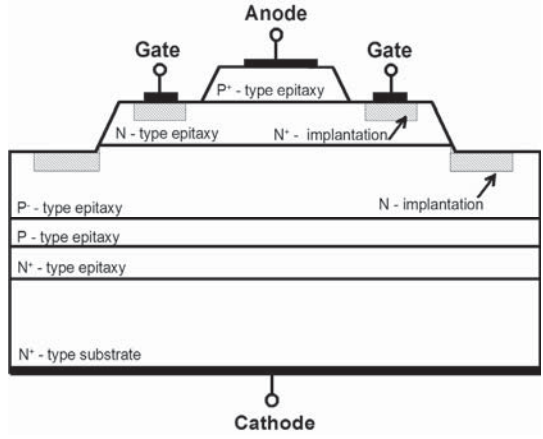


Figure 4.23. *Schematic of an asymmetric, silicon carbide GTO thyristor $P^+NP^-PN^+$ with JTE-type peripheral protection*

The first demonstrators of IGBTs have been made on P^+ type substrates, (SiC-6H then SiC-4H), like their silicon counterparts. A PN^-P^+ bipolar transistor is then combined with a N-channel MOS transistor, as shown in Figure 4.24. The layer of voltage holding in N^- is then deposited on the substrate N^+ (or an intermediate buffer layer N^+ previously epitaxied). The P layer of the canal and N^+ layer of the drain are also made by epitaxy, and trenches are etched in order to create a UMOSFET structure (see section 4.4.1.3.1).

However certain specificities (natural or cyclical) of silicon carbide architecture present the following disadvantages: the P^+ type substrate is difficult to make, and resistive; its injection effectiveness is low at classical temperatures due to the incomplete ionization of acceptors; the PN^-P^+ transistor has a safe operating area smaller than the NP^-N^+ transistor because the ionization coefficient of the holes impact is larger than that of the electrons. These considerations argue in favor of a P channel IGBT structure (despite the lower mobility of holes carriers). A comparative study by simulation of 5 kV structures based on 4H-SiC [WAN 00] concludes that in terms of on-state low voltage drop, P channel IGBT is better suited

for uses between 300 K and 400 K than the N channel component. In terms of switching, the P-channel structure remains faster than the N channel, whatever the temperature of the semiconductor. Polytype 6H is even used by some people to improve the series resistance, (because of better behavior of the SiO2/SiC interface obtained today).

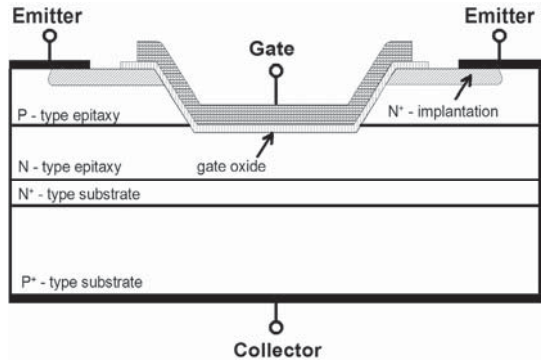


Figure 4.24. *Schematic of an IGBT transistor with N-channel U-MOSFET*

4.4.2.2.1. Performances of GTO and IGBT demonstrators

Table 4.15 provides the main features of several GTO demonstrators tested experimentally, and already shows interesting performance results.

The maximum voltage strength at the moment is 3 kV. Operations under high current densities and high junction temperatures were observed. The maximum demonstrated current rating was 12 A, corresponding to a current density of 700 $A.cm^{-2}$, leading to a direct voltage of 6.5 V at 300°C, obtained for an asymmetric GTO thyristor with voltage strength of 2.6 kV [AGA 00]. The on-state performances at near ambient temperature are less desirable than those at higher temperatures, due to the ionization of acceptors and lengthening of the carrier lifetime with a rising temperature. The SiC GTO are easily trigged and opened, by low amplitude trigger currents.

Structure passivation periphery reference	**Doping / thick-ness of voltage strength layer** (cm^{-3}/µm)	**Anode sec-tion** (cm^{-2})	**Direct voltage strength / temp.** (V/°C)	**Direct current density / temp.** ($A.cm^{-2}$/V/°C)	**Specific differential resistance / current density / temp.** ($m\Omega.cm^2$/ $A.cm^{-2}$/°C)	**Trigger current for switch-on / blocked voltage / temp.** (mA/V/°C)	**Reverse current density / reverse voltage / temp.** (mA/V/°C)
$P^+NP^-N^+$ [PAL 96]	-	$3.2x10^{-3}$ $3.2x10^{-3}$	900/25 700/25	625/3.93 /25 1000/3.6 7 /25	 0.82/300 /25	-/-	$22x10^{-6}$/ 800/27
$P^+NP^-P^+N^+$ triple JTE [FED 00]	-/12	$4.6x10^{-4}$	1100/200	100/12-15 /25 100/4.5-5 /200	#1/500/200 -	- -	10^{-3}/1000 /25 10^{-2}/1000 /200
$P^+NP^-P^+N^+$ SiO_2 engraved floating rings [FUR 00]	$2.1x10^{15}$/ 13 -	$4x10^{-5}$ -	800/25 1200/25	4000/-/25 -	- -	0.4/600 /25 -	10^{-3}/1000 /25 0.2/1100 /25
$P^+NP^-PN^+N^+$4H JTE [AGA 00]	$7-9x10^{14}$ /50	0.0167	2600/25	100/4.25/6 2 100/3.4/30 0 700/6.5/30 0	4/500/100	-	-
$P^+NP^-PN^+N^+$4H JTE [RYU 01]	$7-9x10^{14}$ /50	3.7 $x10^{-3}$	3100/25	100/4.25/6 2 100/3.4/30 0 300/5/25	4/500/100	65/2000 /25	-

Table 4.15. *Major technological and electrical characteristics of GTO demonstrators in SiC-4H*

In addition, the switch-off of current densities up to 4,000 $A.cm^{-2}$ has been reported [FUR 00]. The rise times of the current observed at switch-on decrease with temperature, while switch-off times increase [FUR 00]. For all the structures tested, commutation times are less than a few hundred nanoseconds, including at high temperature (300°C), thus demonstrating the rapidity of these switches.

Table 4.16 provides the main characteristics of experimental IGBTs discovered so far.

Structure polytype periphery reference	**Doping / thickness of voltage strength layer** (cm^{-3}/µm)	**Emitter section** (cm^2)	**Direct voltage strength / temp.** (V/°C)	**Direct current density / direct voltage / temp.** ($A.cm^{-2}$/V/°C)	**Specific differential resistance / current density / temp.** ($m\Omega.cm^2$/ $A.cm^{-2}$/°C)	**Grid threshold voltage / direct current density / temp.** ($V/mA.cm^{-2}$ /°C)
P^+NP^- PN^+ UMOS P channel 4H MESA [SIN 99]	$5x10^{15}$/10	0.02	85/-	1.25/-14/25 70/-14/300 (for V_{GE}=-36 V)	32000/-/25 226/-/350	-29/-/25 -22/-/350
P^+NP^- PN^+ UMOS P channel 6H JTE [RYU 00]	$5x10^{15}$/15	0.02	400/25	15/-10/25 100/-10/400 (for V_{GE}=-30 V)	431/6/25 80/35/400 (for V_{GE}=-30 V and V_{CE}=-5 V)	-10/1/25 -4/1/400 (for V_{CE}=-5V)

Table 4.16. *Major technological and electrical characteristics of IGBT demonstrators in a SiC-6H and 4H*

The voltage ratings of the first IGBTs demonstrators in SiC are low, due to the use of relatively thin films. The direct performances remain modest, especially at room temperature: the highest current densities (100 $A.cm^{-2}$) are measured for the highest test temperature (which corresponds to a current of 2 Amps obtained at 400°C [RYU 00]). The SiC MOSFETs structures cannot currently allow low voltage commands for P channel IGBTs.

4.4.2.2.2. Other structures

In the same spirit that led to IGBT (MCT, MOS controlled thyristor and other) structures being developed on silicon, studies are appearing (essentially by simulation) to assess the performance of silicon carbide components. These studies involve a bipolar structure together with a “drive” structure, so as to exploit the best characteristics of both parties while avoiding their disadvantages. A GMT (gated

MOS transistor) with an architecture of 5 kV is proposed and compared to the N channel and P channel IGBT structures [TAN 00] in order to overcome the compromise between on-state resistance and safe operating area, and eliminate the problem of the parasitic thyristor, imposed by the SiC IGBT structures.

Note that published research on the SiC $N^+PN^-N^+$ bipolar power transistor were, in the past, even rarer than those on IGBTs, more or less guided by the experience of silicon (where this "kind" of large power system gradually disappeared). The demonstrated speed of SiC bipolar structures (as seen previously with diodes and GTOs), and progress in mastering the technology (on which the current gain depends) encourages researchers reconsideration [HUA 00]. Several papers on the power bipolar transistor were proposed at the international conference on silicon carbide ICSCRM'2001, while none were presented for the IGBT transistor.

Many other structures are certainly possible or able to be combined, and there substantial work remains in the area of design for these types of high-power components, taking into account the differences between Si and SiC (which can play a vital role in the strengths of the devices), and also development of optimized tools for both manufacturing and simulation.

4.4.2.2.3. Comparison with silicon

The current performances of the first GTO thyristors and IGBT transistor demonstrators in SiC (with low currents as in the case of diodes, but also low breakdown voltages) does not allow for a direct comparison with existing commercial devices.

Figure 4.25, representing the voltage and current ratings of silicon components for high power applications, and their developments over recent years, is proposed here to predict how long evolution of a pipeline can take, with impressive progression between the original structures and the latest designs. Since this figure was presented in 1999 [DED 99], the situation has further evolved with, for example, the emergence of IGBTs 6.5 kV/600 A onto the market.

It seems even more obvious to say that several years of efforts are still needed to develop a powerful switch benefiting from the advantages of the SiC semiconductor. All elements in the chain must be reinforced, to create higher quality electronic materials, high-voltage and high temperature housing, passing through the various stages of design and manufacturing optimization.

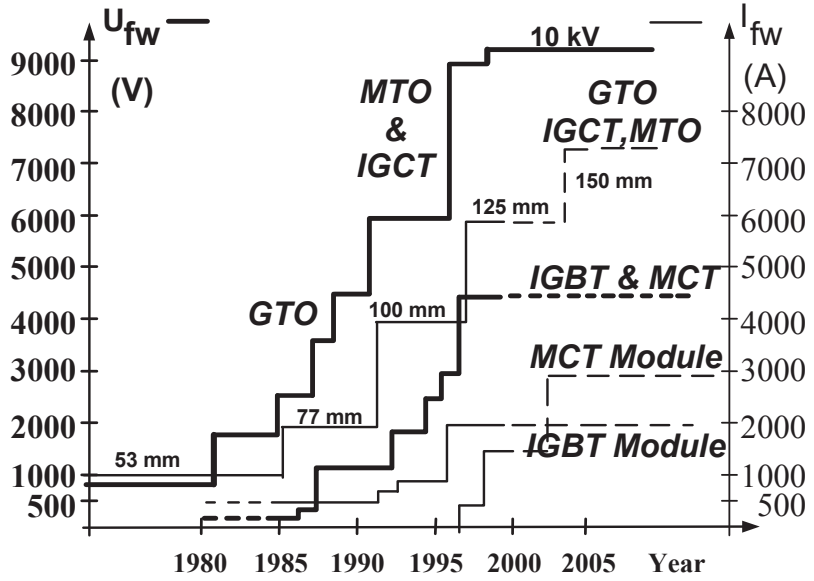


Figure 4.25. *Areas of voltages and currents covered by different families of powerful silicon components and evolution over time [DED 99]. Relevant acronyms: IGBT, insulated gate bipolar transistor; MCT, MOS controlled thyristor; GTO, gate turn-off thyristor; MTO, MOS-turn-off thyristor; IGCT, integrated gate commutated thyristor*

4.4.2.3. *Potential applications*

Given the theoretical potential of very high voltage and high power silicon carbide components, and performances offered by the first demonstrators (including bipolar diodes and GTO thyristors), the first potential applications are certainly in the areas of production, conversion, and transmission of energy, especially since the current trend toward decentralized sources of production generates increased or new demands (multiplication of electrical power distribution stations, network management, quality, etc.). The emergence of solid state electronic devices in systems up until now outside of their bearings, represents a step towards greater flexibility, controllability, even "intelligence" of these ensembles. Power electronics is already present on most of the systems (alternators, engine control, etc.). The downsizing of power electronics (by avoiding serial connections of components, reducing coolers and filters) will allow its direct integration on the machine.

The reduction of losses, and the increase in eligible temperatures (under the condition of integration issue resolution) are also relevant for the field of transport,

from electric traction (train, bus, subway, streetcar) and electric propulsion (cruise ship), to the hybrid vehicle.

High-voltage applications based on the generation of very strong current pulses (electromagnetic launchers [ARS 01]), or with lower current (high density lamp ballast) are also affected by the prospective volume reductions and good energy management offered by silicon carbide.

Maintaining high energies also relates naturally to specifications regarding the protection of electrical circuits. This feature applies to all types of applications: those with very high voltage, as in the field of energy mentioned above with special needs in parallel protection devices, and those at low voltage for domestic installations, for example those requiring series protection devices.

The prospective use of silicon carbide for the series protection of facilities on a low voltage network is discussed in the following section.

4.4.3. *High energy SiC components for series protection systems*

The series protection equipment of electrical circuits, including that supplied by the home network, is currently electro-mechanical systems. No current semiconductor component is able to both; have a sufficiently low resistance under normal operation, and be able to dissipate the energy during a short-circuit on the load. The silicon in particular can not withstand a sufficiently long period of self-heating, produced by the simultaneous presence of short-circuit (even of a few amps) and the voltage at its terminals. Such applications would seem to be within the scope of the properties of silicon carbide, particularly through its high temperature features and its good thermal conductivity.

Figure 4.26 shows a proposed current limiting structure, adapted to the series protection on the low voltage network (voltage strength: 600 V, rated current: 5 A) [NAL 01]. Operating on the same principle the JFET structure (see section 4.4.1.3.2), this structure is normally under a low V_{DS} voltage. Increased V_{DS} voltage causes pinching of the conduction path by the JFET effect, producing current saturation, the following current decline is the result of the semiconductor self-heating, due to the simultaneous presence of high current and high voltage. A thermal runaway may follow if the overheating is created locally.

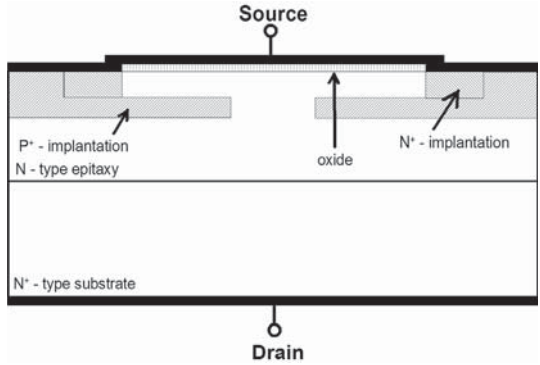


Figure 4.26. *Schematic of a unipolar SiC component proposed for use as a current limiteron low voltage networks [NAL 01]*

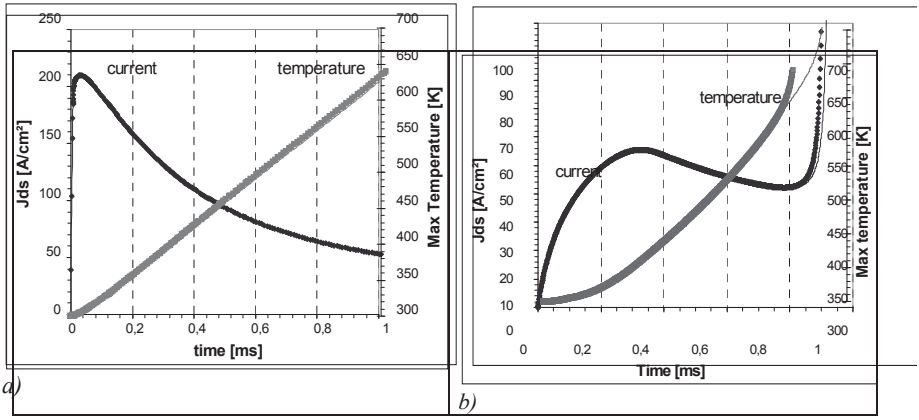


Figure 4.27. *a) Current density and maximum temperature in the 4H-SiC component, as a function of time, the application of a linear increasing voltage (from 0 V (at t=0 ms) to 500 V (at t=1 ms)). between Drain and Source terminals resulting from (The main parameters of the structure are: $N_{epi}=10^{16}$ cm^{-3}, $W_{epi}=6$ µm, $X_{Jcanal}=0.2$ µm, $L_{canal}=4$ µm, $N_{canal}=2x10^{17}$ cm^{-3}, $T_{amb}=300$ K, $R_{Thcomp/ambinferior)}=0.5$ K.cm^2.W^{-1}, $R_{Thcomp/amb(superior)}=0.5$ K.cm^2.W^{-1}) b) Idem for a 600 V silicon MOSFET (implanted channel and epitaxy thickness of 40 µm doped at 10^{14} cm^{-3}), with the aforementioned constraints, leading to the emergence of a thermal runaway after 0.9 ms (extracted from [NAL 00])*

Figure 4.27 shows the assessment of the maximum temperatures inside devices at 600 V in 4H-SiC and Si, obtained by simulation (using the DESSIS program from ISE TCAD [ISE 98]) of their electro-thermal behavior as a result of a linear rise in the voltage applied to the terminals up, to 500 V after a millisecond (only cooling by the underside is considered, with a thermal resistance of 0.5 K.cm^2.W^{-1} between the

component and the atmosphere) [NAL 00]. An acceptable compromise between low series resistance under normal operation and no thermal runaway in current limiting operation cannot be achieved with the simulated silicon structure (on the principle of a 600 V MOSFET with implemented channel), however, can be observed for the 4H silicon carbide structure. The latter shows a stable electrical behavior despite internal locally temperatures rising up to 350°C, and a power increase up to 25 kW.cm^{-2} after 1 ms (for this example).

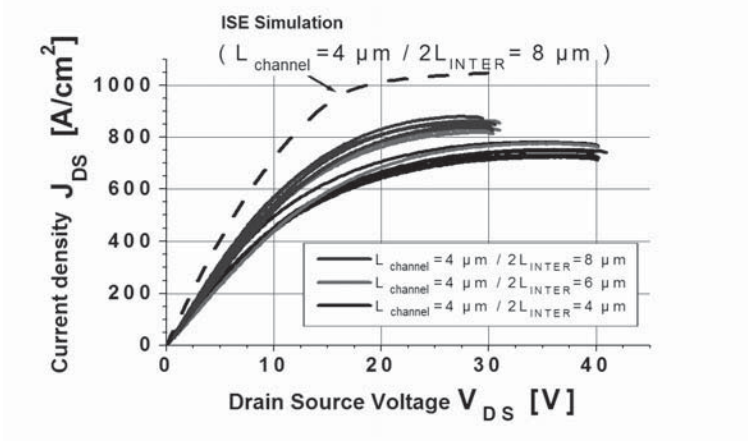


Figure 4.28. *Experimental characteristics $J_{DS}(V_{DS})$ of current limiting demonstrators for 600 V / 5 A applications in SiC-4H (measures on wafer, by testing under peaks at room temperature, without control of self-heating). The simulated characteristic considers a mobility of electrons in the channel of 400 cm^2.V^{-1}.s and no charge at the SiO_2/SiC interface (from [GOD 01])*

Figure 4.28 shows a series of experimental characteristics $J_{DS}(V_{DS})$ obtained from the first demonstrators made in 4H-SiC (peripheral protection is provided by custody P^+ rings made at the same time as the P^+ areas) [GOD 01]. Strong current densities are reached (900 A.cm^{-2}) in the saturation regime, and the experimental specific resistance to linear operation (characterizing the operation without default) at room temperature is low, 13 mΩ.cm^2 on these structures with non-optimal ohmic contacts. These initial achievements validate the concept of current limitation power, being fairly close to the simulation results; also the feasibility of such structures in 4H-SiC with a simple technology encourages further performances.

Current limitation in the alternative network is achievable by setting a "tumble" series of two components (see Figure 4.26). The series resistance, and especially the lack of cut-off power of this solution will not be able to completely eliminate

electro-mechanical breakers from electrical installations, however, a part can be removed, design size can be reduced, and lifetime can be prolonged by reducing peak values of the currents to be interrupted. Structures in SiC including control electrodes are also envisaged [TOU 01]. Compared with the classic solution of the fuse for example, they have the added advantage of not requiring human intervention following a default (thus reducing maintenance on some systems). The introduction of controllable electronic devices in the home automation sector could also provide the possibility of expanding the functions of devices beyond mere protection, by combining these new types of components with interactive control systems.

Optimization of technology (including box setting), and an overall analysis of facilities, are both still necessary before seeing the emergence of these new components on the market, which is a desired advancement while there is no competition of semiconductor based devices.

4.5. Conclusion

The silicon carbide (SiC) is a material with proven and potential applications, almost as numerous as its various forms. Used from a long time as a composite or abrasive material because of its mechanical and chemical properties in polycrystalline state, also acknowledged more recently in jewellery for its crystalline beauty, SiC has also been marketed for the first time as semiconductor for blue light-emitting diodes (where it is still present today, as a substrate for the active gallium nitride). An increasing number of research studies are being undertaken examining the electronic applications of SiC semiconductors in hostile environments (such as sensors at very high temperature, radiation detectors, etc.), in the field of optoelectronics, and in the field of power electronics. Together with its high prohibited energy band, its critical electric field and its good thermal and electronic properties, the SiC semiconductor provides an attractive solution for meeting the new requirements of tomorrow's power systems.

To deal with applications of silicon carbide in power electronics, we felt it was necessary to give an overview regarding this "new" semiconductor material: its main properties and associated potentials, its technology and degree of maturity, the structures obtained so far and their performances, compared with the current power devices based on silicon.

First of all, remember that a few points on a technical level maintain doubts about the future of some branches of power components based on silicon carbide. The first is the quality of the material upon which in turn manufacturing impacts upon the yield (of substrates, epitaxy and components), the feasibility of high

current devices, and ultimately the reliability of the functions carried out and of course their cost. The second, is the existence of an insulating grid adapted to the operation conditions of SiC, and maintaining a good interface, in order to benefit from the theoretical advantages of this semiconductor. The third point relates to obtaining operational and reliable, switches with isolated commands. The same issue arises about the surface passivation of SiC, and more generally in terms of the materials needed to implement housing, including components intended to operate at high junction temperature (i.e. above 200°C). In addition to this blocking points, efforts are still required to improve the performance of components based on SiC and reinforce the technical and economic superiority of the systems using it. These improvements are particularly at the manufacturing level: such as doping control, increased speeds of low residual doping epitaxy, and the mastery of lifetime; but also the physical modelling of these new components. In addition, research also undertaken for the optimal design of their architectures and those of the converters which implement them, and their packaging, is continuing.

In terms of applications and expected progress, it is clear that silicon carbide is theoretically adapted, and probably also necessary to remain inline with the new requirements of electronic power systems: less energy consumption, more power supplied, more miniaturization (or "integration"), more functions (or "intelligence"), and more reliability. Current demonstrators already show (by structures which currently drive tens of amps) SiC's potential to extend the ratings in voltage, frequency and energy, beyond what silicon can achieve. This is done by reducing conduction and switching losses (by reducing or abolishing their causes), or by raising the threshold of tolerance of those losses by the semiconductor (through a higher allowed operating temperature).

The "high voltage" SiC Schottky diode, already a reality on the marketplace for a voltage range up to 600 V, corresponds to the first case (significant reduction of losses). The studies of implementation, in competition with bipolar silicon diode, show that its favored area of use is schematics, involving hard commutation at frequencies above 100 kHz. The extent of the voltage forecast range in the SiC Schottky diode family is 2-3kV within the horizon of two to three years. The high current ratings do not need necessarily large dimensions for substrates, as the Schottky diode is perfectly suited to the parallel setting. The maximum junction temperature of such components is still "classic", less than 200°C. The normally open-switch associated with the very fast silicon carbide diode remains, to this day, silicon; the emergence of a commercial component SiC MOSFET is postponed due to the technological difficulties mentioned above. New circuit topologies will probably emerge in order to benefit from the very interesting performance of "normally closed" switches such as SiC JFETs, which could also be available within two to three years. Note that MESFET type transistors dedicated to UHF and power microwave applications are already on the market (being based on a material whose

characteristics are easier to make). The exploitation of silicon carbide properties to significantly extend the voltage levels of lateral conduction structures (SiC solid material, or SiCOI, etc.), allowing the realization of genuine power integrated circuits, is another prospective major interest for low voltage applications, whose reality is still dependent on the technological advances of each component.

The issue of these devices is thus in the context of reducing dimensions (radiators, filters); increasing efficiencies of conversion, which promote miniaturization and autonomy of the systems of low and medium voltage; and reducing costs (including maintenance and infrastructure).

For applications beyond 4-5 kV wishing to increase their operating frequency, demonstrators in bipolar SiC diodes have shown their superiority to the existing competition (fast silicon bipolar diodes), in terms of speed, of direct current density, of temperature, and therefore power dissipation ability. Aspects concerning the operational reliability and availability of high current ratings (related to the quality of the material) remain unclarified. The marketing forecast for these components is, in the favorable case, estimated at five years at least. The emergence of SiC switches in this range of voltage and for high power applications (such as bipolar transistors, GTO thyristors, or their combination with command by gate isolated structures (IGBT transistors, MGT transistors, or else to be invented, etc.) is at best feasible in a similar period. Demonstrators remain today at low voltage and current ratings, but already attest their switching speed, their temperature strength and high current density, confirming the hopes of increasing the power density of systems.

Thus, there are a number of areas accessible to silicon carbide for which there is no competition, at least in the form of semiconductors components: such as applications at very high voltage (19 kV diodes with very low current have been demonstrated); applications under high temperatures; and static protection systems, with proof of the robustness under high energy of some structures (such as 600 V JFET transistors for the current limitation on the low-voltage grid). The consequences can look similar in this case to the famous 1960s revolution in power electronics; the introduction of semiconductors being in fact a considerable progress in terms of flexibility of command and control of systems, interactivity (even “communication”) with their environment, and expanding the scope of their actions.

These are encouraging results and motivating prospects for the progress and innovation of domestic or industrial facilities, individual or collective transportation, production and management of energy, and telecommunications; for which fascinating research subjects remain to be discovered and discussed.

4.6. Acknowledgments

We can not conclude this chapter without expressing our gratitude to the people without whom we could not have written the lines above.

Our sincere thanks go first to men who, in the late 1980s, were at the foundation of French research dedicated to power components in SiC: mainly, Jean-Pierre Chante (Professor INSA Lyon), Pierre Merle (Professor at the University of Montpellier and head of the Group of Industrial and Research Centres in Power Electronics – GIRCEP), Michel Amiet (Officer of Technical Strategies and Common Technologies of the DGA) and Christian Parnière (former Director of the Research Group in Electronics at Schneider Electric).

We also deeply appreciate the research contribution of the cited authors: some of whose results have been repeated in this chapter.

We are also very grateful to the various people who have directly contributed to the results presented in this chapter, or who have spent time to discuss, correct its contents, or who have "supported" (in all senses of the term) this work, including: the "SiC" team members of AMPERE (Lyon), Frédéric Lanois (STMicroelectronics Tours), Hervé Morel (AMPERE), Henri Schneider (LAAS Toulouse), and also not forgetting our beloved families.

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Chapter 5

Capacitors for Power Electronics

5.1. Introduction

Capacitors are essential components of power electronics systems. They can easily reach or exceed one third of the total volume of static converters, of which they are often the weak point. Their primary applications are in storage circuits, discharge, decoupling, filtering, resonance, snubbers, EMI shielding, etc.

The nature and the properties of the various materials used to build capacitors (dielectric, metallization, connections) have a direct influence on their properties. There are mainly three families of capacitors, each of them addressing a specific application or requirement. These are: metallized films capacitors, electrochemical or electrolytic capacitors and ceramic capacitors.

Historically, the first capacitors to have been used in electronics and in power engineering were paper capacitors. They were later abandoned in to low-voltage applications, for electrolytic capacitors and synthetic film capacitors. The paper based capacitors are still widely used when impregnated with a dielectric liquid that gives them sufficient voltage strength for applications for medium and high voltages. Finally, ceramic capacitors, using materials with very high dielectric constants, then appeared and are constantly finding new fields of applications.

Figure 5.1 summarizes the orders of magnitude of capacity of each of these capacitors, and their development today.

Chapter written by Abderrahmane BÉROUAL, Sophie GUILLEMET-FRITSCH and Thierry LEBEY.

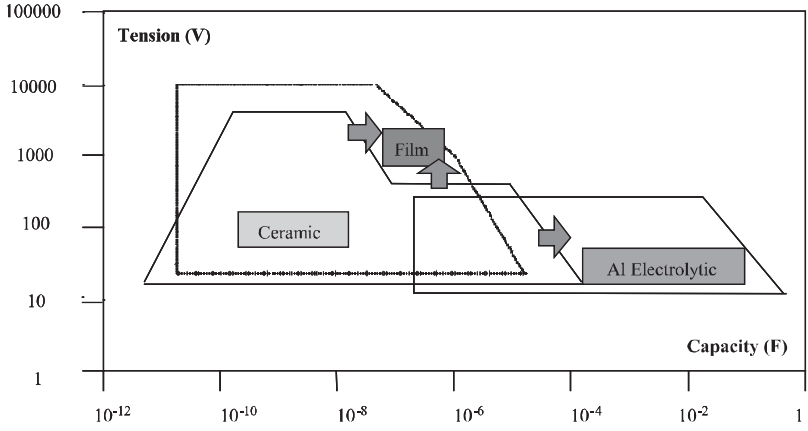

Figure 5.1. *Range of voltages and capacities of the different types of capacitors used in power electronics*

In the first part, we recall the main definitions and characteristics of such components as well as their constraints. We then describe in detail each of the different types. We will particularly expand on ceramic materials. It seems important to emphasize these materials, on the one hand because of their possible applications for hybrid integration and the development of new specific components; on the other hand because a large number of books and works are already devoted to films and electrolyte-type capacitors. At the end of the chapter we give a bibliography of useful references. In the penultimate section, we briefly describe some specific examples of applications of capacitors in power electronics. Finally, in conclusion, we will try to give trends for research and development (R&D) in the field of capacitors.

5.2. The various components of the capacitor – description

Whatever its type, a capacitor schematically consists of two conductive armatures separated by a dielectric material and linked by connections to the terminals of the external circuit (Figure 5.2). Applying a voltage to the terminals of the capacitor creates an electric field between the two armatures causing the polarization of dielectric and the storage of electrostatic energy. The polarization phenomena are depicted by the appearance of displacement currents within the dielectric and conduction currents in the armatures. These are collected by the connections and move towards the terminals of the capacitor. Hence, the electrical behavior of a capacitor cannot be reduced to the phenomena appearing in the

dielectric material. The operation of a capacitor depends on physical phenomena occurring in its three components namely the dielectric material, the armatures and the connections.

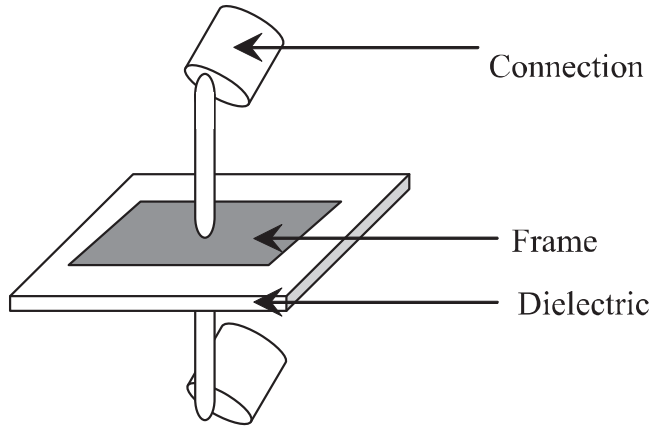

Figure 5.2. *Schematic description of a capacitor*

5.2.1. *The dielectric material*

A dielectric material is a substance able to be polarized when submitted to an electric field. It stores electrostatic energy whose density, for linear homogenous isotropic materials, is given by the relation:

$$w_e = (½)\ \varepsilon_0\ \varepsilon_r\ E^2$$

ε_0, ε_r and E respectively represent the permittivity of a vacuum, the relative permittivity of the dielectric material and the electric field. The density of stored energy is all the more high as the permittivity and/or the electric field are high.

5.2.2. *The armatures*

The armatures of a capacitor are used to apply an electric field to the dielectric and to collect current to drive it to connections. They also help to drive the heat outside of capacitor. Two large families of armatures exist. The so-called full armatures are separated from the dielectric. The armatures can also be made of a thin layer of metal deposited under vacuum on the dielectric material; these capacitors are called metallized armatures. In the case of so-called self-healing capacitors (mainly based on thin films), these armatures also play the role of a fuse. During a

local breakdown of the dielectric material, they evaporate around the default (open circuit), thus avoiding the failure of the capacitor.

5.2.3. *Technology of capacitors*

The capacity of a plane capacitor is proportional to the permittivity of the dielectric material, the surface of the armatures and inversely proportional to the thickness of the dielectric. Thus, to obtain "geometrically" important capacities with acceptable dimensions, the dielectric folds on itself to achieve the geometry shown in Figure 5.3 where armatures alternate with dielectric layers.

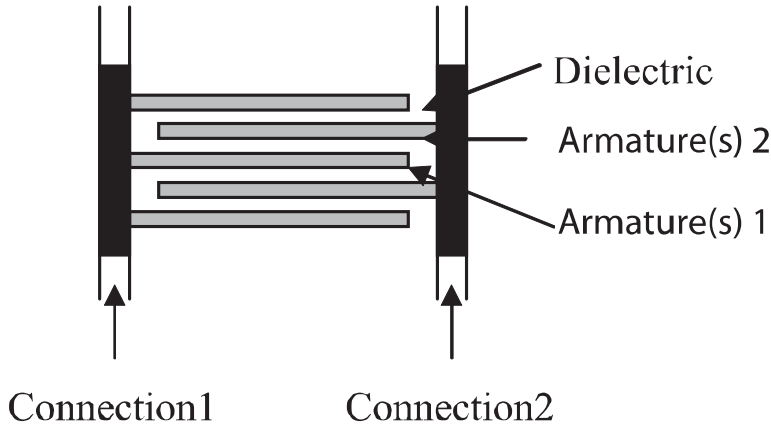

Figure 5.3. *Outline of a real capacitor*

In practice, this geometry is achieved either by stacking discontinuous dielectric layers (chervil technologies) (Figure 5.4), either by winding around an insulating core metallized dielectric films (dielectric and armatures) or winding all together dielectric films and metal sheets (frames) (Figure 5.5). The chervil technologies are particularly suitable for rigid dielectrics (ceramics, mica), but they are sometimes used for plastic dielectrics. The wound capacitors are only achieved with flexible materials (paper, polymers).

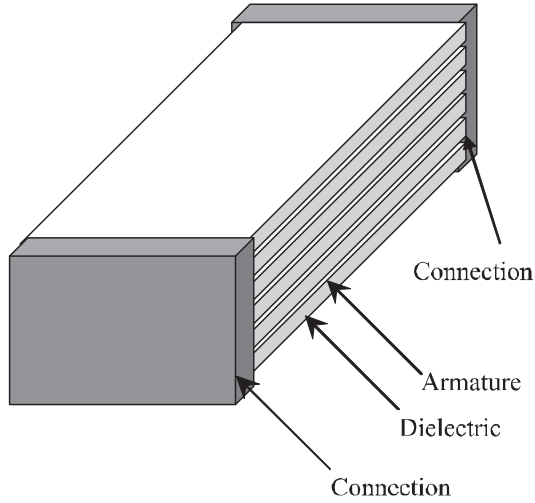

Figure 5.4. *"Chervil" technology*

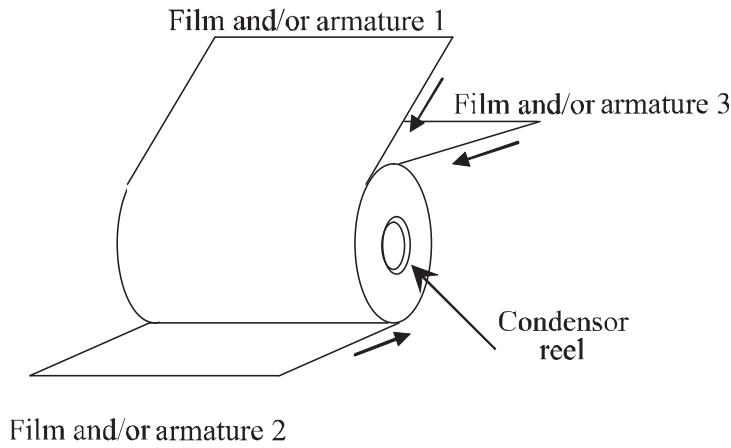

Figure 5.5. *Wound capacitor*

5.2.4. *Connections*

The link between the capacitor armatures and the external circuit is made through connection wires. The junction between the armatures and these connection

wires depends on the type of armatures. It is created either through metal tabs (the contact is made at one point) or by welding all around winding (case of capacitors with overflowing armatures).

In the case of armatures of small thicknesses (case of metallized films), it must be ensured that the dielectric film is not damaged (by heating) during soldering operations (projection of molten metal for setting in parallel the elementary capacities formed by the capacitor coils in the case of a wound coil) and welding of connection wires. The nature and disposition of connection wires (internal or external return with regards to the core in wound capacitors) play a significant role in the distribution of currents and the value of the series inductor of the capacitor.

5.3. Stresses in a capacitor

When using a capacitor, it is important to take into account the constraints endured during its operation. Knowledge of the role it should play, qualities it must possess and stresses to which it will be submitted are of vital importance for an optimal design to the application. Before blaming the capacitor for the shortcomings of a system, we must ensure that its choice fits the requirements and the function it should meet. However, the use of a capacitor in power electronics applications is submitted to a number of constraints related to the waveform and to the amplitude of the applied voltage applied and the characteristics of the dielectric material, armatures and connections.

5.3.1. *Stresses related to the voltage magnitude*

One of the important properties of a capacitor concerns its dielectric strength. It is a complex problem because the breakdown may have very different origins. The voltage strength of a capacitor depends not only on the disruptive strength of the dielectric but also on the temperature, the magnitude and the waveform of the applied voltage, and on its packaging (connectors and armatures). The latter have a direct influence on the distribution of the electric field applied to the dielectric. They can lead to an enhancements of the local electrical field, especially along the metallization. These fields are all the more intense as the thickness and/or the radius of curvature of the armatures are low. Unless using other tricks (increase of the armatures' thickness and of the curvature radius of edges), the dielectric cannot be used close to its intrinsic dielectric strength. The operating voltage of a capacitor must be less than a value of partial or total destruction of the dielectric. This is called "derating" (Figure 5.6).

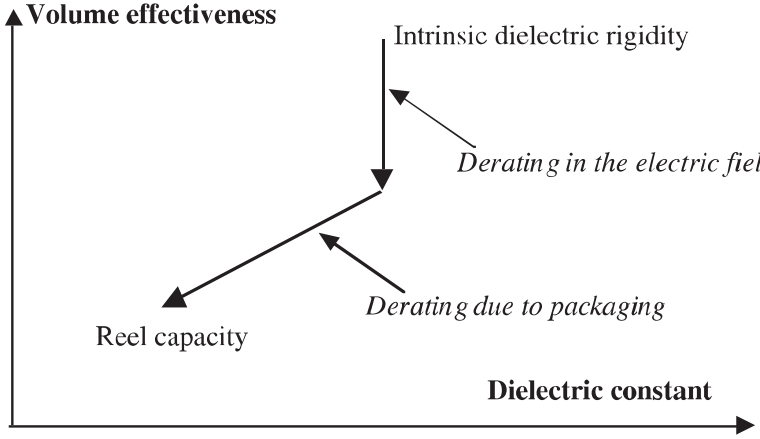

Figure 5.6. *Example of derating of a capacitor*

5.3.2. *Losses and drift of capacity*

Applying an alternative voltage to the terminals of a capacitor may in certain circumstances lead to heating and therefore loss of energy. These losses depend on the voltage waveform, the nature of the frames and the environment of the capacitor.

There are two types of losses:

– ohmic: these are due to armatures and connections, they depend on temperature and frequency. The use of thick armatures and large contact surface between the frames and connections minimize them;

– dielectric: these are the result of conduction in the dielectric (leakage current, losses by conduction) and polarization phenomena in the dielectric, following the application of electric field (losses by polarization). These dielectric losses lead to the drift of the capacity of the capacitor.

The losses in a capacitor are often represented by electrical equivalent circuits, in series or parallel (Figure 5.7). Such representations are only valid for sinusoidal operation of angular frequency ω. In Figure 5.7a (parallel equivalent circuit), resistors R_a and R_{dp} correspond to the ohmic and dielectric losses. The concept of dielectric losses factor $\tan \delta_d$ (δ_d is the complementary angle to the angle of phase shift between current and voltage) is also used to characterize a capacitor (Figure 5.7b). Moving from a parallel equivalent circuit to a series equivalent circuit (R_a, R_{ds}, C_s) (Figure 5.7c) conforms to relations:

$$\tan \delta_d = (1/C_p R_{ds} \omega) = C_s R_{ds} \omega$$

with:

$$C_s = C_p (1 + \tan^2 \delta_d) \text{ and } R_{ds} = R_{dp} [\tan^2 \delta_d/(1 + \tan^2 \delta_d)]$$

Total losses (ohmic and dielectric) in a capacitor are often described using the notion of equivalent series resistance $R_{se} = R_{ds} + R_a$, or global losses:

$$\tan\delta = \tan\delta_d + R_a C_s \omega$$

As the parameters of all the representations above are frequency dependent, their use with non-sinusoidal voltages, which is often the case in power electronics, is possible only through frequency splitting (Fourier transforms). However, it is rare that the principle of superposition principle applies, since the response of dielectric materials with frequency is rarely linear.

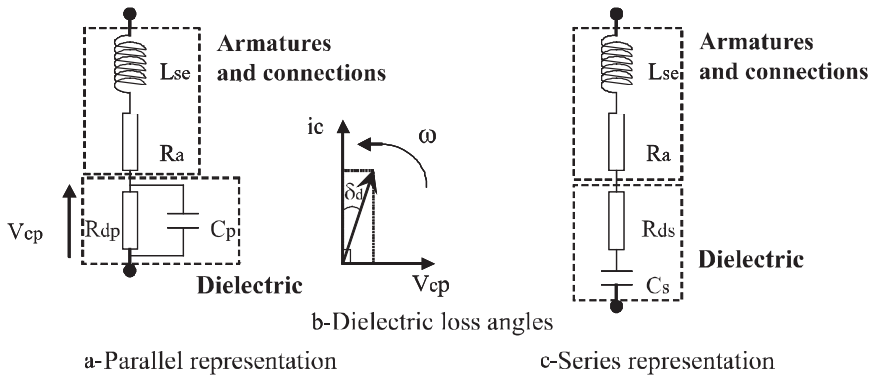

Figure 5.7. *Equivalent electrical circuit of a capacitor under sinusoidal operation*

5.3.3. *Thermal stresses*

If the losses generated in the capacitor are larger than the amount of heat it can dissipate, a heat imbalance occurs, which can lead to the failure of the capacitor. Dielectrics are generally excellent insulators, electrical as well as thermal. It is therefore difficult to dissipate the heat. In an attempt to solve this problem, different techniques are used: space around the capacitor, use of appropriate color for housing, use of heat spreaders, etc.

As mentioned previously, the losses generated in a capacitor may be determined in the first approximation, through the split of the electrical signals in their harmonic components and by calculating the average power dissipated by each component. For a harmonic voltage of angular frequency ω, knowledge of dielectric losses factor $\tan \delta_d$ is used to evaluate the power $P_{average}$ dissipated in the dielectric:

$$P_{average} = C\, \omega\, V_{rms}^2 \tan \delta_d$$

C and V_{rms} are respectively the capacity of the capacitor at angular frequency ω and the effective value of the voltage applied to its terminals.

For a plane capacitor, the power dissipated in the dielectric is:

$$P_{average} = (\varepsilon_0\, \varepsilon_r\, A/e)\, \omega\, V_{rms}^2 \tan \delta_d$$

A, ε_r and e are respectively the surface of the armatures, the relative dielectric permittivity and its thickness.

The amount of heat removed by natural convection is proportional to the surface it exposes to the environment. The heating of capacitor ΔT compared to the atmosphere is such that:

$$\Delta T \;\alpha\; (\varepsilon_r/e)\, \omega\, V_{rms}^2 \tan \delta_d$$

Thus, the heating of the capacitor decreases with the thickness of the dielectric and increases with permittivity and frequency. The ohmic induced losses, i.e. the contribution of power P_a dissipated in the resistance R_a linked to the current in armatures and connections, have to be added to the heating.

5.3.4. *Electromechanical stresses*

When a voltage is applied to a capacitor, armatures with opposed charges attract each other through a Coulomb force that derives from the electrostatic energy stored in the capacitor. The result is a compression of the dielectric. These forces may cause, if the material allows, a deformation of the dielectric material and may lead to a reduction of its dielectric strength. For an alternative voltage, the compressive force is itself alternative, which can lead to mechanical fatigue of the dielectric resulting in an electromechanical failure.

5.3.5. *Electromagnetic constraints*

The magnetic forces acting between armatures or between connections of the capacitor may have main consequences on current collection. These forces are proportional to the square of the current (i^2). They also depend on the geometry of the system, in particular, they are inversely proportional to the distance between armatures. In a given application, these forces are even more important as the peak value of the current applied to the capacitor is high. In capacitors intended to provide high current pulses, particular attention must be given to the design of armatures and output connections to avoid tearing. On the other hand, self inductance of a capacitor (due to its armatures and its connections) can lead to overvoltages in its terminals at large variations in current (di/dt) or frequency. It may also have serious consequences on the life of the component.

5.4. Film capacitors

As mentioned previously, film capacitors can be either full armatures, metallized or dielectric flexible materials.

5.4.1. *Armatures*

5.4.1.1. *Full armatures*

Full armatures can be overflowing or centered. In the case of overflowing full armatures, metal sheets are sometimes placed on the right or left of the longitudinal axis of the winding, leaving a margin of a few millimeters on each side (Figure 5.8). The connections are made by compression of metallic sheets or projection of a metal that is welded to the connection wires.

In the case of a system with centered full armatures, armatures are centered in the longitudinal axis of dielectric films (Figure 5.9). Each armature has a width smaller than that of the dielectric to maintain a margin on each side of the winding. The output connections are created using metal tears connected to each armature. These strips are then linked together to be connected to the terminals of the capacitor.

The orders of magnitude of frames and film dimensions are identical in both systems. The thickness of each frame is between 1 and 10 μm and the thickness of the plastic film from a few μm to 20 μm, according to the effective current and voltage to be held. For high values of the nominal voltage, several dielectric films of low thickness are preferred to one thick film.

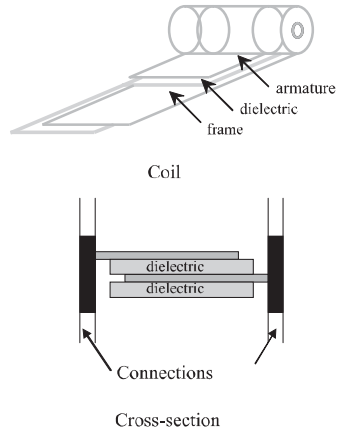

Figure 5.8. *Structure of a capacitor with overflowing full armatures*

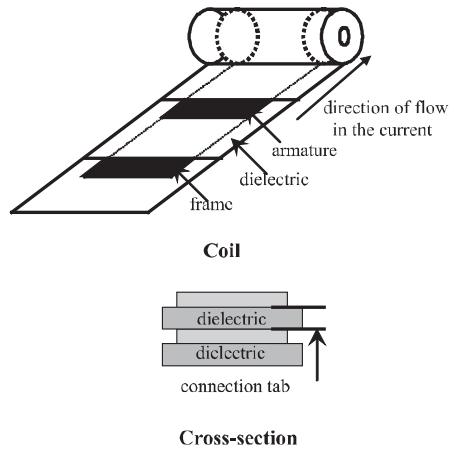

Figure 5.9. *Structure of a capacitor with centered full armatures*

5.4.1.2. *Metallized armatures*

The armatures of a metallized capacitor are obtained by deposition, under vacuum on the dielectric film, of a thin layer of metal (aluminum or zinc) of ten to a few tens of nm thickness. While operating, if a short circuit appears at a point in the dielectric, the thickness of the coating is such that the energy produced by the local breakdown of the dialectic material causes evaporation of the metallization around it. The default is therefore isolated from the healthy part of the capacitor at a cost of

a slight decrease in capacity that it is self-healing. As for the thickness of the dielectric, it is between 5 and 12 μm (Figure 5.10).

The metallization of a dielectric is carried out so as to leave a margin of insulation of a few mm on each side of the winding to prevent short circuits. On the opposite side of this margin, the thickness of the deposit is being strengthened in order to facilitate the connection to the *armatures* (Figure 5.11).

To achieve the capacitor, two metallized films are wound around an insulating support (core) so that their strengthened edges are not on the same side of winding. A lateral shift between the two films facilitates the collection of currents, i.e. contact with the coating (metallic coating obtained by projecting a molten metal) on both sides of the winding. The metallization of film 1 is in contact with the coating (also called "shooping") on one side of the winding and metallization of film 2 is in contact with the other side. The coating connects in parallel all of the winding turns. The output connections are made by welding two wires on coatings on both sides of winding.

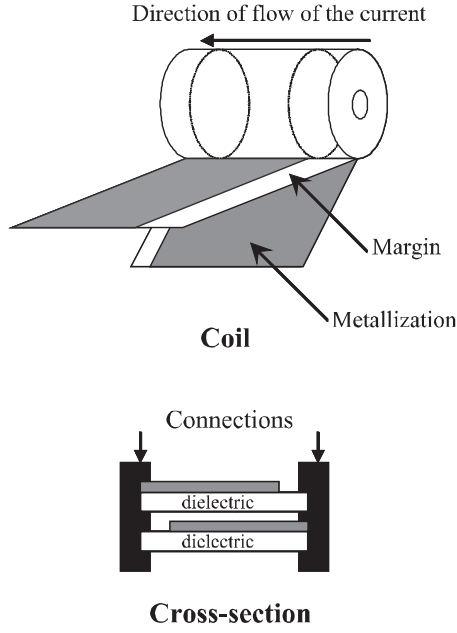

Figure 5.10. *Structure of a capacitor with metallized armatures*

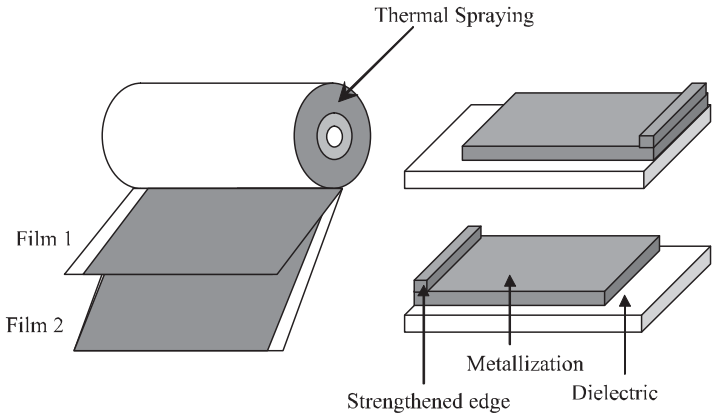

Figure 5.11. *Structure of a capacitor with metallized armatures and strengthened edges*

5.4.2. *Dielectric materials*

The main materials used in the manufacture of film capacitors' films are polypropylene, polyester (polyethylene glycol ethylene, known as Mylar) and polycarbonate. All these materials have nearly the same permittivities. The use of one or the other depends on the operating conditions (mechanical, thermal, etc.). Polyester and polycarbonate can be used between -55°C and 125°C, while polypropylene can be used between -40°C and 100°C (or 85°C). However, polypropylene is the preferred dielectric due to its low cost, the stability of its properties (low losses and low drift of capacity) and its high dielectric strength (around 500 MV/m (500 V/μm!) for films by 10 μm film thickness). All these things make polypropylene widely used.

For high temperature applications, other materials like Teflon or polysulfon are used. They can operate at temperatures above 150°C, but due to their cost, their use is limited.

5.5. Impregnated capacitors

The capacitors with full armatures can also be impregnated. In this case, there are two dielectric materials, a solid and a liquid are used. The liquid dielectric makes it possible to replace the air (or any air gap) across the whole structure of the capacitor and especially at the frame edges, thus avoiding the initiation and development of partial discharges which affect the lifetime of the capacitor.

This impregnation technique was used in the early 20th century with basic materials such as paper and mineral oil (all-paper capacitor). The paper, composed of cellulose, is easily impregnated by mineral oil but has fairly high losses ($10^{-3} < \tan\delta < 10^{-2}$) for normal operating conditions (frequencies and temperatures), so the mean fields for a paper-oil structure are relatively low (around 20 V/μm). The use of polychlorinated biphenyls (PCBs) in the 1930s made possible a service gradient of 20 to 30 V/μm and prolonged the timelife of these capacitors.

Thanks to progress in polymers science, a new generation of capacitors began in 1966 with the use of paper together with polypropylene films whose electrical properties are remarkable (dielectric strength three to five times the one of paper and dielectric losses less than 2×10^{-4}): they are called mixed capacitors. These elements, made of alternating layers of polypropylene and paper, have led to a significant rise in average field service (35 to 40 V/μm), a reduction of losses and an increase of reactive power density, compared to paper capacitors.

New techniques, allowing service operation to a value of up to 50 V/μm, reduced dielectric losses ($\tan\delta \sim 10^{-4}$) and volume, removing the paper, have emerged as a result (in the 1980s): "all-film" polypropylene capacitors. The difficulties encountered for impregnation while removing paper, which served as a wick for impregnation in mixed capacitors have been resolved by the use of rough films and/or corrugated frames leading to a better dissemination of impregnation inside the structure.

The impregnating liquids have also contributed to improve the performance of capacitors. For environmental reasons and public health (toxicity), the use of PCBs has been strictly regulated or even prohibited in some countries. They are gradually being replaced by new liquids or mixtures that meet both environmental and electrical requirements, and are products that have very good dielectric properties and "gassing" properties (i.e. a good ability to absorb gas generated by the action of the electric field or as a result of partial discharges). The main dielectric liquids currently used for impregnation are MDBT (mono-dibenzyl toluene known as UGILEC) and PXE (phenyl xylyl ethane).

5.6. Electrolytic capacitors

The two armatures are, in this type of capacitor, made of metallic sheets (aluminum in general) immersed in a slightly acidic conductive liquid called an electrolyte. For manufacturing, an electrochemical reaction (anode oxidation) is produced between one of the armatures (aluminum foil of thickness between 50 μm and 100 μm), which plays the role of anode and the electrolyte, applying a positive

difference of potential, and this leads to the formation of a thin layer of aluminum oxide (Al_2O_3) with a dielectric constant $\varepsilon_r \sim 8$.

The main feature of these capacitors is to be polarized. The foil and oxide (Al_2O_3) filed over are intended to form the anode and the dielectric of an electrolytic capacitor. It is a system obtained by winding together several different sheets:

– the anode foil with the dielectric layer, which is in contact with an electrolyte (the same as the one used in the forming phase of alumina) ensuring a continuous regeneration of the alumina layer;

– a second foil of aluminum with a thickness of about 30 μm constitutes the cathode;

– a blotting paper of a few tens of μm is inserted between the two previous foils, it serves as a reservoir to the electrolyte, which is in direct contact with the alumina layer deposited on the anode.

To increase the energy density, today's technologies use etched aluminum foils before undergoing anodic oxidation (Figure 5.12). Also, the loss factor of this type of capacitor depends on the purity of aluminum used: the weakest loss factor being obtained for the most pure aluminium foils.

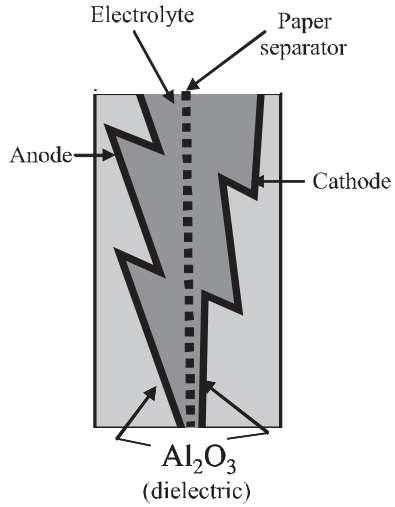

Figure 5.12. *Schematic showing the structure of an aluminum electrolytic capacitor*

The anode and cathode foils are connected to the terminals of the capacitor with strips introduced during the winding (Figure 5.13). To minimize series resistance

and inductance (ESR and ESL respectively) as much as possible, strips are inserted and combined all together to the terminals of the capacitor.

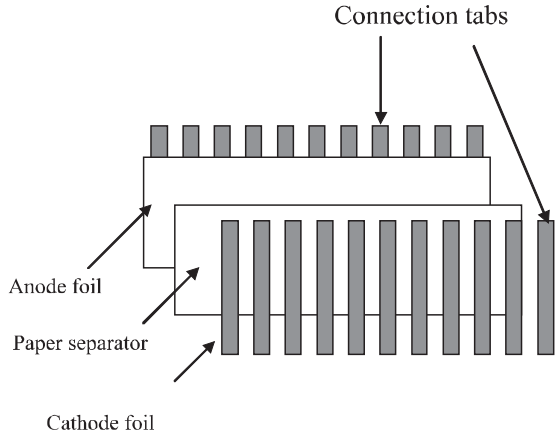

Figure 5.13. *Mode of connection to the terminals in the electrolytic capacitors*

A peculiarity of aluminum electrolytic capacitors is that they are polarized. Applying a reverse voltage between the anode and the cathode can generate gas inside the package whose pressure can lead to the explosion of the component if it is not equipped with a release valve.

5.7. Modeling and use of capacitors

The capacitors used in power electronics are subject to very severe stresses directly related to switching. They are flowed by currents that have on the one hand, very high rates of changes, sometimes exceeding 500 A/μs, and on the other hand, a very large harmonic content. In most of the power electronics systems, the switching frequency is larger than 20 kHz. Regarding low power systems, soft switching converters may operate at frequencies above 10 MHz (e.g., electronic ballast of discharge lamp). The use of capacitors in converters is mainly for input and output filtering of the DC or low frequencies voltages. They can also be found in resonant converters, quasi-resonant converters, multilevel converters, as well as in systems to help the commutation (snubbers with or without power dissipation).

5.7.1. *Limitations of capacitors*

Losses in capacitors are mainly due to stresses (voltage and temperature and flowing currents). In power electronics, all conditions are encountered together and make the capacitor a fragile component of the system.

The main limitation is the current which, on the one hand may lead to surges caused by inductive phenomena in the capacitor's internal connections, and on the other hand, due to its magnitude, can lead to electrodynamic efforts capable of destroying the capacitor.

The operating temperature also limits its performance. Indeed, the maximum operating temperature is relatively low ($\theta_{max} \leq 85°C$) and the ageing of a dielectric is temperature dependent. Losses in dielectric insulation, Joule losses in armatures, connections and in the case (eddy current) contribute to increase the loss of its performance.

Recent work has revealed the non-homogenous distribution of currents in capacitors according to their frequency. The knowledge of this phenomenon enables us to understand more precisely the "hotspots" of the capacitor flowed by high frequency currents and to determine its internal inductance. This can reduce, using appropriate internal connections, the internal inductance for a cylindrical geometry. We will now discuss the procedure to establish this type of model.

5.7.1.1. *Fine model*

Consider a cylindrical metallic film capacitor (Figure 5.14) wound on an insulating mandrel, where the coatings on the basis of the cylinder collect conduction current from the armatures. The geometry results in the symmetry of distribution of fields and currents in the capacitor. The conductors outside the winding are in fact arranged symmetrically in relation to the axis of symmetry of revolution of the capacitor.

The electrical and electromagnetic values are assumed to be sinusoidal. They will therefore be dependent on the pulse ω and the radius r of the capacitor. Let:

- $\underline{I}(r,\omega)$ be the current in the coating;
- $\underline{J}_{sc}(r,\omega)$ the surface density of current flowing in the coating;
- $\underline{B}(r,\omega)$ the magnetic induction.

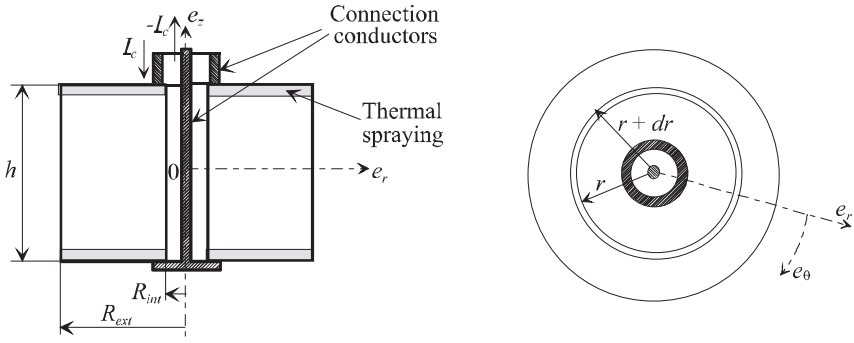

Figure 5.14. *Outline of capacitor*

The winding dimensions are as follows: R_{ext} external radius, R_{int} radius of the mandrel and h its height. The central connection imposes the following conditions on the current $\underline{I}(r,\omega)$ directed along the axis e_r running through the loop (C_1):

– on the external side of the coil $\underline{I}(R_{ext},\omega)=0$;

– on the external side of the mandrel $\underline{I}(R_{\text{int}},\omega)=\underline{I}_C$,

where $\underline{I}_C$ is the current supplying the power capacitor. The boundary conditions on the coating give a relationship between the orthoradial magnetic field $\underline{B}(r,\omega)$ in the winding and the current $\underline{I}(r,\omega)$:

$$\underline{B}(r,\omega)=-\frac{\mu_0}{2\pi r}\underline{I}(r,\omega)$$

If C is the total capacity of the capacitor, the surface capacity per area unit of the coating is $\gamma=\dfrac{C}{\pi(R_{ext}^2-R_{\text{int}}^2)}$. The conductance per area unit $\underline{Y}_s(\omega)$ is setting a series connection of a conductance $j\gamma\omega$ due to the capacitive effect and a conductance G_s associated with dielectric losses and Joule losses in metallization.

The surface admittance is expressed by the relationship:

$$\underline{Y}_s(\omega)=\frac{j\gamma\omega}{1+j\dfrac{\gamma}{G_s}\omega}$$

In addition, the alternating magnetic field $\underline{B}(r,\omega)$ will in turn create electromotive forces and thus disturb the distribution of the potential in the capacitor. In the plane (O, e_r, e_z) of the capacitor, the circulation of the electric field between two points, located at the same distance r from axis (O, e_z) and placed on a different coating, and the voltage drop resulting from the impedance of the coating $\underline{Z}_{sc}(r,\omega)dr$ between two circular crowns of radius r and $r + dr$ (Figure 5.14) is equal to the temporal variation of magnetic flux created by $\underline{B}(r,\omega)$ on the surface limited by the contour ***abcda*** (Figure 5.15). The abovementioned Faraday law is written:

$$-\underline{\xi}(r+dr,\omega)+\underline{\xi}(r,\omega)-2\underline{Z}_{sc}(r,\omega)\underline{I}(r,\omega)dr=-j\omega h\underline{B}(r,\omega)dr$$

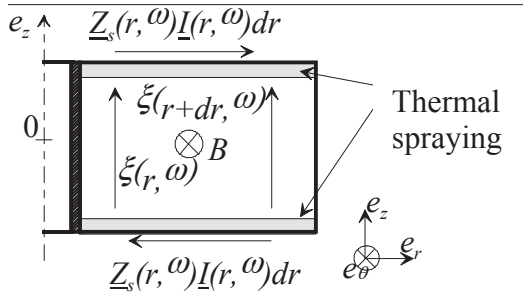

Figure 5.15. *Circulation of the electric field in a loop*

When dr tends to zero, the equation becomes:

$$\frac{f\underline{\xi}(r,\omega)}{fr}=-2\underline{Z}_{sc}(r,\omega)\underline{I}(r,\omega)+j\omega\underline{B}(r,\omega)$$

with $\underline{Z}_{sc}(r,\omega)dr=\frac{\underline{Z}_{sc}}{2\pi r}dr$ elementary impedance between crowns depending on the surface impedance of coating which itself may be written in the form $\underline{Z}_{sc}=\frac{(1+j)\rho_{sc}}{\delta_{sc}}$ with $\delta_{sc}=\sqrt{\frac{2\rho_{sc}}{\mu_{sc}\omega}}$ where μ_{sc} is the magnetic permeability of coating and ρ_{sc} its resistivity.

In the case of a zinc coating, then: $\mu_{sc}=\mu_0=4\pi\ 10^{-7}$ H/m and $\rho_{sc}=5.8\cdot10^{-8}\ \Omega$m.

The distribution of potential between the two coatings is associated with the current surface density running through the capacitor, so:

$$\underline{J}_s(r,\omega)=\underline{Y}_s(\omega)\underline{E}(r,\omega)$$

The surface current density $\underline{J}_s(r,\omega)$ is also associated with the current $\underline{I}(r,\omega)$ by the relationship:

$$\frac{\partial \underline{I}(r,\omega)}{\partial r} = -2\pi \underline{J}_s(r,\omega)$$

Combining equations, we obtain:

$$r^2 \frac{\partial^2 \underline{B}(r,\omega)}{\partial r^2} + r\frac{\partial \underline{B}(r,\omega)}{\partial r} + \left[\frac{r^2}{\delta_c{}^2} - 1\right]\underline{B}(r,\omega) = 0$$

with δ_c equivalent to a skin thickness in the capacitor:

$$\delta_c = \left[\frac{-1}{\underline{Y}_s(\omega)[2\underline{Z}_{sc} + j\omega h\mu_0]}\right]^{\frac{1}{2}}$$

To solve this equation, we note J_n and Y_n as the Bessel functions of order n, respectively of the first and second species. Taking into account the boundary conditions, the solutions of the equation are written for a return to the center:

$$B(r,\omega) = \frac{\mu_0 \underline{I}_c}{2\pi R_{\text{int}}\Delta}\left[Y_1\left(\frac{R_{ext}}{\delta_c}\right)J_1\left(\frac{r}{\delta_c}\right) - J_1\left(\frac{R_{ext}}{\delta_c}\right)Y_1\left(\frac{r}{\delta_c}\right)\right]$$

with $\Delta = Y_1\left(\frac{R_{\text{int}}}{\delta_c}\right)J_1\left(\frac{R_{ext}}{\delta_c}\right) - J_1\left(\frac{R_{\text{int}}}{\delta_c}\right)Y_1\left(\frac{R_{ext}}{\delta_c}\right)$

On the other hand, we can determine the current density in the capacitor:

$$\underline{J}_s(r,\omega) = \frac{\underline{I}_c}{2\pi R_{\text{int}}\delta_c\Delta}\left[Y_1\left(\frac{R_{ext}}{\delta_c}\right)J_0\left(\frac{r}{\delta_c}\right) - J_1\left(\frac{R_{ext}}{\delta_c}\right)Y_0\left(\frac{r}{\delta_c}\right)\right]$$

The equation shows that the current density depends in part on the ratio between the outside radius of the capacitor and of the "pseudo-skin thickness δ_c". The total impedance of the capacitor is derived from the expression of the distribution of the current density in the capacitor, where l_s and r_s represent the inductance and the resistance of the external connections of the capacitor. The total impedance is then written as:

$$\underline{Z}_{tot} = \frac{\underline{J}_s(R_{int},\omega)}{\underline{Y}_s(\omega)\underline{I}_c} + jl_s\omega + r_s$$

5.7.1.2. *Impedance of the wound capacitor*

The representation of the impedance of a capacitor as a function of the frequency is given in Figure 5.16. As in the classic model, the impedance decreases with a slope of -20 dB per decade up to its resonance frequency. However, beyond this frequency, the impedance increases with a slope close to 20 dB per decade. From this example around 1.6 MHz, there is a fairly clear variation of the module of the impedance and of its phase. This variation, which is repeated to a lesser degree at 3 MHz, corresponds to a minimum of the expression Δ given in 15 and hence to a maximum of the current density $\underline{J}_s(R_{int},\omega)$.

These increases reflect, in the winding, changes of phase of $\underline{J}_s(R_{int},\omega)$ which reflect the existence of loop currents as shown in Figure 5.17. Thus, capacitors wrapped in metal films behave in a similar manner to the anti-resonant circuits or microwave cavities.

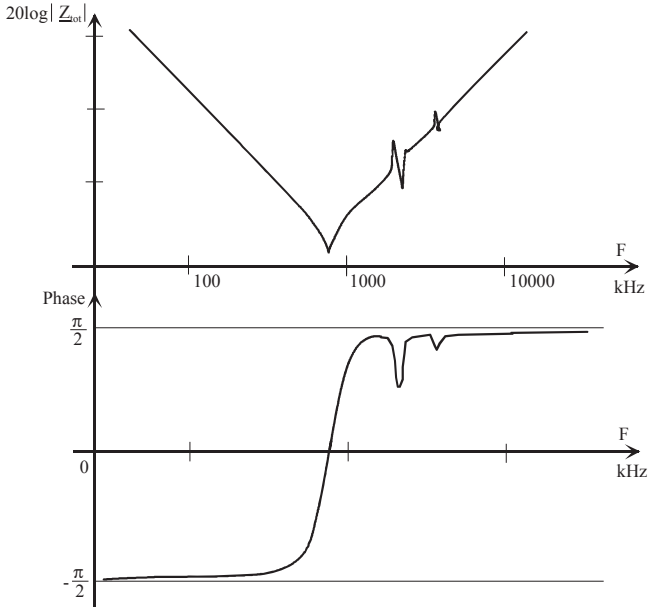

Figure 5.16. *Impedance of the capacitor*

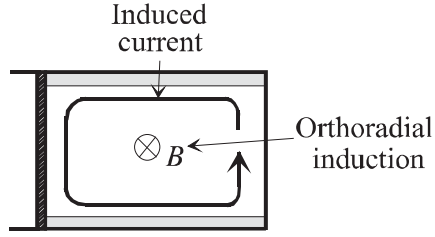

Figure 5.17. *Currents induced in the winding*

5.7.1.3. *Distribution of current density in the winding*

It is possible to reveal the distribution of current density in the capacitor depending on the distance r from the center for different frequencies (Figure 5.18). For low frequencies, the current density is homogenous in the capacitor; beyond its resonance frequency, it becomes larger inside (close to the mandrel) and outside of the winding, involving very significant local heating.

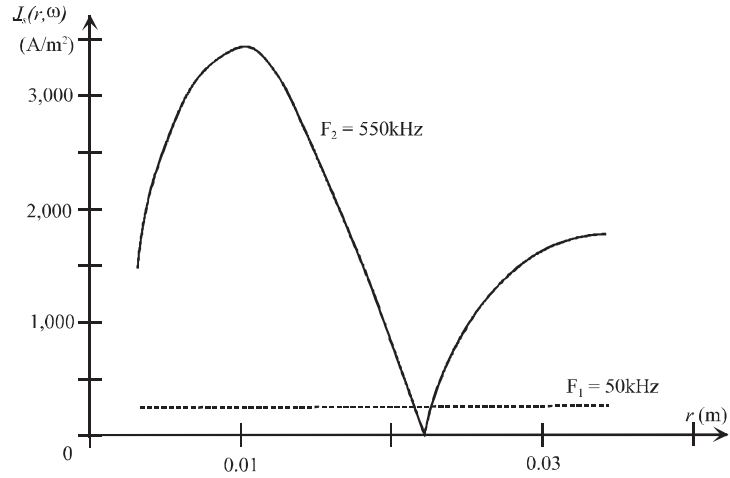

Figure 5.18. *Distribution of current density depending on the distance to the axis of symmetry of winding for two frequencies*

The use of capacitors with symmetric connections, while desirable to minimize self inductances and radiated fields, is not always possible because of the manufacturing technologies used. There are often, in power electronics designs, wound capacitors with structures as shown in Figure 5.19 (return conductors being simple wires made of insulated copper). To take these asymmetries into account, the former model must be changed. Thus, a misalignment of 3 mm of the return conductor leads the current density flowing through the winding (in an amount not exceeding the wire) in the vicinity of the return wire to be multiplied by a factor of 300 for a capacitor of 72 mm diameter.

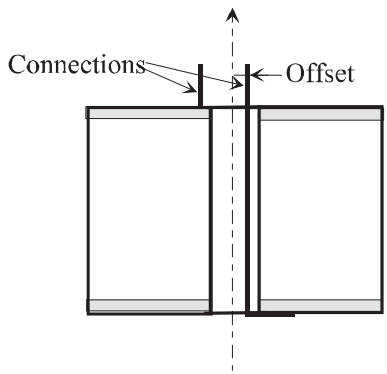

Figure 5.19. *Capacitor with non-symmetric return*

5.7.1.4. *Self-inductance of capacitor*

The behavior described by the impedance equation can show the resonant frequency of the capacitor for a return conductor in the center. It is easy to obtain, for a same type of capacitor (same geometry and same physical characteristics), its impedance with an external return. To do this, new connection conditions must be imposed: $\underline{I}(r=R_{int},\omega)=0$ and $\underline{I}(r=R_{ext},\omega)=-\underline{I}_c$. The model shows that an external return is preferable to a central return: the resonance frequency is twice as high for an external return as for a return to the center, implying that the self inductance in the first case is 1.414 ($\sqrt{2}$) times lower.

Starting from this model, it is also possible to seek a capacitor, which will minimize inductance, changing its geometric parameters (h, R_{int} and R_{ext}). Two types of simple geometries are eligible for this result: *flat capacitors* (diameter of winding > length of winding) and *annular capacitors* (large R_{ext} and R_{int}).

5.7.2. *Application of capacitors*

Power electronics systems require capacitors for:

– filtering stages or decoupling;

– resonant circuits (resonant load, quasi-resonant converters, storage of electrostatic energy, etc.);

– snubber circuits.

For each domain, some background on the characteristic wave shapes of currents that can flow in the capacitors are given.

5.7.2.1. *Filtering capacitors (or decoupling)*

The filtering capacitors are designed to minimize the voltage ripples. They operate under almost quasi-continuous voltage.

At the converter input, in most cases (choppers, switching power supplies, inverters, PWM rectifiers with zero voltage switching, active filters, etc.), they can filter the power network, rectified or not. In the first case, their value is very large considering the low frequency of the network. Simultaneously, they also serve as bypass for commutation cells, in order to recreate at their terminals a voltage source as ideal as possible to limit the voltage surges due to the switching. Electrolytic

capacitors are mainly used here and capacitor films to a lesser extent. Sometimes, whatever the technology (same or mixed), they are placed in parallel to reduce the internal stray inductances.

At the output, only a filtering function is needed, according to the quality required. Depending on the nature of the voltage (DC or AC), either continuously or alternative, electrochemical capacitors or capacitor films are used.

According to the preceding section on the limitations of capacitors, it may be demonstrated that, by an appropriate internal connection, it is possible, from a wound capacitor, to make an almost perfect decoupling. This capacitor is called a "quadripolar capacitor".

5.7.2.2. *The quadripolar capacitor*

On a metallized film capacitor wound around a core, cylindrical revolution connections, with simultaneous returns to the center and to the periphery, are carried out as presented in Figure 5.20. This component becomes quadripolar including two accesses, AD and EH. The currents flowing in the capacitor coil do not distribute homogenously as their frequency increases. In particular, HF currents propogate toward the center of the coil (CC' area) for a connection ABFD and to its periphery (DD' area) for a connection EBFH, which contributes to an almost perfect HF decoupling between the two circuits.

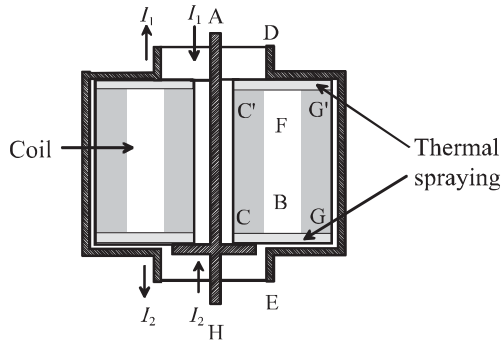

Figure 5.20. *Structure of the quadripolar capacitor*

The physical model of this quadripolar capacitor is shown in Figure 5.21. The quantities r_s and l_s represent the resistors and inductors of external connections, M_{12} the residual mutual inductance between the two connected circuits and $V_{CC'}$ and $V_{GG'}$ the sources of potential differences between points C and C' on the one

hand and G and G' on the other. These are functions of the distribution of current density $\underline{J}_s(r,\omega)$ in the capacitor and surface conductance of winding films $\underline{Y}_s(\omega)$.

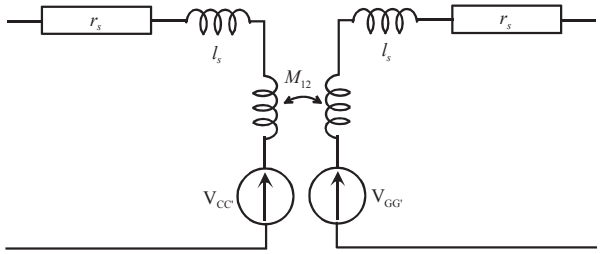

Figure 5.21. *Physical model*

The characterization of decoupling capacitors is described by its "insertion loss" (rated *PI*) depending on the frequency. This quantity is defined as follows: $PI(dB) = 20\log\frac{V_1}{V_m}$ with V_1 the voltage on a 50 Ω load without the capacitor and V_m the voltage on the same charge connected with the capacitor (Figure 5.22).

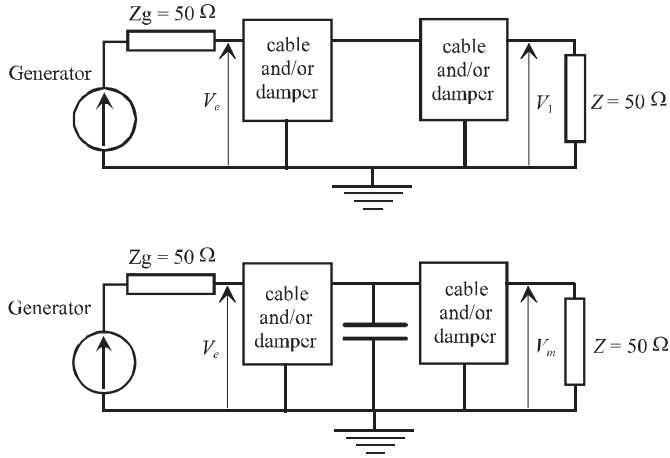

Figure 5.22. *Measurement of insertion losses*

In Figure 5.23, the comparison between the *PI* of a quadripolar capacitor and those of a classical dipolar capacitor shows that at high frequency the first one keeps its capacitive characteristics. This type of capacitor could be used to greatly reduce differential mode electromagnetic disturbances.

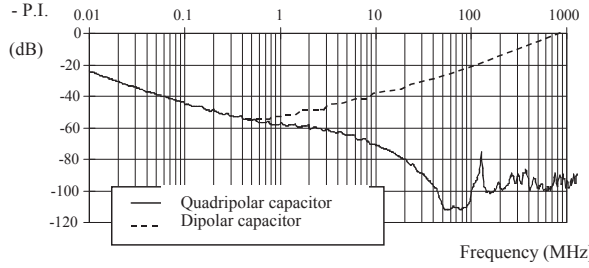

Figure 5.23. *Insertion losses of 10 μF capacitors*

5.7.2.3. *Resonant capacitors*

Capacitors used in resonant converters, quasi-resonant converters or structures where the capacitive element is directly involved in the conversion, are subject to very important current intensities at high frequencies. The shapes of waveforms applied are almost AC and DC voltages and alternative voltages. In these cases, the dielectric losses and the temperature increases are large. Their ability to endure heat must be a choice criterion.

5.7.2.4. *Switching capacitors*

The capacitors used for snubbers are subject to large current pulses during switching. Here, the value of internal inductance is a key parameter and must be as low as possible. The connections must be made very carefully. As the switching cell is a source of large electromagnetic fields, the capacitor must be shielded if its electromagnetic susceptibility is low.

5.8. Ceramic capacitors

The current interest for ceramic materials is mainly associated, on one hand, with the possibilities of sustaining high permittivity values and, on the other hand, thanks to the development of technological processes to decrease the size of these components hence favoring their integration in power electronics systems. In the

following, we will draw a quick overview of the properties of these materials to enable the engineer to choose the appropriate component on a rational basis. In a first step we describe the main characteristics of these materials. Then, their methods of manufacture (from material to component) are presented. Finally the main types of capacitors currently available on the market and some of their possible applications in power electronics systems are given.

5.8.1. *Definitions*

5.8.1.1. *Ceramic materials*

The word ceramic comes from the Greek word "keramos", which means "potter" or "potter's clay". It comes from the ancient Sanskrit root "burn". The definition given generally for a ceramic is "product obtained by action of fire on a material derived from the earth". These are inorganic materials contrary to polymers (based on carbon chemistry).

5.8.1.2. *Nature of chemical bonds*

From a physical point of view, ceramics are made of crystals, inside which – in the first approximation – the individual atoms are bonded by ionic type connections. The nature of atomic bonds is therefore also different from that between atoms in a polymer which is a type of low-valence (dipole, or hydrogen or van der Waals type).

The ionic bond presents a spherical symmetry leading to a non-directionality of the valence; their binding energy is thus very high (about 750 kJ/mol (compared to the tens of kJ/mol for polymers)), giving them unique properties: a high hardness, a high melting point, a low electrical conductivity and high permittivity. This last property is of particularly interest here.

5.8.1.3. *Dielectric properties*

In crystals, and contrary to polymers, electric dipole moments are usually tightened. The dipoles are part of the crystalline structure: they are the structure. The electric field polarizes these materials by inducing dipole moments. The charges' displacement from their position of equilibrium changes the solid dimensions. The properties of these materials may no longer be described by vector quantities but rather by tensors. Relations between the electrical parameters (Polarization, P, Displacement, D, etc.) are generally linear (but may not be: see the type II components (section 5.8)) but involve the three space components of the electric field E.

5.8.1.4. *Piezoelectricity and ferroelectricity*

The consequence of the previous assertion is that the physical properties of the crystals are related to their crystalline structure. Of the 32 existing symmetries, 20 of them are piezoelectric. When these materials are compressed, they develop a potential difference and, conversely, if an electrical voltage is applied, a mechanical deformation appears. Among these 20 classes, 10 of them are polar, i.e. they have an electrical polarization even in the absence of an applied external electric field. Their dipole moment is spontaneous and generally small and fixed.

A certain category of polar crystals are called ferroelectrics: here the polar axis, support of a permanent dipole, is mobile in the crystal lattice under the influence of an external electric field high enough. The ferroelectric materials have a polarization Po in the absence of field. The high dielectric constant of these materials allows us to produce capacitors with a high capacity per volume unit, thereby reducing their size.

5.8.1.5. *Temperature coefficient of a component*

Some physical properties are intrinsic to this type of material (or components). The main property is the temperature coefficient of the capacitor (CTC). This is defined by:

$$CTC = \frac{1}{C}\frac{dC}{dT}$$

with C the capacity and T the temperature.

This coefficient must be as low as possible except when a temperature drift of the circuit in which these components are placed has to be compensated. CTC may then be negative, positive or zero (the literature talks about NPO components).

CTC can also be written according to the intrinsic properties of materials and becomes in this case the temperature coefficient of permittivity, $CT\varepsilon$ such that:

$$CT\varepsilon = \frac{1}{\varepsilon}\frac{d\varepsilon}{dT} + \lambda$$

with ε the permittivity and λ the thickness changes of the material with temperature.

When the material is not isotropic, or when it is very sensitive to temperature, these two factors (CTC and $CT\varepsilon$) are very different. In ceramics, anisotropic

materials by definition, these two factors are different. Changes in the capacity with temperature are due to:

– the existence of impurities;
– changes in the dimension of the structure;
– changes in polarizability (due to the change of structure).

5.8.2. *Methods of producing ceramics*

The process of manufacture of ceramics, like the ones used in power electronics, requires a large number of steps. They are summarized in Figure 5.24.

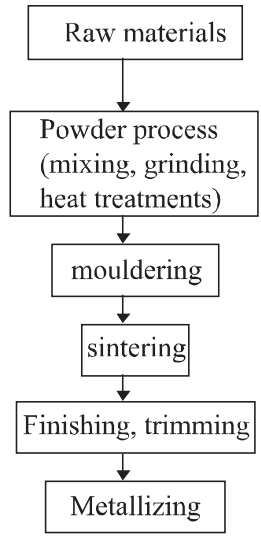

Figure 5.24. *Steps for manufacturing of ceramics*

5.8.2.1. *Powder process*

The manufacturing technology is used to obtain a material with specific properties of perfectly controlled dimensions and of course at the lowest cost. The material properties are mainly affected by the chemical composition, but also by the size and distribution of powders, porosity, uniformity, etc., which depend greatly on the synthesis method.

Two distinct processes may be used for the preparation of powders, the chemical method and the traditional solid/solid method.

5.8.2.1.1. The solid/solid method

This is a mix of powdered raw materials of simple oxides (transition metals or others) in proportions calculated to achieve the desired composition. The mixture can be made dry or wet: the slurry. The slurry is shaken to homogenize the mixture which, after drying, is calcinated. The mechanical grinding treatment can reduce the particle size, increase the specific surface and increase the reactiveness of the powder during the sintering. To obtain the appropriate result, it is often necessary to carry out several runs of grinding-calcination.

5.8.2.1.2. The chemical method

This technique aims to develop powders of mixed oxides, in the adequate proportions, directly from "precursor" powders (carbonates, oxalates, formiates, etc.). The steps are as follows:

– precipitation in solution of the "mixed" precursor corresponding to the composition desired;

– thermal decomposition of the original salt and transformation into an oxide.

This method of preparation at room temperature allow to control the shape, size and distribution of the powders and thereby improve the densification, reproducibility and stability of the properties and among them the electrical properties of the ceramics. This prevents many grinding and burning operations.

5.8.2.2. *Shaping*

It is during this operation that "raw" ceramics are produced, which can be broadly described as a stacking of grains mechanically linked by an organic binder. The powder must first undergo a granulation which increases the fluidness. This operation consists of incorporating an organic link in the oxide powder to give it plasticity and to ensure a sufficient cohesion of the raw ceramic. The choice of shaping crucially depends on the geometric structure of the component to be produced. In the case of "bulk ceramics", the set (oxide powder + binder) is pressed. For manufacturing multilayer ceramics, a "tapecasting" process is used. This shaping is industrially used for the manufacture of components from thin strips (a few mm). This operation consists of the suspension of a dry powder in an aqueous or organic media. The stability of this suspension is provided by the addition of a

scattering agent. The production and handling of thin strips of large surface requires the introduction into the slurry of organic binders and plasticizers. These products give to the dry band the mechanical rigidity and flexibility necessary for its handling. The mixing and homogenization of the slurry are generally carried out mechanically using ball mixers (zirconia) and the viscosity is adjusted by adding a solvent. The slurry, under magnetic stirring, is then introduced into a casting mould with a pump.

Different techniques are used, depending on the thickness:

– casting by extraction (combined effect of the viscosity and gravity) for strip thickness ranging from 15 to 50 μm;

– casting by rolling (blade method) for thicknesses ranging from 50 μm to several mm.

Other parameters affect the thickness of the slurry, particularly the viscosity, the inclination of the casting tank and the surface tension of the slurry.

After drying and evaporation of the solvents, the ceramic tape is cut and then stacked. The plate is then thermo compressed. Finally, a heat treatment (a burning) is performed on ceramic plates to remove the organic substances before sintering.

5.8.2.3. *Sintering*

This heat treatment allows a system of individual particles or a porous body to move towards a state of maximum compactness (zero porosity). The material is heated below its melting temperature, leading to both a mechanical consolidation and to an increased density. The sintering is described as a succession of steps:

– slight withdrawal or slight swelling after the removal of the binder;

– internal reorganization of grains by creating bridges at the contact joints;

– start of junction part between the grains by creating bridges at the contact points;

– formation of a strong skeleton;

– elimination of open porosity between grains;

– elimination of closed porosities.

These phenomena are the result of various transport mechanisms (surface diffusion, at the grain boundaries and in the volume, phenomenon of evaporation, dissolution/crystallization, material transport to intergranular areas). A powder must have specific characteristics in order to optimize the sintering process such as high

chemical purity, a tight distribution size, an isotropic *habitus*, small size and monodisperse particles.

The sintering cycle (rate of temperature change during heating and cooling, temperature and dwell-time duration nature of the atmosphere) must be adapted to each type of material.

5.8.2.4. *Metallization*

The electrical contacts are usually made of precious metals (Ag, Pd, Pt). The filing of electrodes may be produced by different methods (spraying, screen printing rolling or immersion in silver (*dipping*)). After removing the binders and solvents, the silver-based mixing diffuses superficially in the ceramics during a heat treatment carried out at a temperature between 500°C and 900°C, depending on the type of silver used. The firing cycle depends on the morphology of the particles of silver, the particle size, the surface of the ceramic, but also of the wettability and of the melting temperature.

5.8.3. *Technologies of ceramic capacitors*

In a uniform and homogenous field, the value of capacity, C, is given by:

$$C = \frac{\varepsilon_0 \varepsilon_r S}{e}$$

with ε_0, ε_r the permittivities of vacuum and of the ceramic material respectively, S the surface of electrodes and e dielectric thickness. An Increase of the capacity may therefore be obtained, from a geometric point of view by an increase of the specific surface of the electrodes and/or a low thickness and/or from a material point of view by using a high permittivity material.

Therefore several structures of ceramic capacitors exist, which are based on different parameters such as the final value of capacity, the dielectric strength and the degree of miniaturization.

5.8.3.1. *Structures of ceramic capacitors*

Two main structures are available.

5.8.3.1.1. Disk

This is the simplest structure. A single ceramic whose thickness can reach several hundreds of microns is achieved in the form of a disk. The electrodes are usually made of silver.

5.8.3.1.2. Multilayers

This structure applies to the different types of materials used. The goal is to artificially increase the surface with successive layers of metal and dielectric, leading us to consider that elemetary capacitors are in parallel (Figure 5.25).

The thickness and number of dielectric layers vary, depending on the value of the capacity and from one manufacturer to another. Capacity values between 1 pF and 1 μF are likely to be reached.

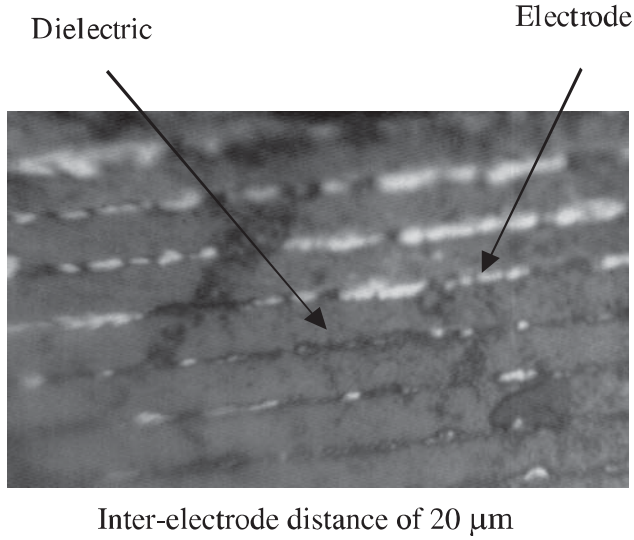

Figure 5.25. *SEM picture of a multilayer structure*

The external contacts are made of metal endings that are welded on to connections. The component is then encapsulated in a resin. It finally leads to a component whose volume is several mm^3. The capacity per volume unit of such components is very large.

5.8.3.2. *Electrodes*

5.8.3.2.1. Nature

Electrodes are one of the key issues in the manufacture of ceramic capacitors. The metals used are generally precious metals (Ag, Pd, Pt, etc.), or indium, gallium, and/or their eutectic and/or their alloys.

These electrodes are connected at their ends by two endings, which may be of two types. These endings are Ag/Pd (which is an expensive option) or nickel/tin (Ni/Sn). These endings are diffusion barriers to limit the spread of lead solder in the dielectric, which would result in the deterioration of the component properties (Figure 5.26).

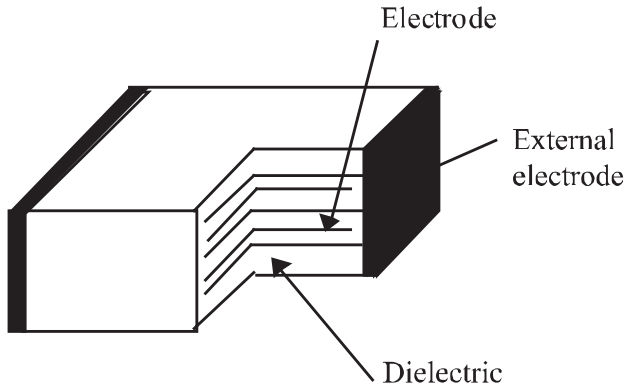

Figure 5.26. *Scheme of a multilayer capacitor*

5.8.3.2.2. Electrical properties of electrodes

The resistivity of metals and the thickness of electrodes may have very significant drawbacks. Hence the high frequency losses are mainly associated with the series resistance of the capacitors, which itself depends on the resistance of electrodes. This resistance is often increased by skin effect. For the frequencies where this effect is negligible, and for the multilayer structure presented, the share of losses attributable to the electrodes is:

$$2\pi\nu R_s C \approx 4\pi\nu\left(\frac{\rho_e}{e_e}\right)\left(\frac{a}{b}\right)$$

with: a, the length over which the electrodes are superimposed, b, the width of the electrodes, and e_e, ρ_e, respectively their thickness and resistivity.

This approximation leads to dielectric losses at 1 MHz of about $2\ 10^{-2}$ for a capacity of 50 nF with Pd electrodes ($\rho e = 10^{-7}\ \Omega\cdot m$) of 3 μm thickness .

For higher frequency applications (> 100 MHz), losses are controlled by the skin effect and the metal that is used for the electrodes must be less resistive.

Finally, note that the metal/dielectric contact must be as close as possible to avoid the formation of an interface leading to the existence of a stray capacitance whose role will be even more damaging the higher the value of the ceramic permittivity. As an example, if the ratio of permittivities between the metal oxide layer and the dielectric material is about 1,000, the ratio of thicknesses in the case of a multilayer structure must be at least 10^{-5} to be considered as negligible. A thickness of 25 μm for the dielectric material therefore lead to layers whose dimensions must be less than the nm to be regarded as negligible. This simple example illustrates the importance of careful manufacturing of this type of structure.

5.8.4. *The different types of components*

5.8.4.1. *Definitions*

The distinction and definitions given below are nothing but subjective. However, it is usual to find them. There are three types of ceramic capacitors, which differ in their electrical properties.

5.8.4.1.1. Type I components

Their capacitance ranges from 1 pF to 1 μF. They have low dielectric constants (6-500) that almost never vary, especially versus temperature. More exactly, their temperature coefficient can be positive, negative or zero, but must have a low value. These capacitors also have a constant permittivity versus both the voltage and the frequency. They are mainly used in the high frequency range. Their dielectric losses are very low ($tg\delta < 0.01$).

5.8.4.1.2. Type II components

The capacitance of these components ranges typically from 2.5 pF to 0.4 μF. The dielectrics are generally ferroelectric ceramics like barium titanate. Many doping materials may be introduced to ensure a nearly constant value of the capacitance

versus the temperature and to obtain a high permittivity (a few thousand). However, this value is changing with many parameters such as the applied voltage, temperature and frequency, etc.

5.8.4.1.3. Type III components

The range of capacities of this type of ceramics is from 33 nF to 1 μF. The large permittivities (of the order of hundreds of thousands) are due to the grain/grain boundary structure of these ceramics. Their use is in applications requiring low losses, high insulation resistance but which do not demand a stability of the capacitance value with the voltage, the frequency or the temperature. Finally, their breakdown voltage (due to their "real" thicknesses) is relatively low, in fact preventing their use for "high voltage" power electronics.

5.8.4.2. *Capacitors of type I: materials and applications*

Ceramics with permittivity less than 10 such as porcelain (zirconia or steatite), refractory based-cordierite, aluminum silicate, aluminum nitride, are mostly used in insulation functions. They are used in so called DCB (direct copper bonding) substrates, high voltage insulators, spark plugs, etc. As capacitors, their applications are in the field of high frequencies (up to and beyond GHz). Their properties must be particularly controlled: low dielectric losses, constant ε with temperature and frequency, etc. For permittivities above 10, the main applications of these materials are capacitors used in electronic circuits and known as NPZ (negative, positive or zero variation of their CTC). In addition to appropriate temperature dependence, they have low losses.

The materials used are:

– Glass: (silicate, with lead, borosilicate, alumino-silicate, etc.) with various percentages of Si, Na, K, Ca, Mg, Al, etc., conferring dielectric permittivity between 3.8 and 15 and CTC between 40 and 600×10^{-6} /K. The interest of this type of capacitor is, on the one hand, its low dissipation factor (10^{-4}), low dependence of its properties with frequency and, on the other hand, to its insensitivity to temperature and humidity.

– Ceramic-based glass: they involve a glassy part and a crystalline part. Heat treatment gives them their structural properties. Since the crystalline part has permittivities larger than glass, it is necessary to control its dimensions. The latter sets the final value of the permittivity and, consequently, the capacity per volume unit of the component. It has to be remembered that it is possible to obtain multilayer capacitors based on tapes of lead glass, barium, strontium, nobiate, etc., whose properties will mainly depend on the grain size. Their permittivities vary between 200 and 1,200 at room temperature and can be very stable in both

temperature and frequency. For the lowest grain sizes the thickness of these layers may vary between 20 and 200 μm.

– Porcelains: This term is used to describe a dielectric made from a mixture of glass and one or more crystalline phases but which does not use manufacturing techniques specific to ceramics. The best known are lead silicates. The layers used are in the order of 200 μm, their permittivity is about 15 with a good temperature stability and high resistivity (> 10^{14} Ω·cm).

– Mica is a mineral with splits whose thicknesses range from 50 μm and more. The ruby shape ($kAl^2(Si^3Al)O^{10}(OH)^2$) is the most widely type of mica used in electronics. Its permittivity varies between 5 and 9 and has a good temperature stability (10^{-5} to 10^{-4} /K) and a dissipation factor of a few percent. This material, because of its structure, is sensitive to pressure. Particular attention must be given, during coating or encapsulation, not to exert too much pressure, the changes of capacity with pressure being around $4x10^{-10}$ /Pa. Finally, being in the form of strata, mica is sensitive to moisture (which will have a tendency to bind interfaces). The components are of the multilayers type and connections are made by clamping.

5.8.4.3. *Capacitors of type II: materials and applications*

The components of type II are mainly based on ferroelectric materials, many of which have a perovskite structure type (ABO^3) or an ilmenite type of structure. In the first step, the definitions needed to understand this family of materials are reminded. Few examples are given and their behaviors are depicted. Their main properties are defined. These components are the most commonly used in power electronics because of their large capacity per volume unit, their non-linear behaviors with both the voltage and the temperature.

5.8.4.3.1. Definitions

As already reported (section 5.8.1.4), a ferroelectric material has a polarization Po even in the absence of electric field. In addition, the polarization P according to the applied electric field is neither linear nor reversible: the hysteresis loop. Figure 5.27 allows the definition of key values that are useful:

– Ps: spontaneous polarization, corresponding to the saturation value;

– Pr: remnant polarization, which is the value for a zero field;

– Ec: coercive field, corresponding to the field necessary to cancel the polarization.

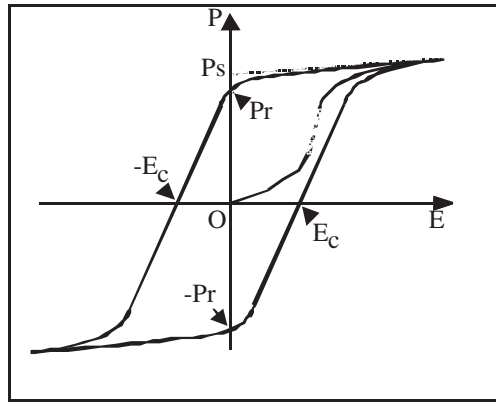

Figure 5.27. *Example of hysteresis cycle obtained in a ferroelectric material*

However, the ceramics used are not mono crystalline materials. As a consequence, the cycle shape is changed (Figure 5.28b).

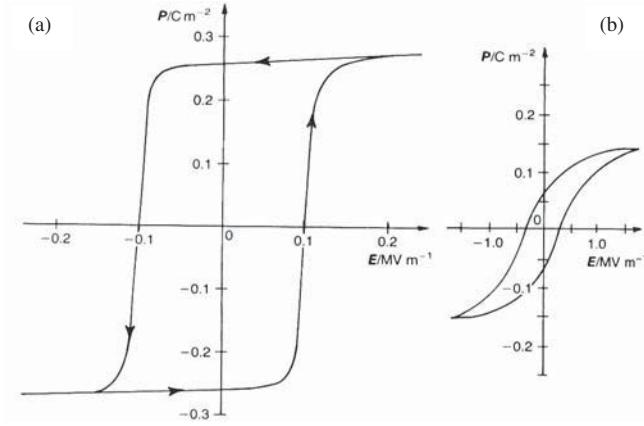

Figure 5.28. *Hysteresis cycle and orders of magnitude of major quantities in a sample of monocrystalline $BaTiO_3$ (a) and in a ceramic (b)*

If the material is heated beyond the so-called Curie temperature, the relationship P(E) becomes linear and the material becomes apolar: it is in its paraelectric state. Figures 5.29 and 5.30 respectively illustrate these behaviors in a crystal of barium titanate and in a commercial capacitor.

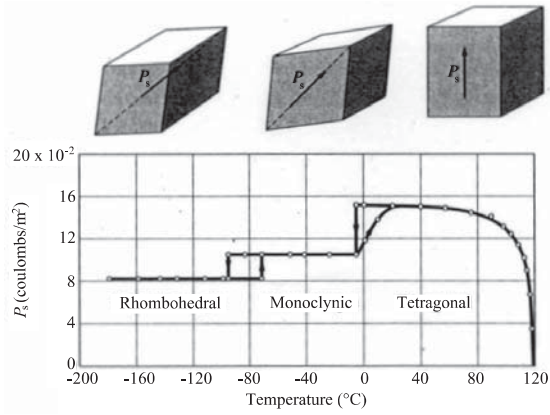

Figure 5.29 *Evolution of the permittivity in a monocrystalline $BaTiO_3$, as a function of temperature, along one of its axes*

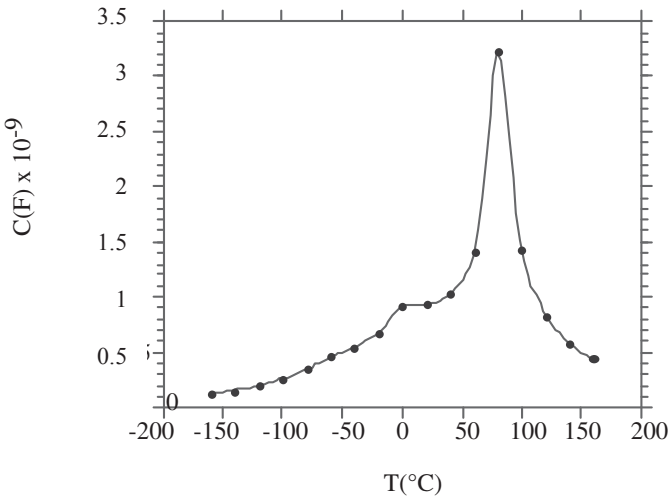

Figure 5.30. *Evolution of the capacity of a $BaTiO_3$ ceramic according to temperature*

5.8.4.3.2. Capacitors available on the market

These components are classified according to their properties by various standards such as EIA (*Electronic Industries Association*) and IEC (*International Electrotechnical Commission*). A code is allocated to them, such as Z5U for the EIA standard or 2F4 for the IEC standard. It allows us to specify the temperature range and changes in the capacitance of a capacitor over a given temperature range. This

variation is expressed as a percentage of the value of the capacity measured at 25°C under a zero polarization field. Table 5.1 shows, for the EIA standard, the different codes.

EIA Code	Temperature Range (°C)	EIA Code	ΔC/C (%)
X7	–55 to +125	D	± 3.3
X5	–55 to +85	E	± 4.7
Y5	–30 to +85	F	± 7.5
Z5	+10 to +85	P	± 10
		R	± 15
		S	± 22
		T	+22 to –33
		U	+22 to –56
		V	+22 to –82

Table 5.1. *Codes according* to *EIA standard*

Generally, these standards are difficult to meet and the manufacturers prefer to give, in addition to a code, the electrical characteristics of their own components. Table 5.2 shows an example of electrical data supplied by manufacturers and where you can see the gap between the codes and the electrical characteristics may be seen.

Finally, nominal operation voltage of these components is given for a few tens of volts. In fact, their non-linear behavior with voltage (Figure 5.31), representing a disadvantage, generally prevents the manufacturer to ensure a stable capacity for use at higher voltage.

Type	Unom (V)	Variation (ΔC/C) (%)	Temperature Range (°C)
Z5U MB	50	± 20	+10 to +85
X7R MB	50	± 10	–55 to +125
Y5V MB	50	± 20	–30 to +85
BX	50	± 20	–55 to +125
2F4	100	–20 to +80	–25 to +85
Y5V MM	50	–30 to +80	–25 to +85

Table 5.2. *Manufacturer data for samples*

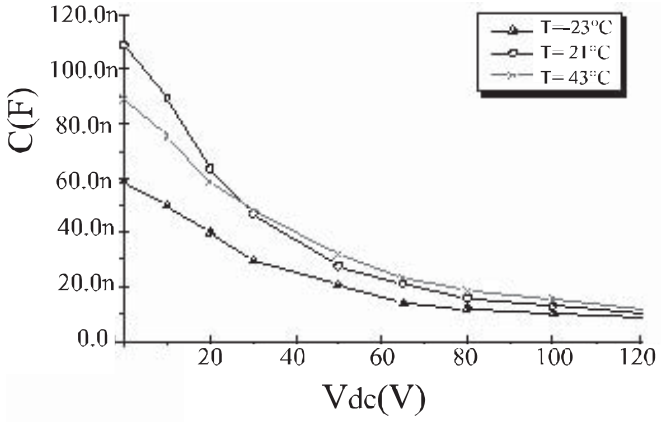

Figure 5.31. *Evolution of capacitance value with the voltage in a Z5U capacitor*

However, their use is possible for larger voltages (up to 10 times the rated voltage specified by the manufacturer). Also rarely reported is the variation of properties according to frequency (Figure 5.32).

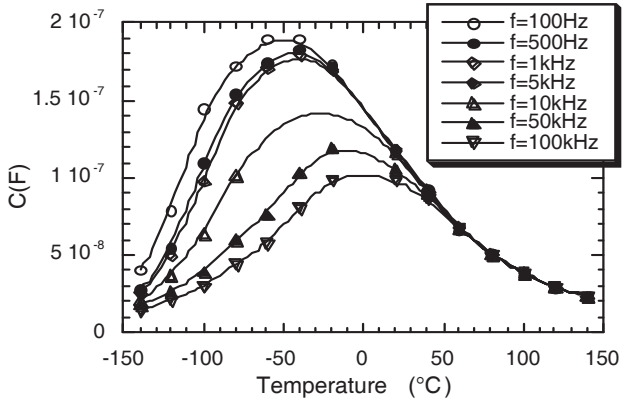

Figure 5.32. *Variation of capacity according to temperature and frequency*

Knowledge of these properties is generally sufficient to design the capacitor in its application.

5.8.4.4. *Type III capacitors: materials and applications*

Under certain conditons, preparations with barium titanate or strontium may exhibit permittivities higher than 100,000, but with high losses and low resistivities, which decrease with the voltage. Mastering the manufacturing process, coupled with an understanding of physical phenomena involved, lead us to obtain in a reproducible way this type of material, with, however, higher values of resistivities compatible with electronics applications. In order to understand their operation, the easiest way is to consider thin dielectric films with a large surface, obtained through the oxidation of the grains of barium titanates or strontium which were previously made conductive by adding appropriate doping (La3+, Ba2+, etc.). However, these structures do not behave at all like a resistor in series with a very high capacitance value. Indeed, these structures have very non-linear behavior of their current - voltage characteristics, which can be explained by the existence of a semi-conductive layer barrier. This behavior is related to the nonlinear resistivity of the grains with the applied voltage, which affects the amount of charge stored at the interfaces and therefore the capacity.

The most commonly encountered materials in the synthesis of such components are:

– for the ceramic phase: barium titanate or strontium;

– for the materials conferring conductivity to the grain: yttrium, lanthanum, niobium, antimony, etc.;

– for the additives: silica, alumina, etc.;

– for the electrodes: silver, indium/gallium, nickel/chrome, all chosen to avoid the formation of a Schottky barrier at the metal/ceramic interface.

These materials are very difficult to produce, thus explaining the rarity of their use.

These components can, because of their non-linear current/voltage characteristics (described by an equation of type $\mathbf{I = A\ V^n}$), be used as voltage clamps in power supply. Thus, by combining specific compositions based on barium titanate and strontium, dielectric permittivities ranging between 50,000 and 230,000 have been measured with values of non-linearity (n) of around 15! These components can operate up to 50 V.

5.8.5. *Summary – conclusion*

There is no doubt that ceramic components will take an increasingly important place in many applications, especially for applications involving large gradients of temperature and voltage. At a time when power components with high temperature features occur, it is obvious that ceramic materials will be the only ones likely to promote optimal operations.

Tables 5.3 and 5.4 summarize some of the most important materials mentioned.

Type	Capacity Range (μF)	DC voltage Range (Volts)	Tolerance on capacity (%)	Range of temperature (°C)
Ceramic (small ε) Disk and tube	1 pF–1.0	80–20K	+/–20	–55/+85
Ceramic (large ε) Disk	1 pF–1.0	80–20K	+/–20	–55/+125
Ceramic (small ε) Multilayer	2.5 pF–0.4	25–200	+/–20	–55/+85
Ceramic (large ε) Multilayer	0.033–1.0	3–30	–25+50	–55/+85
Ceramic Layer Barrier	1 pF–1.0	100–400	+/–5	–55/+100
Mica	0.01–4	200–15 K	+/–20	–55/+325
Reconstituted Mica	0.5 pF–0.01	300–500	+/–5	–55/+125
Glass	5 pF–0.004	300–500	+/–5	–40/+70

Table 5.3. *Summary of the main characteristics of the different materials presented*

Type	(ppm/°C)	Maximum Frequency (KHz)	tanδ (%) (1 kHz, 20°C)	tanδ (%) (1 MHz, 20°C)
Ceramic (low ε) Disk and tube	–5000 +100	10^6	< 0.01	0.1
Ceramic (large ε) Disk	–	10^4	1	4
Ceramic (low ε) Multilayer	+30	10^4	0.001	0.1
Ceramic (large ε) Multilayer	–	10^3	1	4
Ceramic Layer Barrier	10^3	1	1	5
Mica	+100	10^7	< 0.1	0.1
Reconstituted Mica	–	10^8	< 0.1	0.1
Glass	+1000	10^6	0.1	0.1

Table 5.4. *Summary of main characteristics of the different materials presented*

5.9. Specific applications of ceramic capacitors in power electronics

In addition to their high capacity per volume unit, the most interesting property of ceramic capacitors for power electronics is the non-linearity of their capacity with the applied voltage. Works have shown the interest of such non-linear ceramic capacitors in three main applications.

5.9.1. *Snubber circuits*

This application seems to be the most interesting because it can limit the switching time and the power that should be dissipated by the resistance of the snubber. Figure 5.33 gives the voltage across a semi-conductor in the particular case of a dissipative snubber. This figure enables a comparison of voltages in the case of linear and non-linear capacities (a) and secondly in the case of two non-linear capacitors (b).

The power dissipation is clearly even lower when the capacitor is non-linear. However, problems related to their withstanding voltage and temperature are likely to limit their use.

5.9.2. *In ZVS*

To reduce blocking losses of dual thyristors, capacitors are placed in parallel on the latter, thus reducing the area of switching operation. Using non-linear capacitors reduces the minimum current necessary for the switching of dual thyristors but also reduces the electromagnetic radiations.

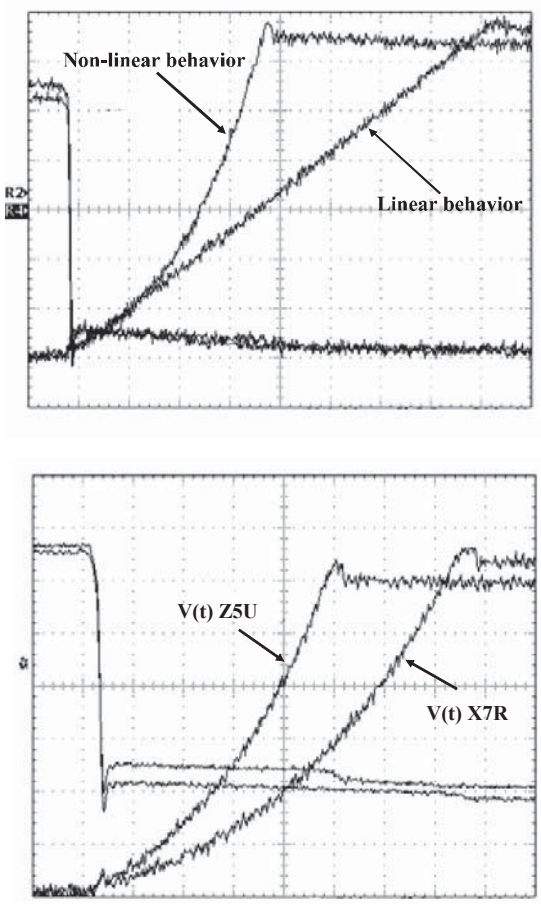

Figure 5.33. *Comparison of voltages for a linear snubber a) and a non-linear snubber b) for two types of non-linear capacitors*

5.9.3. *Series resonant converters*

In these structures, adjusting the power delivered to the load is performed using the switching frequency. The maximum power is given at a switching frequency equal to the frequency of the resonant circuit.

A small non-linearity of the capacitor can improve the dynamics of adjustment and may allow us, when the load is short circuited, to stop the operation of the converter for a backward phase shift operation ($F_d < F_0$) (Figure 5.34).

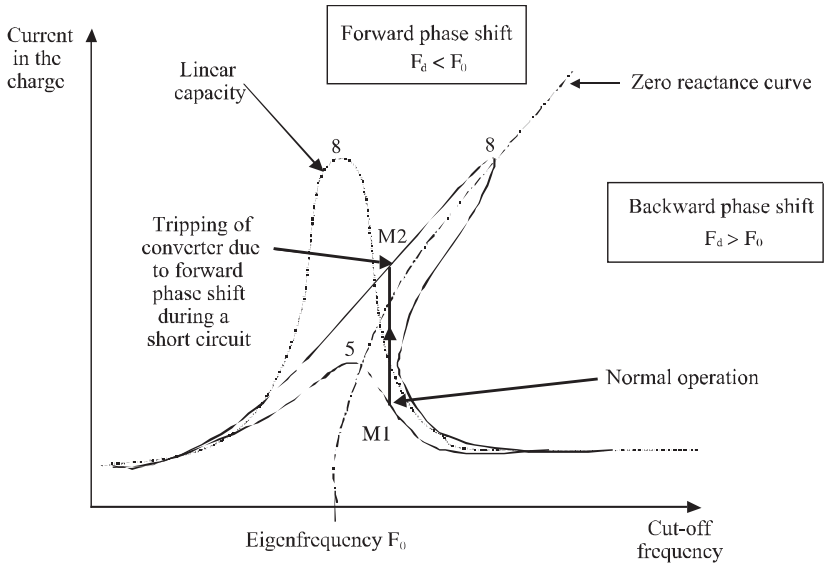

Figure 5.34. *Load current characteristics depending on the reduced frequency for two quality factors (5 or 8)*

5.10. R&D perspectives on capacitors for power electronics

5.10.1. *Film capacitors*

The capacitors made from polymer films (polypropylene, polyester, polystyrene, polycarbonate) currently represent between 25 and 40% of the capacitors available on the market. Due to their low permittivity (always <10), their specific capacity (i.e per unit volume) is low. The R&D focuses mainly on manufacturing processes allowing a decrease in thickness (<1 μm) in a reproducible manner while maintaining the main properties of these materials (reliability, high dielectric strength, low ESR and ESL, etc.).

Meanwhile, works are being carried out on optimizing metallizations (frames) in order to "protect" the component during breakdown or to ensure that the failure is always an open circuit.

Finally, new materials are being explored (polysulfone (PS), polyether ether-ketone (PEEK), polyetherimide (PEI)) which should enable use at temperatures up to 180, 230 and 300°C, respectively.

5.10.2. *Electrolytic capacitors*

The R&D works on aluminum-based electrolytic capacitors are to expand their area of operating voltage via an increase in the anode thickness, to make them more reliable via a monitoring of the electrolyte, and finally to find a replacement fluid with lower resistivities (polypyrol, polythiolen, etc.).

Regarding tantalum-based electrolytic capacitors, encapsulation, packaging, the search for a solution to their use in dry form, or the replacement of MnO_2 current frames by conductive polymers, or finally the development of new geometric structures with several anodes, are all key points in the process of exploration.

5.10.3. *Ceramic capacitors*

The efforts of R&D are currently mainly focused on materials, both dielectric and conductors. Regarding the dielectrics, research concerns the process of implementation to decrease thicknesses, mastering of specific properties (ferroelectricity and anti-ferroelectricity) and reduction of dielectric losses.

Many materials are already candidates whatever the manufacturing process (sol-gel, hydrothermal, thick layers, etc.). They are BT, PZT, SBT, PLZT, etc.

Frames are also subject to particular interest for at least two reasons: the cost of metals employed (noble) (Ag/Pd), and the method of disconnection in the case of failure which should be an open circuit type but is most often a short circuit.

Finally, note that most of these ceramics are particularly suited for integration because of their ease of implementation, their technological compatibility with semiconductors and their excellent thermal properties.

5.11. References

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Chapter 6

Modeling Connections

6.1. Introduction

6.1.1. *Importance of interconnections in power electronics*

Interconnections or, more simply, wiring, have always played an important role in power electronics. The message has always been "cut wire length and decouple the closest semiconductor commutation". Times have not changed, but the era of laboratory converters gave way to series production, where we must now be able to integrate the presence of wiring or interconnections from the moment of conception. The modern components (IGBT) available today are characterized by higher and higher "di over dt". In the high power field (rail traction, naval propulsion, etc.), an area where we encounter probably the biggest constraints currently, current gradients di/dt increase to a few thousand amperes per microsecond, and apply strong constraints on wiring and on switching cell diodes. The existence of such constraints comes from the parallel implementation of several semiconductors, multiplying through this the di/dt in interconnections imposed by the number of chips involved. The phasing out of boxes such as "press-packs", involving wiring by massive conductors naturally very inductive, allows us to suppress more and more often snubber circuits which affect the simplicity and reliability of systems. As a result, the absence of passive components to properly tackle waveforms during the commutations requires new small inductive techniques for wiring. Examples include the development of bus bars regarding applications of medium to high power, or the

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development of isolated metal substrate (IMS) applications for lower power dedicated to large series production.

6.1.2. *The constraints imposed on the interconnections*

The increase in the required performances of converters always leads to more electrical requirements on the interconnections. We can discuss constraints linked to power electronics, electromagnetic compatibility, but also to the reliability of these new techniques.

Consider first the power electronics aspect: we can see that brutal transitions generate significant surge at the interconnection terminals endangering semiconductors. The performance increase of power converters requires putting in parallel and gradually setting a series of semi-conductors, while guaranteeing the compactness and simple solutions. We must therefore try to remove passive circuits necessary for balancing currents or voltages. We will therefore demand these new interconnections to ensure a supply of semiconductors more and more perfect.

Regarding the electromagnetic compatibility (EMC), the increase in switching frequency with the aim of improving the performance of converters (quality of the pulse-width modulation, reducing the size of the filters) and the increased compactness can lead to problems that are called EMC problems. Indeed, the increase in switching frequencies and, by extension, frequencies generated during the commutations, and the shrinking of distances inside devices, lead to increasingly significant acute couplings. We must take care of linkages between power conductors and wires carrying signals.

From a standard point of view, and since shieldings are cut off for cost reasons, it becomes important to be concerned about interconnection radiation and its impact on the spread of conducted noises.

Finally, regarding the reliability of these interconnections, we try to keep voltages ever higher through the dielectric constituents of bus bars or IMS. The operating temperature of these devices, which can reach several dozen degrees Celsius, limits the life time of the equipment. In addition, mechanical constraints are also taken into consideration for high power applications.. These constraints have different consequences. On the one hand, the connection itself may be destroyed in the case of a short circuit (tear, opening of pressed bus bars). However, on the other hand, the forces passed by the bus bars or the massive conductors on the components they supply may damage them.

We are therefore able, after this list, to see how a modern interconnection becomes a fully real component, the design of which results from complex

calculations and sometimes involves many disciplines such as electromagnetism, mechanics, thermal and power electronics (for interactions with semiconductors).

6.1.3. *The various interconnections used in power electronics*

The use of different interconnection technologies depends mainly on the level of power. From the highest level of power to the lowest, we encounter the achievements described below.

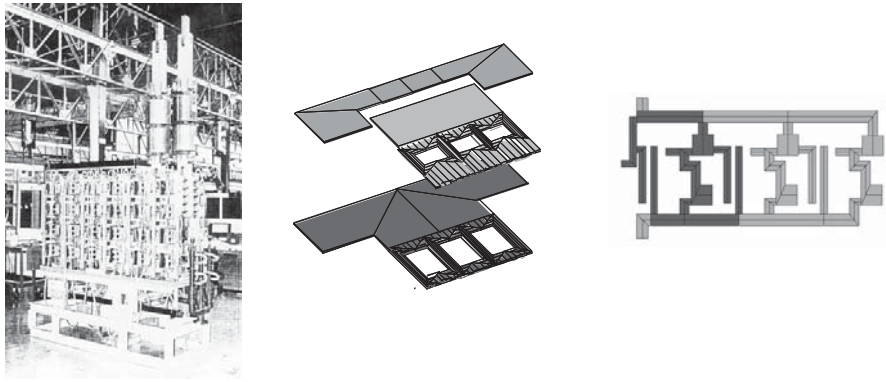
Electrochemistry or electrometallurgy applications involve currents of the order of hundreds of thousands of amperes. Although several converters are made in parallel for reasons of redundancy, currents are still extremely important (several dozen kiloamperes). Generally, the interconnections are made using massive aluminum conductors. We may also cite problems with current distribution between diodes in parallel induced by the dissymmetry of circuits (Figure 6.1a).

We must of course not forget induction heating, when powers and high frequencies make control of wiring inductances necessary. A strong knowledge has been gained in this field.

The railway applications or, more generally, traction applications, require rapid semiconductors (IGBT), but also smaller currents (typically 1,000 amps). This is the domain of bus bars composed of sheets of copper separated by sheets of dielectric (Figure 6.1b).

The automotive applications, requiring both a high reliability and important mass production, are mainly using isolated metallic substrate (IMS) techniques (Figure 6.1c). The wave weld and the heatsink ability of the substrate makes it highly attractive. Also note the achievements of hybrid power modules made on an alumina support. Although the electrical and thermal characteristics are different, they are strongly similar to the case of IMS in its concept.

Finally, the traditional power supplies, for general purposes, often use the classic printed circuit on an epoxy support.



a) b) c)

Figure 6.1. *Different types of connections: a) massive bars, b) erupted bus bar, c) IMS*

6.1.4. *The need to model the interconnections*

On the one hand, the willingness to develop products in an increasingly quick time and at the lowest cost tends to exclude more and more the use of prototypes, at least for applications other than those developed on printed circuit. On the other hand, as noted above, when the power density is greater, the number of constraints and their severity are increased. It is therefore easy to understand that meeting these constraints becomes increasingly difficult empirically or heuristically. It therefore becomes gradually essential to develop models of interconnections mainly reflecting electrical phenomena, but also thermal and mechanical.

If, for the moment, we merely want to know the behavior of electrical interconnections, we need models that can be applied in software commonly used in power electronics (SABER, SPICE, SIMPLORER, etc.).

In this chapter, we propose a method of modeling (PEEC), which seems well suited to the topology of power converters. This method is based on a program called InCa3D. It is possible that in the case of circuit boards, other methods borrowed from microwaves (transmission lines, moments method for calculating the parameters) appear to be more efficient. However, their scope is not as broad and the many examples that we were able to deal with, belonging to all categories of power, confirm us in this approach.

6.2. The method of modeling

6.2.1. *The required qualities*

To be used without restriction in the industry by engineers in power electronics, it was necessary to propose a method that will not require too much skill in electromagnetism or in the field of numerical methods. In particular, the finite element method, widely used for the design of electrical machines, requires a heavy investment which is not justifiable in power electronics, where the design of interconnections, even if it is a decisive phase in a project, has only a limited place in the whole design of a converter.

By the same logic, it is desirable to obtain a modeling of interconnections in the form of located elements easy to integrate in an analysis software of electrical circuits. At the moment, a model in the form of resistances, inductances and mutual inductance, possibly dependent on frequency, is valid for the frequency range extending from continuous to a few megahertz, or even a few dozen megahertz. This model is quite sufficient for the majority of interconnections from medium to high power. Now, in the field of printed circuit boards, or IMS, capacity between tracks and ground plane (radiator, chassis) must be added to take proper account of phenomena.

One of the results provided by the software must be an easy evaluation of the inductive weight of each section of the global interconnection. Considering the hunting down of nanohenry in power electronics, the engineer must know what is the most inductive portion and thus focus its efforts wisely, i.e. consider changes to geometry where it is actually possible to intervene and where the gain is substantial, and finally to know the financial implications. Regarding the interactions between conductors (power and control), the ability to directly edit the value of the mutual inductance is something appreciable.

In power electronics, although the switching frequency is still low, especially for high power (below 10 kHz), current commutations show contributions in frequency bands that are quite high. Even if the well known formula 0.35/tm, where tm is the rise time of the signal can be criticized, however it gives an idea of the frequency with which must be evaluated the parasitic elements of interconnections.

For a large majority of cases, the variation of interconnection parameters with the frequency is quite marginal. The impact of a change in the loop inductance of 50% for a commutation of semiconductors has no known impact both in terms of losses and in terms of spectra. Note that the change in inductance of an interconnection with the frequency depends on the change of distribution of current lines inside the conductor (Figure 6.2).

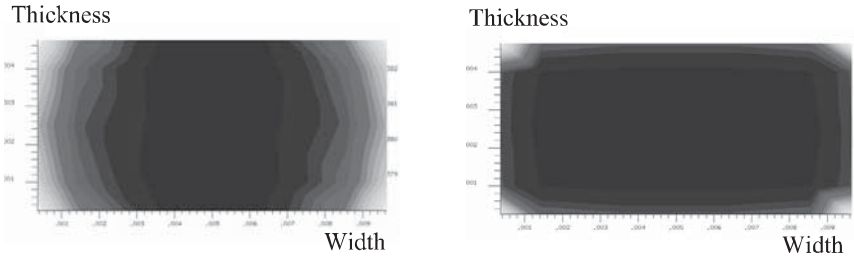


Figure 6.2. *Distribution of current lines for two different frequencies (100 Hz on left, 10 kHz on right) obtained with InCa3D*

The change in interconnection parameters with the frequency comes from two causes that are quite distinct from each other [DJO 94].

The first is what is commonly known as the skin effect, which is to concentrate currents on the edges of conductors and therefore increase the resistance of the conductor since the passage for the proposed current is lower. This effect occurs for a single conductor into the vacuum and submitted to a field created by its own current. The new distribution of current lines maintains the symmetries presented by the straight section of the conductor.

The second effect is the proximity effect, which occurs when the conductor is subject to an outfield that can be produced by a neighboring conductor. In particular, this effect often breaks the symmetry in the distribution of current lines mentioned previously.

6.2.2. *Which method of modeling?*

Having demonstrated the need to model the interconnections with an electric model, it remains to establish formulations to be used depending on the scope and especially the methods of resolution. For calculation of inductance or mutual inductances, Maxwell equations are required, perhaps simplified on the basis of assumptions.

One method of solving these equations, the most commonly used and that which first comes to mind is the numerical finite elements method. It achieves a partition of the problem (or mesh) to form 3D known elements (tetrahedron, brick, etc.) and assesses the unknown function at nodes of these elements. By interpolation throughout the area, the value of the function is then known everywhere. This method is very powerful when it is applied for mapping fields and fluxes (rotating

machines, transformers, etc.). However, it becomes less obvious when we must treat these data in order to obtain the values of global inductances and mutual inductances. Indeed, in the case of interconnections, for the mutual effect of a conductor on others, it will have to be fed by a current or voltage generator (boundary conditions of used formulations) and the various fluxes picked up by other conductors will have to be calculated. This involves as many resolutions as conductors in the problem (one less exactly) to fill in the matrix impedance. Moreover, the mesh size of the problem is closely linked to a particular frequency. Thus, the change in electrical parameters with the frequency requires as many resolutions as the number of values of frequencies. Finally, the structures studied here are mainly static converters for which it is necessary to have an estimate of the contribution of wiring in the air and in the absence of magnetic materials. The finite element method requires us, however, to mesh the entire field, including air, which increases the size of the problem to be solved. The mesh, on which ultimately rests a large part of the finite element method, poses a large problem when it comes to modeling conductors very thin and wide. The designer will be confronted with this when bus bars will be used to achieve the interconnections. Meshing this stacking of conductive plates very thin and very close, with finite elements of good quality, results in unacceptable resolution time. Using elements with potential drops is possible for a single layer, but impossible at present for a stack. For all these reasons, the local approach for solving Maxwell's equations is therefore excluded to model the interconnections [BOT 94].

When conductors become too long, another method exists. This is the TLM approach, which replaces the conductor by a transmission line. This approach is used in microwaves for which the geometry of conductors is simple. It can be adapted to power electronics for special wiring (PCB) as discussed further. The challenge is to correctly model side effects when conductors are short and wide. The complex 3D geometric structures are difficult to model. Finally, it requires the presence of a ground plane used as a reference for electromagnetic coupling. The latter is present in certain applications with medium power and high frequency. However, this is not the case in high power applications. Also, this method of resolution is rejected when it comes to modeling the interconnections of complex geometric shapes for medium frequencies and high powers.

We have just seen that using a local approach is not feasible, as well as a research approach with distributed elements. In addition, we will turn to a comprehensive approach to solving the problem whose result will be the values of localized electrical equivalent schematics of conductors.

This method of solving Maxwell equations exists. This is the PEEC (*Partial Element Equivalent Circuit)* method, which decomposes the vector potential and its circulation on each portion of the straight conductor, to evaluate the contribution of

each of them on the total inductance of the current loop. Thus, the immediate results are partial elements, inductances and mutual inductances between conductors. The side effects are automatically reflected in this approach.

6.2.3. *Brief description of the PEEC method*

This method comes from A.E. Ruehli, an engineer at IBM, who in the 1970s was instructed to model the interconnections of digital computer boards [RUE 72, RUE 74, RUE 79]. He noted that the transmission line method was not sufficient to correctly model all types of interconnections. In particular, the very short interconnections inside integrated circuits did not seem to be properly represented. This was mainly due to the invalidity of the basic assumption of the transmission line method: the existence of fields crossing the propagation direction of the current, mainly for short interconnections. At its origin, only an inductive and resistive modeling was carried out, then improvements were made on electrostatic phenomena, and then were taken into account delays related to propagation.

Our main contribution in adapting this method to power electronics focuses on techniques to represent the skin effect and proximity effect by meshing rectangular sections and all the analytical work that was undertaken to correctly represent 3D structures and very complex connections.

6.2.3.1. *Principle*

This method is based on the partial element concept: partial resistance, inductance and mutual inductances. More specifically, it is based on the fact that a current loop can be broken into straight components each contributing to the impedance of the total closed circuit. The vector potential and its circulation are decomposed on each element, which can determine their contribution. The total resistance of a current loop will be the sum of partial resistances of each element and its total inductance is the sum of all inductances and mutual between these inductances:

$$R_b = \sum_{n=1}^{N} R_{pn}$$

$$L_b = \sum_{m=1}^{N} \sum_{n=1}^{N} M_{pmn}$$

– Rpn: partial resistance of element *n*;

– Mpmn: partial mutual inductance of element *n* on element *m*;

– Mpnn: partial inductance of element *n*.

The value of the partial resistance of an element is given by:

$$R_s = \frac{\rho L}{S}$$

– ρ: resistivity of the material (Ω.m);

– L and S: length (m) and section (m^2) of the element.

In air and in the absence of magnetic material, the partial mutual between two massive parallel conductors is calculated, also from an analytical expression after successive integrations of vector potential. By assuming a uniform current density in the straight section of the two conductors, this value depends only on geometric characteristics of these elements (Figure 6.3) [HOE 65]. The partial inductance is then a mutual element on itself (E = P = l3 = 0, l1 = l2, a = c, b = d).

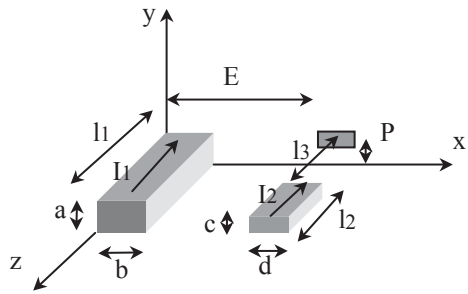


Figure 6.3. *Definitions for the calculation of the partial elements with the PEEC method*

We give below the exact formula (equation E) because it is the basis of calculations of inductances and it is important to know the different elements it comprises. The value of M is obtained in μH with a definition of the sides in cm.

To implement these formulations in case of power electronic interconnections, we must dissociate the geometry of connections into elements of straight conductors for which the assumption of uniform current density is valid.

$$M = \frac{0.001}{abcd}\left[\left[\left[\left(\frac{y^2z^2}{4}-\frac{y^4}{24}-\frac{z^4}{24}\right)x\ln\frac{x+\sqrt{x^2+y^2+z^2}}{\sqrt{y^2+z^2}}+\right.\right.\right.$$
$$\left(\frac{x^2z^2}{4}-\frac{x^4}{24}-\frac{z^4}{24}\right)y\ln\frac{y+\sqrt{x^2+y^2+z^2}}{\sqrt{x^2+z^2}}+$$
$$\left.\left.\left(\frac{y^2x^2}{4}-\frac{y^4}{24}-\frac{x^4}{24}\right)z\ln\frac{z+\sqrt{x^2+y^2+z^2}}{\sqrt{y^2+x^2}}+\right.$$
$$\frac{1}{60}\left(x^4+y^4+z^4-3y^2x^2-3y^2z^2-3x^2z^2\right)\sqrt{x^2+y^2+z^2}-$$
$$\frac{xyz^3}{6}Arctg\frac{xy}{z\sqrt{x^2+y^2+z^2}}-\frac{xy^3z}{6}Arctg\frac{xz}{y\sqrt{x^2+y^2+z^2}}-$$
$$\left.\frac{x^3yz}{6}Arctg\frac{zy}{x\sqrt{x^2+y^2+z^2}}\right]_{E+d-b,E}^{E-b,E+d}(x)\left]_{P+c-a,P}^{P-a,P+c}(y)\right]_{l3+l2-l1,l3}^{l3-l1,l3+l2}$$

(equation E), with:

$$\left[\left[\left[f(x,y,z)\right]_{q2,q4}^{q1,q3}(x)\right]_{r2,r4}^{r1,r3}(y)\right]_{s2,24}^{s1,s3}(z)=\sum_{i=1}^{4}\sum_{j=1}^{4}\sum_{k=1}^{4}(-1)^{i+j+k+1}f(qi,rj,sk)$$

6.2.3.2. *1D, 2D… assumptions*

The geometric shape of conductors encountered in power electronics will, in most cases, make possible the assumption of unidirectional lines of current. This is the case with massive bars and conductors for which the length is large compared to the width and thickness. The conductor model will be a LR series circuit (Figure 6.4a).

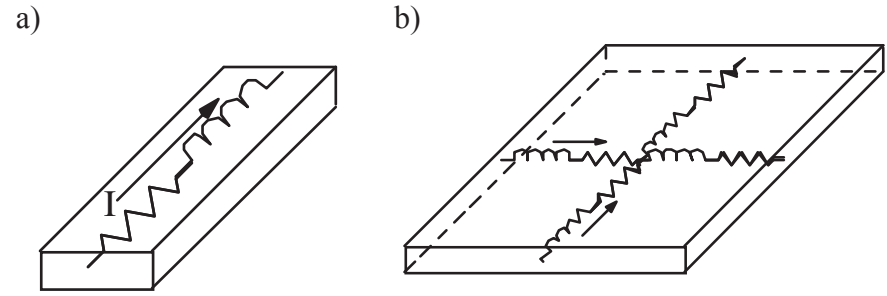


Figure 6.4. *(a) 1D and (b) 2D model*

Considering bus bars, interconnections for which the current often comes from a point to be distributed later, this 1D assumption is no longer valid. A 2D model is then developed (Figure 6.4b), which allows current lines to go in two perpendicular directions.

Then in this case only circulating currents in the thickness of the bus bar plates are neglected. Given the frequency range, this assumption is justified. It is therefore not necessary at this time to develop a 3D model.

6.2.3.3. *Ground plane*

The structures in power electronics are often located on a radiator or a chassis which acts as a ground plane. Hence currents flow inside it and their influence will modify the electrical characteristics of interconnections located above.

The easiest way of modeling is the image method [PED 91]. It replaces a conductor above a perfect ground plane (infinite and infinitely conductive) with the same conductor and its image fed by opposed currents if it is parallel to the plane (Figure 6.5a) and currents of same direction if it is perpendicular to the plane (Figure 6.5b). In the first case, the equivalent inductance is $L'_1 = L_1 - M_{1i}$ and in the second case $L'_1 = L_1 + M_{1i}$ (partial resistance is unchanged because the ground plane is considered ideal).

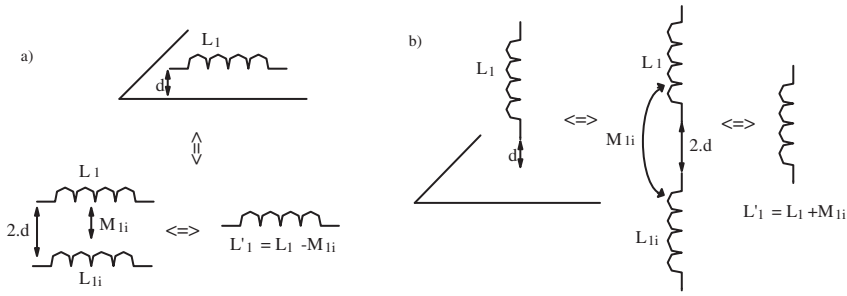


Figure 6.5. *Different positions of the conductor located above the ground plane*

The assumption of a perfect ground plane is in most cases valid: it is sufficient to have a material being either very good conductor (copper or aluminum) and with transverse dimensions relatively large compared to dimensions of the circuit located above [SCH 94].

Another problem exists when the structure is surrounded by a box, then you are in the presence of several ground planes. In this case, the images method is very difficult to apply because it can lead to a large number of images.

If it is not possible to assume a perfect ground plane, it must be seen as a conductor and meshed in the same way as other elements of the circuit. In this case, take a lot of care with the meshing, which will require the use of, in most cases, 2D elements.

6.2.3.4. *Mesh*

The underlying assumption used is that the current density is uniform in the straight section of conductors. We have already seen that for large plates, the current direction was not known, which led to 2D mesh-types (section 6.2.3.2). Another issue that may require a mesh is the frequency. Indeed, with increasing frequency, a redistribution of current lines occurs (skin effect): this is not symmetric if there are other conductors close to the one under consideration (proximity effect).

For a straight conductor, for which current lines have a preferred direction, the section will be only meshed into elements of smaller section and of the same length (Figure 6.6). In this latter case, the length of conductors will not be discretized assuming that frequency is not too high (length of the conductor compared to the wavelength). This reduces the number of elements, as compared to a finite element method.

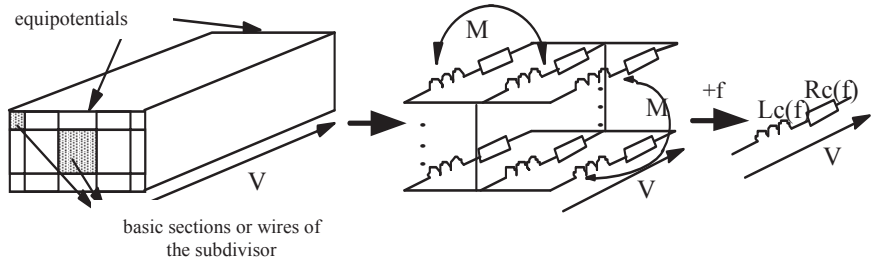


Figure 6.6. *Obtaining electrical characteristics of a conductor depending on the frequency with a subdivision of its section*

In the case of a 2D model, the mesh will be finer depending on the frequency. This methodology has been implemented in a simulator called InCa3D®, consisting of a 3D geometric descriptor, a mesh assistant, a calculation module and a post treatment.

6.3. The printed circuit board

The method described above obviously applies in the case of printed circuit board. Analytical formulations are similar to equation E: they are even intermediate results obtained in the course of integration. However, with generic software, they add no particular advantage:

– the printed circuit board is used in many fields other than power electronics, many works have been completed, including high-frequency electronics;

– modeling them is based on the transmission line theory, possibly multiconductors. Then the parameters of these lines are calculated: resistances, inductances, capacitances and couplings, all these quantities are per unit length parameters;

– the use of these methods is allowed in the case of printed circuit boards, because the plane structure offers simple geometries, unlike static power converters, which include 3D wiring.

6.3.1. *Introduction*

Printed wiring is commonly used in high frequency and average power converters. Also, modeling must be able to simultaneously take into account all electromagnetic phenomena:

– self- and mutual inductance between tracks;

– capacitive effect in relation to a plane and between tracks;

– resistive effect, function of frequency: skin effect and proximity effect;

– existence of a conductor near the wiring (chassis or heatsink).

In order to achieve a simulation tool for printed wiring dedicated to computer-aided design, the analytical method must be inexpensive considering computing time. If we further consider that the electric field in a print conductor has only one direction, that of its greatest length, the problem becomes 1D, facilitating further formulations. Thus, the proposed method uses line theory. It allows assuming some adaptations to answer the imposed criteria. The principle used is to share a printed wiring in rectangular segments, oriented in the direction of the current, themselves divided into thin conductors placed in parallel (Figure 6.7). On this decomposition line theory can thus apply. Indeed, the analytical expressions of the per unit length inductances, capacitances and mutual couplings for this type of row form conductors are known [LEE 86]. The calculation of row currents allows us, knowing the voltage conditions at the ends, to determine an overall equivalent impedance and finally its representation by a "circuit" model. Thus, a conductor is represented by a four pole impedance referenced to a ground plane, which can take into account both the differential mode and common mode effects.

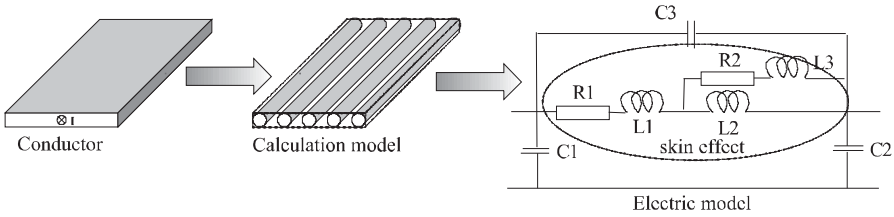


Figure 6.7. *Principle of modeling*

6.3.2. *Thin wire method*

6.3.2.1. *Principle of the method*

Studies cited in [MAC 93, PET 96] showed equivalence between a micro strip line and a bundle of N thin conductors parallel between them (Figure 6.8), insofar as a minimal distribution of thin conductors per centimeter is respected.

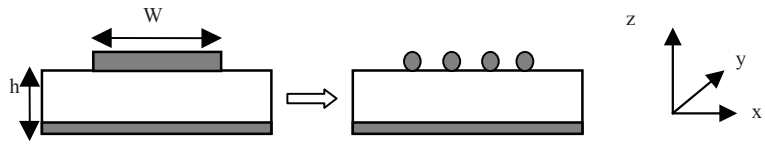


Figure 6.8. *Equivalence to a set of thin conductors*

These *N* thin conductors are immersed in an environment which characterizes an equivalent dielectric substrate. The principle is to calculate the electrical parameters of the line from geometry and material. The frequency resolution method is based on the transmission line theory for multiconductors. This model requires the resolution of the system:

$$\frac{d^2[I]}{dz^2} = [Y].[Z].[I]$$

$$\frac{d^2[V]}{dz^2} = [Z].[Y].[V]$$

The matrices of linear impedance and admittance [Z] and [Y] are defined from:

$$[Z] = [R] + j\omega[L]$$

$$[Y] = [G] + j\omega[C]$$

[L] and [R] represent matrices of linear inductance and resistance; [C] and [G] symbolize matrices of linear capacity and conductance. The latter is supposed to be zero as we consider no losses in the dielectric: [G] = 0.

Depending on the operating frequency, a quasi-TEM mode is assumed to propagate throughout the micro strip line. It equates to a pure TEM mode. Although the propagation environment is inhomogenous, the structure may be treated as an homogenous environment of effective permittivity ε_{eff}. This value is calculated from expressions of by Wheeler, Schneider and Hammerstad [SCH 69, WHE 77]. It can also be calculated by the finite element method in 2D. The capacitance matrix is deducted from the inductance matrix by a simple inversion.

$$[C] = \mu_0 . \varepsilon_{eff} . [L]^{-1}$$

6.3.2.2. *Solving equations*

The resolution of a system requires us to reduce the product (Y)(Z) to diagonal to move in the modal basis. In fact, the product (Y)(Z) is not diagonal since losses in the lines are taken into account. The matrices of passage (Ti), respectively (Tv) are determined, they allow the reduction to diagonal of (Y)(Z), respectively (Z)(Y):

$$(I) = (Ti)\,(i)$$

$$(V) = (Tv)\,(v)$$

where (i) and (v) are matrices of the current and voltage in the modal basis. The differential equation of the second order of the matrix system is then written:

$$\left(\frac{d^2 i}{dz^2}\right) - (\gamma_p)^2(i) = 0$$

$(\gamma_p)^2$=(Ti) – 1(Y)(Z)(Ti) is the diagonal matrix for propagation in the modal basis. The solution of the system is given by:

$$\left[i(z)\right] = e^{[\gamma_p]z}[A] + e^{-[\gamma_p]z}[B]$$

where [A] and [B] are determined using the boundary conditions. The matrices of the current and voltage in the original basis are obtained by the relationship above.

6.3.3. *Expressions of per unit length parameters*

The analytical formulation of per unit length parameters is the focal point of this method. This should help take into account all the effects you want to represent, whatever the geometries and disposition of thin conductors (not parallel, non-coplanar, etc.) even in non necessarily homogeneous media. We present two families of formulation: the first assumes that the conductor is very long compared to its width (ratio greater than 4). In this case we use simple formulations since we assume infinite conductors. In a second case, we take into account the finished length of thin conductors. The formulation is more complex and we use the PEEC method applied to cylindrical conductors of finished length. Finally, the computing time is linked to the meshing of printed conductor. Two types of meshing are proposed:

– a linear distribution which has the disadvantage of computational cost increasing with the width of the track;

– a geometric distribution which allows a constant number of thin wires regardless of the width of the track, and is therefore more interesting for calculation time, but needs to be adapted according to the operating frequency range.

6.3.3.1. *Linear distribution of thin wires*

The determination of per unit length parameters reduces to the calculations of inductance and resistance matrices. Consider a set of *N* thin wires coupled over a ground plane (Figure 6.9).

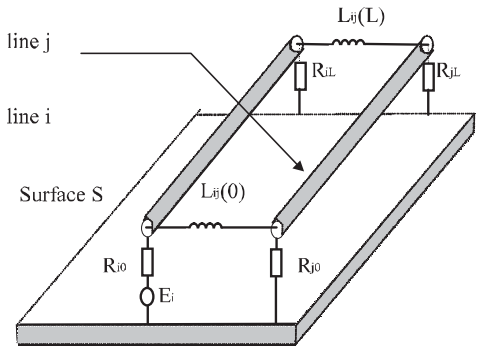


Figure 6.9. *Electric representation*

The elements of the inductance matrix (Lij) are calculated by the traditional analytical formulations of cylindrical conductors, assuming the thin wires of infinite length and interwire distance d_0 much higher than their diameter ϕ. This is equal to the thickness of the micro strip line.

$$L_{ii} = \frac{\mu_0}{2\pi}.\ln\left(\frac{4.h}{\phi}\right) + L_{\text{int}\,erne}$$

$$L_{ij} = \frac{\mu_0}{4\pi}.\ln\left(1 + \frac{4.h^2}{d_{ij}^2}\right)$$

where dij means the interwire distance.

Skin effect and proximity effect phenomena are also taken into account as well as the change in internal inductance of thin wires. Recent work [GAU 00] gives an analytical expression of the internal per unit length inductance using Kelvin

functions. However, the contribution of internal inductance has little influence on the accuracy of the "thin wire" model made up of conductors of small cylindrical diameter. It is nevertheless important for conductors of large section. The resistive effect is important in the frequency band studied in power electronics. Also, the conductor model introduced the per unit length resistance matrix [R] which depends directly on the frequency. In the case of the linear distribution of conductors, the per unit length equivalent resistance of a thin wire is expressed by:

$$R_{fil} = N.\frac{\gamma}{\sqrt{2}.\sigma.(w+\phi)}.F\_R_{Bessel}\left(2\gamma.\frac{w.\phi}{w+\phi}\right)$$

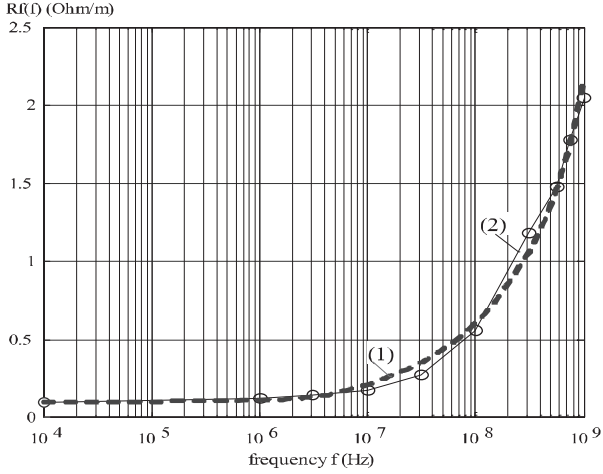
N: number of thin wires describing the printed conductor.

F_RBessel is defined by:

$$F\_R_{Bessel}(x) = \frac{Ber_0(x)Bei_1(x) - Ber_0(x)Ber_1(x) - Bei_0(x)Bei_1(x) - Bei_0(x)Ber_1(x)}{Ber_1^{\,2}(x) + Bei_1^{\,2}(x)}$$

$$\text{with: } \gamma = \sqrt{\omega\mu\sigma}\ \ \Omega/\text{m}$$

Figure 6.10 shows that this analytical function properly reflects the evolution of resistance with frequency. The reference values are derived by calculating with finite elements. The example is a track 5mm wide and 35 μm thick.



Curve (1) (dotted) corresponds directly to the evolution of this function.

Curve (2) is the result obtained by calculating the resistance by finite elements

Figure 6.10. *Evolution of linear resistance for a 5 mm wide track: comparison between thin wire method and finite element method*

It is therefore possible to obtain a total impedance of a printed track with a good accuracy, as shown in Figure 6.11. However, one of the disadvantages of this method results from increasing the size of matrices with the width of the tracks. Accordingly, the computing time can become prohibitive. Also one change is to adopt a non-linear distribution of thin wires.

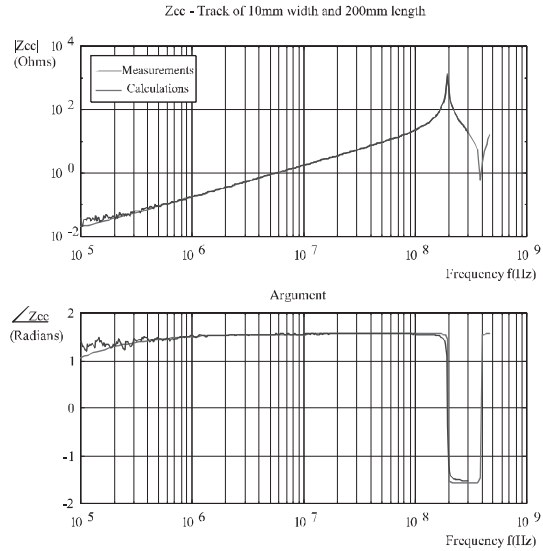


Figure 6.11. *Example of track impedance calculated by the thin wire method*

6.3.3.2. *Non-linear distribution of thin wires*

The observation of the distribution of current density in a track led to develop a new distribution of wires in order to reduce the computing time. To this effect, thin conductors are concentrated on the edges of the track (Figure 6.12). The calculation of the interwire distance achieved through an arithmetic reason r:

$$d_n = d_0 + n.r$$

n represents the number of wires in the first half of the track. Given the symmetry of the system, the distribution of wires is made solely for the first half of the track. The total number of wires is equal to:

$$n_{\text{wire}} = 2\ (\text{n} + 1) + 1$$

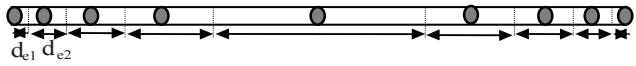


Figure 6.12. *Non-linear distribution of thin wires*

The vector = [de1 de2 ... de*n*] can represent the position of thin wires.

with: $d_{e1} = \frac{d_0}{2}$ and $d_{en} = \frac{1}{2}.\left(d_{n-2} + d_{n-1}\right)$

We then obtain the expressions of inductance and resistance matrices:

$$\left[L_{ij}\right] = \frac{\mu_0}{4\pi}.\ln\left(1 + 4.h^2.\left[d_{ij}\right]^{-1}\right)$$

$$\left[R\right] = \frac{F\_R_{Bessel}\left(\phi,\delta\right)}{\sigma.\phi}.\left[d_e\right]^{-1}$$

[dij] is the distribution matrix of non-linear thin wires and δ the skin thickness.

Figure 6.13 shows a comparison between the two meshing modes of a printed track for calculating the current density in the section. Both methods converge satisfactorily; the gain in computing time is very significant.

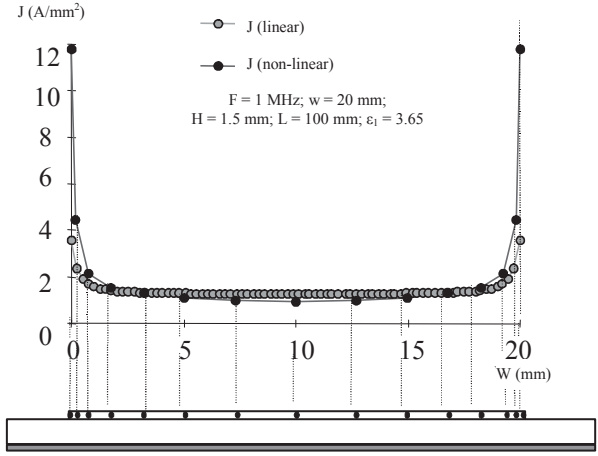


Figure 6.13. *Comparison of current densities depending on the meshing of the track*

This method reduces the CPU time. It maintains a constant calculation time whatever the width of the track. However, the distribution of conductors is optimized for a certain frequency range. The distribution must be adapted according to this criterion. For example, some values of computing time are given in Table 6.1, depending on the method. The calculation concerns the impedance of a line for 60 values of frequencies compatible with the chosen distribution.

Width of the line studied (mm)	Number of wires in the linear case	CPU time (s)	Number of wires in the non-linear case	CPU time (s)
5	20	71.73	15	15.44
10	40	307.75	15	15.22
20	80	1540	15	15.16

Table 6.1. *CPU time depending on discretization of thin wires*

6.3.3.3. *General formulation of per unit length inductances*

In the previous sections, the per unit length parameters are independent of the length, which introduces errors in the case of short tracks. To solve this issue, the principle is to use the PEEC method to calculate equivalent linear parameters for cylindrical thin wires of finished length.

The calculation of the terms of matrix [L] requires taking into account the neighboring conductors denoted wire 2 and its respective image wire 3 (Figure 6.14).

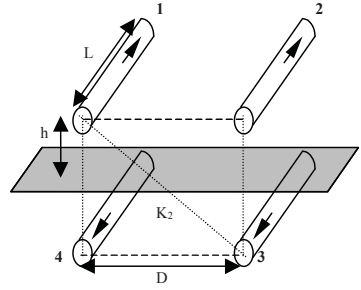


Figure 6.14. *Coupling thin wires above ground plane*

By definition: Lij = Lp12 – Lp13 (H/m)

This concludes formulations given by:

$$L_{p12} = \frac{\mu_0}{2\pi}.\left\{\ln\left[\frac{L}{D} + \sqrt{1+\left(\frac{L}{D}\right)^2}\right] - \sqrt{1+\left(\frac{D}{L}\right)^2} + \frac{D}{L}\right\}$$

$$L_{p13} = \frac{\mu_0}{2\pi}.\left\{\ln\left[\frac{L}{K_2} + \sqrt{1+\left(\frac{L}{K_2}\right)^2}\right] - \sqrt{1+\left(\frac{K_2}{L}\right)^2} + \frac{K_2}{L}\right\}$$

where: $K_2 = \sqrt{D^2 + 4h^2}$.

If the length is large compared to the width of the line, we find the analytical expressions above. Figure 6.15 shows the change in the per unit length mutual inductance for two thin wires distant from 175 μm, located in a conductor having a width of 5 mm, a thickness of 35 μm and placed at 1.5 mm above the ground plane.

Depending on the length of the track, we can choose a formulation independent of the length or that takes into account, this is to optimize the CPU time.

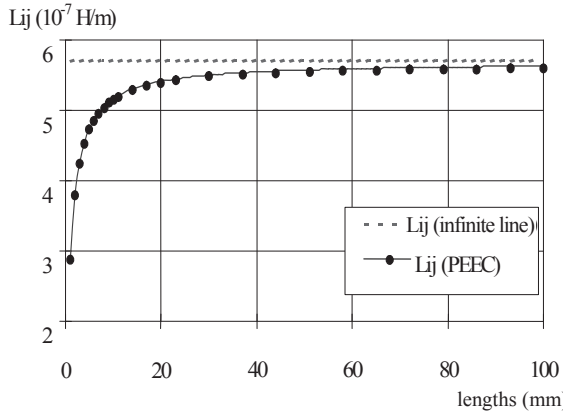
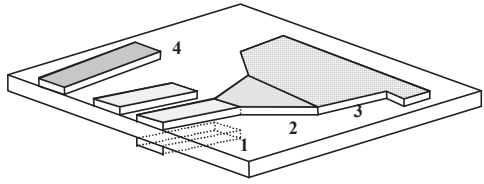


Figure 6.15. *Change in linear mutual inductance with the length*

6.3.3.4. *Extension of the method to non-parallel lines and multilayer lines*

It is possible to generalize the previous formulation to cases of non-parallel and non-coplanar conductors. This extension allows us to treat all types of conductors, including multilayer circuits (Figure 6.16).



1: double face tracks

2: enlarged tracks

3: massive tracks

4: coupled tracks, parallel or not

Figure 6.16. *Examples of topologies that can be managed by the thin wire method*

The difficulty in this case concerns areas whose permittivities are different. Line theory applies well in an isotropic environment. Different methods exist for determining an equivalent permittivity [BAT 89]. To illustrate case 2 (enlarged tracks) an example of formulation is given in the case of coplanar conductors.

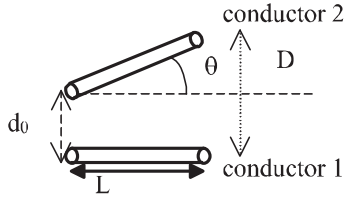


Figure 6.17. *Non-parallel conductors*

$$L_{ij} = \frac{\mu_0 \cos\theta}{4\pi\sqrt{1+\tan^2\theta}} \cdot \ln\left\{ \frac{\left(\frac{L}{2}+A+\sqrt{\left(\frac{L}{2}+A\right)^2+B^2}\right)\left(-\frac{L}{2}+A+\sqrt{\left(-\frac{L}{2}+A\right)^2+C}\right)}{\left(-\frac{L}{2}+A+\sqrt{\left(-\frac{L}{2}+A\right)^2+B^2}\right)\left(\frac{L}{2}+A+\sqrt{\left(\frac{L}{2}+A\right)^2+C}\right)} \right\}$$

The constants A, B and C are determined by the length L and the distance d_0. The curve of Figure 6.18 illustrates the evolution of per unit length mutual inductance L_{ij} depending on the angle θ. It should be noted that mutual inductance between the two orthogonal conductors is quasi-zero.

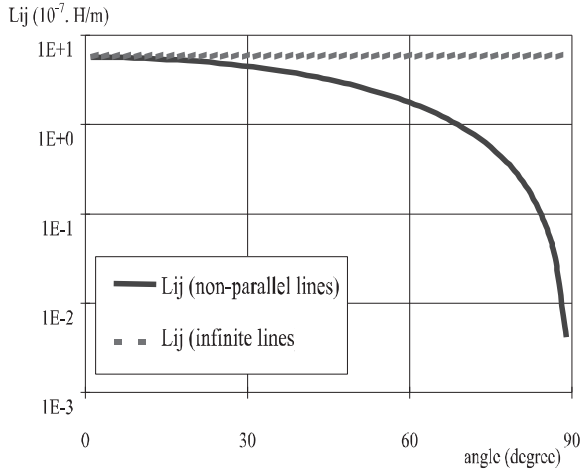


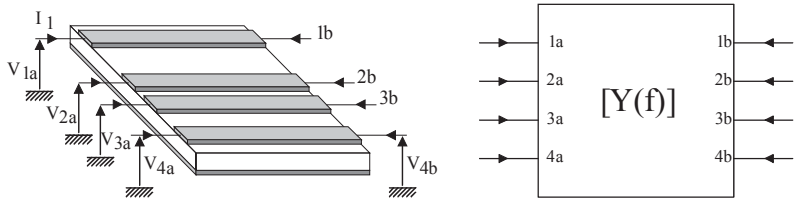
Figure 6.18. *Change in mutual depending on the angle*

The previous formulation is generally applied to non-coplanar conductors, which can solve the case of a multi-layer printed circuit board.

6.3.4. *Representation by multi-poles, "circuit" modeling*

6.3.4.1. *Couplings between tracks*

The thin wires method allows us to calculate the coupling between different segments of parallel tracks. We must then consider all these segments of the track as a multi-pole, characterized by an overall matrix of admittance [Y]. In the case of N segments of coupled tracks, the multi-pole is connected to $2N$ ports and the corresponding matrix of admittance has a dimension $2N \times 2N$.



4 tracks ⇔ 8 ports: matrix Y(f) 8 × 8

Figure 6.19. *8 port multi-pole*

Because of symmetries, the number of different primary admittances defined in the matrix Y(f) is less than the total number of elements of the matrix. Thus, for a 8 × 8 matrix (4 coupled tracks), there are actually 20 different admittances defined. If a complete model of electrical coupling between the four tracks is sought, these 20 admittances must be correctly reproduced, which implies a complex electric model and complex calculation of parameters, and therefore a high CPU time. A possible simplification is to only take into account linkages between adjacent tracks. The former problem was thus reduced to the study of three couplings between two tracks, which is the calculation of three 4 x 4 matrices.

To limit the number of couplings to be taken into account in the printed circuit model, a criterion has been defined in [PET 96]. The criterion allows determining the significant couplings considering the geometrical characteristics of segments of track, and maximum current that can cross each segment.

6.3.4.2. *"Circuit" modeling*

The ultimate goal of the multi-polar formalization is then to build an electric model of circuit type of *N* coupled tracks to be easily simulated by SPICE type software. The "circuit" model will then include only R, L, C and inductive couplings terms. Having calculated the electrical characteristics of different segments of tracks using the thin wire method, it is necessary to determine the circuit models to use, as well as the parameters of these models to accurately simulate the behavior of printed circuit boards. This process is represented in Figure 6.20.

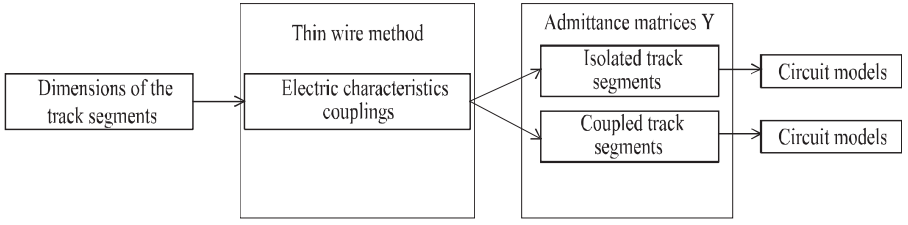


Figure 6.20. *Approach to obtain circuit models*

The parameters of the "circuit" model are determined automatically by an identification software from admittance matrices. In a first phase, the frequency range is shared into three zones, which correspond to different dominant behaviors of the segment of the track (resistive, inductive and with propagation). The model parameters are determined by frequency range where each effect is dominant.

6.3.4.3. *Example of application on the case of two coupled tracks*

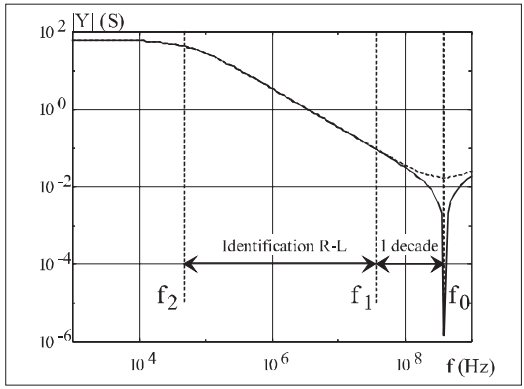


Figure 6.21. *The different areas of frequencies*

In the example below, we present the method of identification of the circuit model. The thin wire method enables us to obtain the admittance matrix [Y] of the system of two coupled tracks. The matrix is size 4 x 4. An example of parameters Y_{ij} is shown in Figure 6.21.

We can see several areas of frequencies in which the behavior of admittances are characteristics:

– $f < f_2$, impedance behavior is resistive;

– $f_2 < f < f_1$, impedance behavior is inductive;

– $f > f_0$, impedance presents a capacitive behavior.

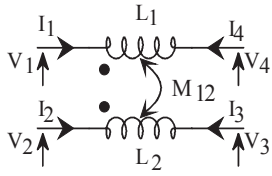
The frequency f_0 corresponds to the resonance of the track. This is the same for all parameters Y of the system and depends only on the length of the track and the permittivity of the environment

$$\left(f_0 = \frac{1}{2\ell \cdot \sqrt{\varepsilon \mu_0}} \right)$$

This is used to identify the different terms of the "circuit" model according the frequency band.

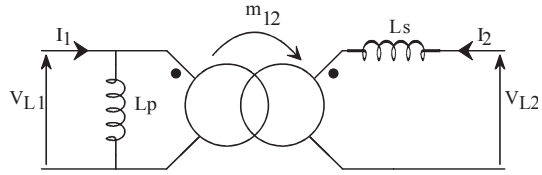
6.3.4.3.1. Inductive coupling

The first step is to represent the inductive coupling between segments of tracks. A simple model is depicted in Figures 6.22 and 6.23 with the corresponding formulations.



$$\begin{cases} V_{L1} = L_1 \dfrac{dI_1}{dt} + M_{12} \dfrac{dI_2}{dt} \\ V_{L2} = M_{12} \dfrac{dI_1}{dt} + L_2 \dfrac{dI_2}{dt} \end{cases}$$

Figure 6.22. *Equivalence between segments of tracks and coupled inductors*



$$L_p = L_1 \qquad L_s = \frac{L_2}{1 + \dfrac{M_{12}^2}{L_1^2}} \qquad m_{12} = \frac{M_{12}}{L_1}$$

Figure 6.23. *Equivalent representation of inductive coupling*

The electrical parameters of the model are then identified under the matrix [Y] (calculated using the thin wire method) using a numerical identification method. It concerns the resistive and inductive terms.

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{12} & Y_{22} \end{bmatrix} \cdot \begin{bmatrix} (V_1 - V_4) \\ (V_2 - V_3) \end{bmatrix}$$

By identification on the domain [f2, f1], we obtain:

$$L_1 \cdot \omega = \frac{Y_{22}}{Y_{11}Y_{22} - Y_{12}^2} \qquad L_2 \cdot \omega = \frac{Y_{11}}{Y_{11}Y_{22} - Y_{12}^2} \qquad M_{12} \cdot \omega = \frac{-Y_{12}}{Y_{11}Y_{22} - Y_{12}^2} \;;$$

The skin and proximity effects that result in a variation of resistance with frequency are represented by R-L networks, as shown in Figure 76.24.

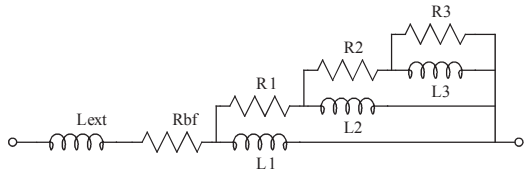


Figure 6.24. *R-L network – equivalent schematic to model the skin effect*

The number of cells depends on the frequency range on which we wish to represent the phenomenon. The parameters of the model are identified using the matrix [Y] for f <f2.

6.3.4.3.2. Multiple capacitive coupling

From capacitive model of tracks represented on Figure 6.25, the second step is to identify capacitances of each segment and capacitive couplings between adjacent segments of track.

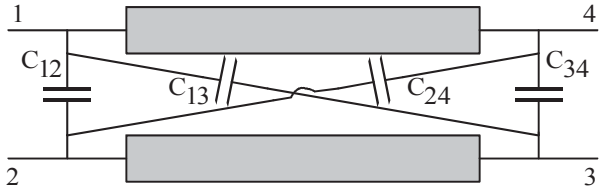


Figure 6.25. *Coupling capacities between two segments of track*

The capacitances are identified using the matrix [Y] calculated by the thin wires method. The following relationships are established for the model of Figure 6.25:

$$\begin{cases} I_{1capa} = (C_{11}+C_{12}+C_{13}+C_{14})\cdot\dfrac{dV_1}{dt} - C_{12}\cdot\dfrac{dV_2}{dt} - C_{13}\cdot\dfrac{dV_3}{dt} - C_{14}\cdot\dfrac{dV_4}{dt} \\ I_{2capa} = -C_{12}\cdot\dfrac{dV_1}{dt} + (C_{12}+C_{22}+C_{23}+C_{24})\cdot\dfrac{dV_2}{dt} - C_{23}\cdot\dfrac{dV_3}{dt} - C_{24}\cdot\dfrac{dV_4}{dt} \\ I_{3capa} = -C_{13}\cdot\dfrac{dV_1}{dt} - C_{23}\cdot\dfrac{dV_2}{dt} + (C_{13}+C_{23}+C_{33}+C_{34})\cdot\dfrac{dV_3}{dt} - C_{34}\cdot\dfrac{dV_4}{dt} \\ I_{4capa} = -C_{14}\cdot\dfrac{dV_1}{dt} - C_{24}\cdot\dfrac{dV_2}{dt} - C_{34}\cdot\dfrac{dV_3}{dt} + (C_{14}+C_{24}+C_{34}+C_{44})\cdot\dfrac{dV_4}{dt} \end{cases}$$

The symmetries of the system can reduce the number of independent terms Y_{ij} and therefore the number of capacitances to be determined noting that:

$$\begin{cases} C_{11} = C_{44} \\ C_{22} = C_{33} \\ C_{12} = C_{34} \\ C_{13} = C_{24} \end{cases} \quad \text{and} \quad \begin{cases} Y_{11C} = Y_{44C} = (C_{11} + C_{12} + C_{13} + C_{14}) \cdot s \\ Y_{22C} = Y_{33C} = (C_{12} + C_{22} + C_{23} + C_{13}) \cdot s \\ Y_{12C} = Y_{21C} = Y_{34C} = Y_{43C} = -C_{12} \cdot s \\ Y_{13C} = Y_{31C} = Y_{24C} = Y_{42C} = -C_{13} \cdot s \\ Y_{14C} = Y_{41C} = -C_{14} \cdot s \\ Y_{23C} = Y_{32C} = -C_{23} \cdot s \end{cases}$$

The values of capacitances are identified from the knowledge of the previously calculated inductance matrix and the resonant frequency f_0 of each term Y_{ij}. We can write that:

$$[Y] = [Y_L] + [Y_C]$$

The terms Y_{11}, Y_{22} and Y_{12} have the same anti-resonance frequency, whereas the terms Y_{13}, Y_{14} and Y_{23} have a minimum for this frequency. It follows that, at this particular frequency, capacitances can be determined from the following relationships:

$$Y_{11} = \frac{L_2}{(L_1 L_2 - M_{12}^2) \cdot p} + (C_{11} + C_{12} + C_{13} + C_{14}) \cdot p$$

$$Y_{22} = \frac{L_1}{(L_1 L_2 - M_{12}^2) \cdot p} + (C_{12} + C_{22} + C_{23} + C_{13}) \cdot p$$

$$Y_{12} = \frac{-M_{12}}{(L_1 L_2 - M_{12}^2) \cdot p} - C_{12} \cdot p \qquad Y_{13} = \frac{M_{12}}{(L_1 L_2 - M_{12}^2) \cdot p} - C_{13} \cdot p$$

$$Y_{14} = \frac{-L_2}{(L_1 L_2 - M_{12}^2) \cdot p} - C_{14} \cdot p \qquad Y_{23} = \frac{-L_1}{(L_1 L_2 - M_{12}^2) \cdot p} - C_{23} \cdot p$$

The complete model of the two coupled tracks is shown in Figure 6.26. Its interest lies in the modularity. Indeed, according to the dynamic applied, the model can be very simple and gradually becomes more complex when all the effects must be taken into account.

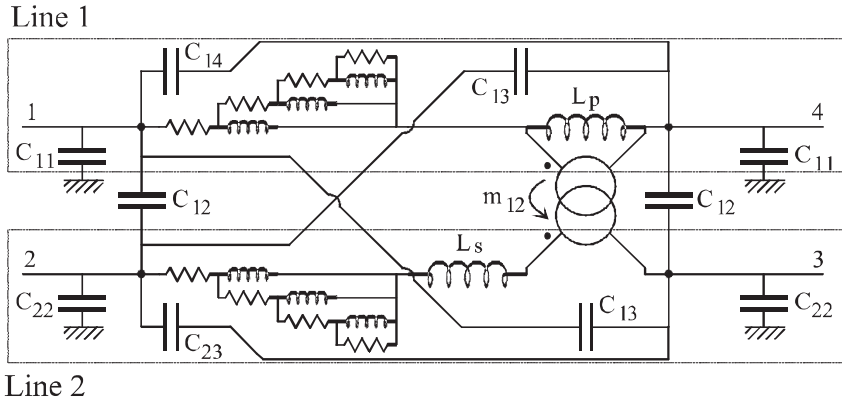


Figure 6.26. *Complete equivalent electrical schematic for two segments of coupled tracks*

However, when the model becomes more complex, the simulating time increases. The method presented for two coupled tracks is generalized to any number of tracks. This generalization is presented in [GAU 00].

6.3.5. *Topological analysis of printed circuit*

The objective of having a CAD tool for the power printed circuit board imposes to automate the tasks to share the design into elementary elements, to verify the existence of couplings between tracks, to identify the parameters of the "circuit" model and finally to make a net list interpretable by the simulator. A software of automatic sharing and analysis of printed circuit is necessary for these tasks. This software must generate, from the geometric description of the tracks on the circuit board, the information necessary for its characterization by the method of thin wires. It also allows the user to specify different levels of modeling for each element obtained during sharing. Finally, it conducts an initial analysis on possible couplings between the various segments of track. Figure 6.27 clarifies this software stage (dotted line) in the overall modeling process.

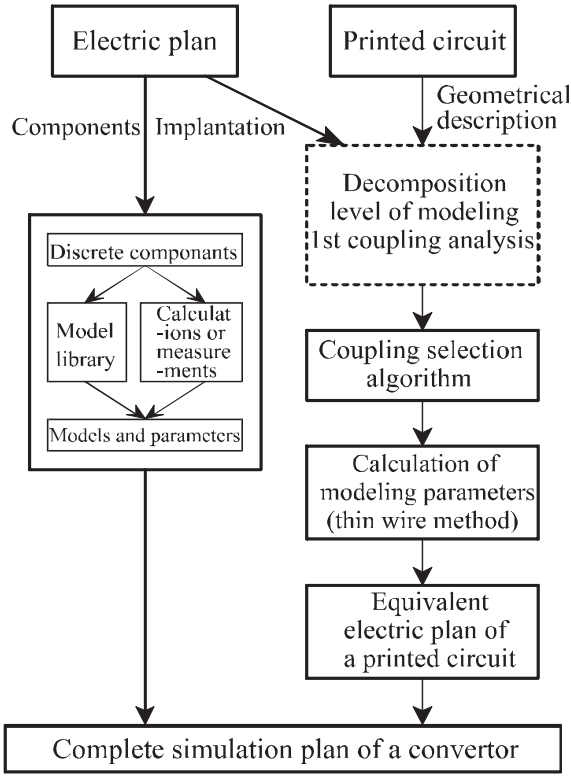


Figure 6.27. *Modeling process*

This algorithm enables the sharing of tracks of a printed circuit for modeling by the thin wire method, as shown in Figure 6.28. The segments of track obtained during the decomposition correspond to the elements of printed circuit board that can be modeled using this method. The nodes correspond to the linking elements between the various segments of track or the junction points with components. The thin track method is not well adapted to model these particular areas which are characterized by low lengths and large surfaces. The geometry of these nodes and parts of linkage with segments of track, however, are fully identified, which allow us to consider their modeling and characterization using a 2D numerical method (finite differences or transmission line matrix) without changing this algorithm. An initial identification of nodes is carried out to allow a simplified characterization (analytical formulations [GAU 00]) in the case of some well-defined configurations.

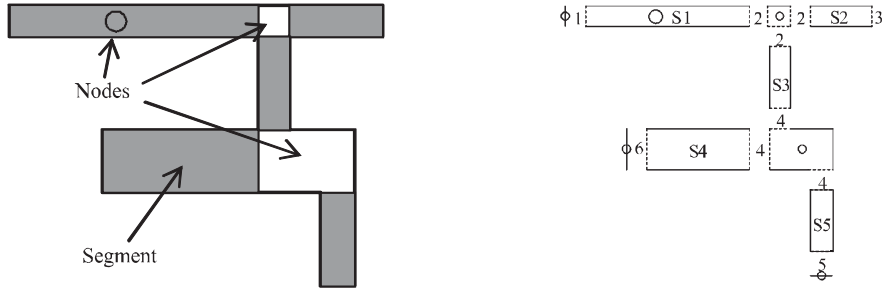


Figure 6.28. *Decomposition of a design in elements treatable by the thin wire method*

Once the stage of decomposition into segments and nodes is completed, the user can perform an initial analysis of the couplings between different segments of track. This analysis allows identifying all segments of track that are parallel with parts face to face (in Figure 6.28 S4 and S1 but not S4 and S2 even if they are parallel). By default, all segments of track are treated in this analysis, but the designer can specify the segments in which we should not use the standard modeling. The determination of significant linkages in turn helps to reduce the total number of linkages to be represented.

Finally, the third and final step is to automatically create a specific library for the printed circuit analyzed, comprising the parameters of models for all segments of track. Using a library can make the link between generic components, used in the electrical diagram, and the degree of complexity of models, as shown in Figure 6.29.

Some generic components have been created under SPICE to model:

– a single track segment (track_1m);

– two coupled track segments (track_2m);

– three coupled track segments (track_3m).

Different libraries are generated automatically depending on the degree of complexity required:

– level 1: R-L model with inductive coupling;

– level 2: R-L-C model with inductive and capacitive coupling;

– level 3: R-L-C model with inductive and capacitive coupling, and skin effect (4 cells).

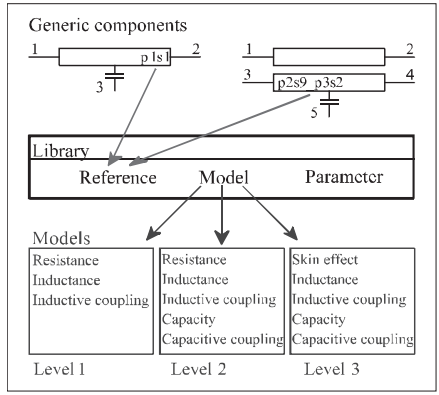


Figure 6.29. *Links between components, models and parameters*

We can consider an extension of this approach to a multi-layer printed circuit: successively applying the previous method to the different layers, which can allow identifying segments of rectangular track. The couplings are treated the same way as for a simple face circuit, parallel segments of track with part face to face are identified during an initial topology analysis.

6.3.6. *Experimental applications*

6.3.6.1. *Analysis of printed wiring*

This section illustrates, using an example, the principles and methods of modeling printed circuit developed here. The device under study is a half bridge of an inverter with MOSFET transistors, powered by 150 V and with switching at 20 kHz. It is represented in Figure 6.30 with its mono-layer printed circuit wiring.

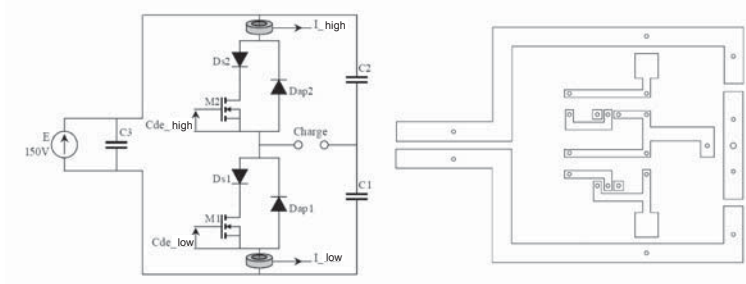
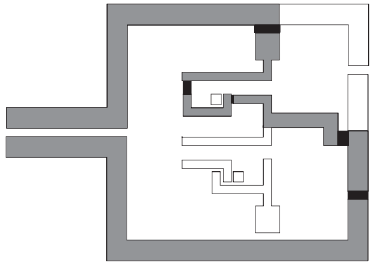


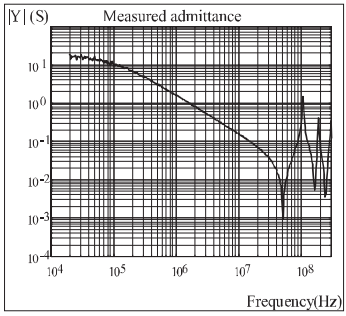
Figure 6.30. *Converter and its printed circuit board*

The analysis of a printed circuit takes place in 5 stages.

	Step	Result
1	Decomposition of printed circuit	All track segments and nodes
2	Study of couplings	list of couplings
3	Calculation of electric characteristics	Admittance matrices Y
4	Calculation of equivalent models	Model parameters
5	Generation of the SPICE library	Library for all elements of the printed circuit board

After applying the method, an impedance measure of the design is performed to validate the simulation. Figure 6.31 presents these results in an indicated wiring configuration.





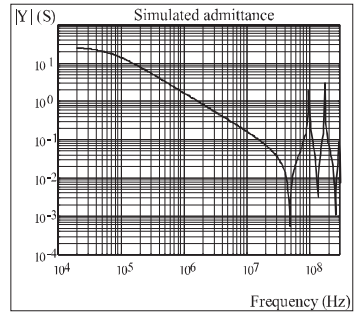


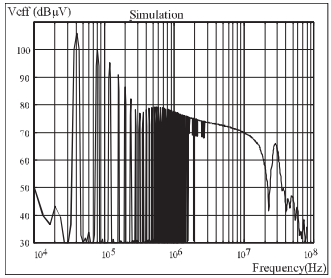
Figure 6.31. *Printed circuit board located 11.5 mm from the ground plane*

You can find a correct representation of the impedance of the circuit up to several hundred MHz. The interest of this analytical method is to easily vary a parameter, for example, the height of a printed circuit compared to the ground plane. The simulation shows in this case a decrease of inductances and an increase in parasitic capacitances with the ground plane. The designer may assume the consequences in terms of EMC (current leakages by common mode capacitance) or operation of converter (voltage surge), compared to a specification. It is thus possible to quickly optimize the wiring using some simulations.

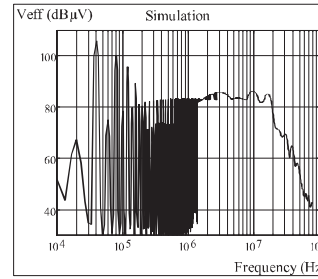
6.3.6.2. *Influence of wiring on conducted disturbances*

Having the complete wiring model, it is then possible to simulate its influence in terms of electromagnetic compatibility by comparing an ideal situation (wiring with no impedance) and the actual situation induced by different types of wiring. The study was conducted in Figure 6.32 where the influence of printed wiring is represented on the spectrum of conducted disturbances. These are measured on the Line Impedance Stabilizer Network (LISN) connected at the input of the converter. The simulation reproduces the measurement configuration.

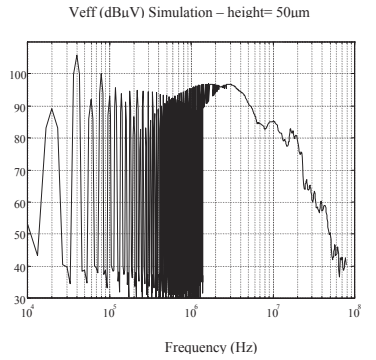
In the simulation corresponding to Figure 6.32a, only the imperfections of semiconductors and passive components were taken into account. In Figure 6.32b the wiring model was added. It is located 11.5 mm above the ground plane, a classic value for printed circuit boards. The case of Figure 6.32c corresponds to a type of IMS wiring where the height compared to the ground plane is 50 μm. There is a marked increase over the ideal case and over the case of a printed circuit board. The comparison of simulations clearly shows the influence of wiring on the electromagnetic signature of the converter. It is dominant in the range of 1-30 MHz and already sensitive a decade before. Finally, Figure 6.33 presents measurements on the actual converter in the configuration of simulation b. There is a good fit with the simulation results, which validate the methodology. We should note that, according to the level of detail used for simulation, the time to calculate can be long, especially if we introduce skin effect models and multiple couplings. Also, in a CAD oriented simulation, the time to calculate can be long, especially if we introduce skin effect models and multiple linkages. Also, in a CAD oriented simulation, the designer must begin the simulation by using low-level models to determine the weight of any particular parameter on EMC or electrical performance of his device. The complex model is then reserved for the final stage of the calculation.



a) ideal wiring, real components



b) height in relation to ground plane: 11.5 mm



c) height in relation to ground plane: 50 µm

Figure 6.32. *Study of the influence of wiring on the spectrum of conducted disturbances by simulation*

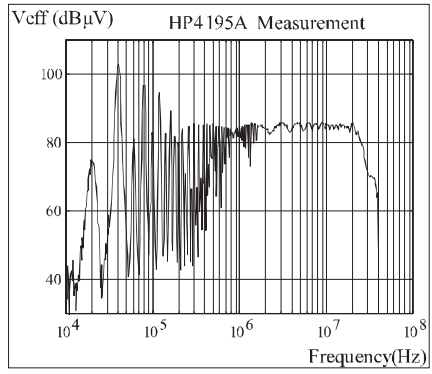


Figure 6.33. *Spectrum of conducted disturbances*

6.3.7. *Conclusion on the simulation of printed circuit*

These sections have shown that the printed wiring used for power electronics, whether traditional (epoxy) or on substrates of IMS type or DCB type for hybrid modules, can be simulated with a satisfactory accuracy and calculation time for a CAD design by a mono-dimensional transmission line method.

All types of printed conductors (multi-layer, variable width, etc.) can be simulated using this method with a sufficient accuracy up to 100 MHz. Some configurations, however, require a 2D modeling, this work is currently underway.

6.4. Towards a better understanding of massive interconnections

In this chapter, we will try to show some examples of power interconnection with their own specificities. We will focus in this section on the design of interconnections according to the criteria of power electronics, that we have already highlighted in the previous sections. Of course, these models can then be completed for EMC. Our intention here is to give examples that can be used in a certain way as guide lines for design. Of course, some proposed solutions are not necessarily original, and have already been developed by engineers of strong powers in the field of induction heating. We will try to illustrate the particularities of each family of interconnections showing orders of magnitude to be expected, and the simplifying assumptions that can be made according to the specificity of each and according to the accuracy that is expected. This accuracy is not always easy to determine, as we will show in section 6.5.

The interconnections in power electronics, except bonding, are mostly and quite exclusively, made of rectangular cross-section conductors. In the same way, but less systematically, conductors are parallel to each other or perpendicular, which greatly simplifies the representation of models of a complete structure (zero coupling between perpendicular conductors). Thus, first studies of quite general scope can be made, and only after this will we see the impact of the specificities of each type of interconnection according the geometrical dimensions and geometrical shapes encountered.

6.4.1. *General considerations*

In this section, we first of all want to illustrate the general trends regarding the evolution of the inductive impact of conductors, based on their geometric dimensions. Most connections used (printed circuit board, IMS, bus bars, massive

bars, etc.) have rectangular cross-sections that make possible to apply the following general trends.

6.4.1.1. *Change in partial inductance depending on the geometry of the straight section of the conductor*

Figure 6.34 highlights the change in inductive impact of a conductor according to its section. In this example, the length of the conductor is 50 cm and the cross-section of the conductor is changed, taking as constant the surface equal to 4 cm^2.

It should be noted that more the conductor is thin and large, the less inductive it is. This makes it very obvious which geometric shape of sections must be chosen to minimize the inductance of a path. The square section gives an idea of the inductance of a round wire whose transverse section is an equivalent surface.

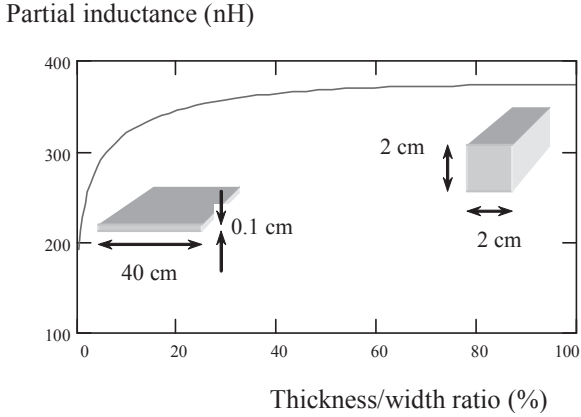


Figure 6.34. *Evolution of the partial inductance with the geometry of the section*

6.4.1.2. *Change in partial inductance depending on the surface of the straight section of the conductor*

The second concept that is as important as the previous one is to have an idea of the change of partial inductance of a conductor depending on the surface of its cross-section.

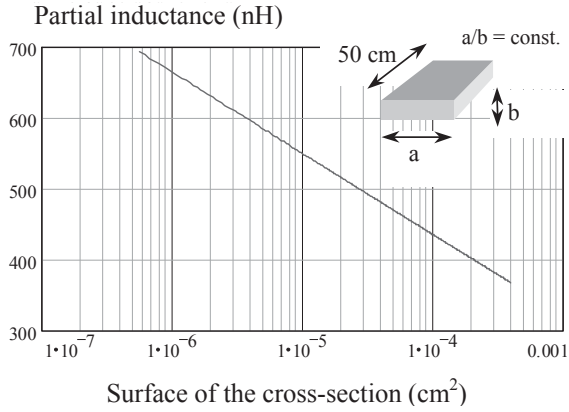


Figure 6.35. *Evolution of the partial inductance depending on the surface of the cross-section keeping constant ratio width over thickness*

Even if the first criterion for choosing a cross-section is thermal, the chart contained in Figure 6.35 shows that the partial inductance of a conductor is very much reduced when the amount of copper used increases.

More specifically, we can observe on the curve in Figure 6.35 that the evolution is linear if a logarithmic scale is used for the surface value. It may be recalled that the expression of the partial inductance shows on denominator the surface of the conductor. It is therefore normal to find this type of variation. The user can then easily extrapolate the curve to solve his problem.

6.4.1.3. *Change in partial inductance depending on the length and section of conductor*

In the following illustration, we want to overcome stereotypes which consider it is sufficient to say that one meter of conductor has an inductance of 1 μH (order of magnitude is however useful in some simple cases). Given the expected performance of interconnections in power electronics (often less than 100 nH), there was no question of use of such magnitudes, legitimate only in the case of wiring several tens of meters separating electrical assemblies. We take this opportunity to recall that the partial inductance is not a linear concept and that, therefore, inductance of a 2 meter conductor is not twice the inductance of one meter. The partial inductance takes into account the fact that the length of the conductor is finite and this concept does not, therefore, makes the assumption of TEM mode (transverse electro-magnetic field).

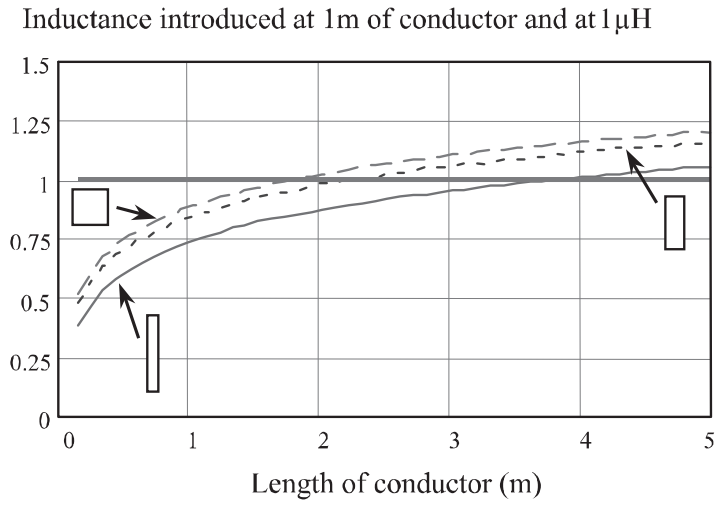


Figure 6.36. *Dependency of inductance of a conductor with the length and the section*

The graph in Figure 6.36 shows this considering conductors whose cross-sections are different (from the flatter to the extreme case of a square or cylindrical conductor). The partial inductance of a conductor has been calculated taking into account its length, then divided by its length to obtain a per unit length value. This result was then compared to 1 μH to show errors that can be made with this kind of approximation.

As for longitudinal dimensions of less than 3 m, the "magic" value of designers of 1 μH/m overstates the inductance, while for dimensions greater than 3 m, it underestimates. Moreover, this distance depends on the section of conductors. The thinner and wider this section, the more this changeover distance increases.

6.4.1.4. *Change in partial inductance depending on the frequency*

Traditionally, we consider that the inductance of a circuit can be broken into two parts. One is the magnetic energy contained in the volume of the conductor. This is called internal inductance and depends on its geometry. The other part is called external inductance, which is defined by the flow embraced by the current loop. It depends on the shape of the loop but also that of conductors. The total inductance of a circuit is the sum of these two inductances. In high frequency, current tends to spread to the periphery of the conductor (skin effect); internal inductance therefore tends to zero when the frequency tends towards infinity.

We can illustrate these remarks by the school case which consists of a cylindrical wire infinitely long with radius a. The internal low-frequency inductance expressed per unit of length is: $\frac{Li}{l} = \frac{\mu_o}{8 \cdot \pi}$.

For any wire, whatever its diameter, this is a low frequency internal inductance of 50 nH/m.

High frequency redistribution of current in the conductor is performed with the same cylindrical symmetry as with low frequency (Figure 6.37), if the conductor is not subject to any external influence; external inductance of the circuit made by cylindrical conductors does not vary.

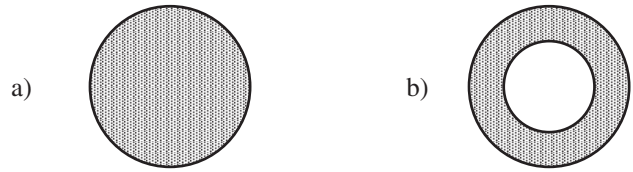


Figure 6.37. *Current density of a cylindrical conductor far away from other conductor:. a) low frequency; b) high frequency*

In cases where another wire (back of the loop for example) is considered close to the conductor, high frequency redistribution of current looses its symmetry and external inductor is amended (Figure 6.38).

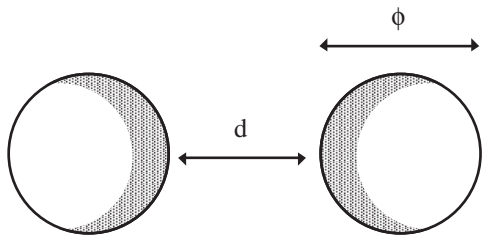


Figure 6.38. *Current density of a cylindrical conductor: influence of the back conductor in high frequency (d of same order of magnitude than Φ)*

Figure 6.39 shows in the case of a loop of rectangular shape (perimeter 50 cm) made of round wire that the change of inductance with frequency is indeed 50 nH/m, because there is no significant proximity effect (10 cm - 15 cm) between conductors.

Where two conductors of the loop are close (24.5 cm - 0.5 cm), the decrease of inductance with frequency is higher.

The external inductor has therefore been amended by the presence of the return conductor.

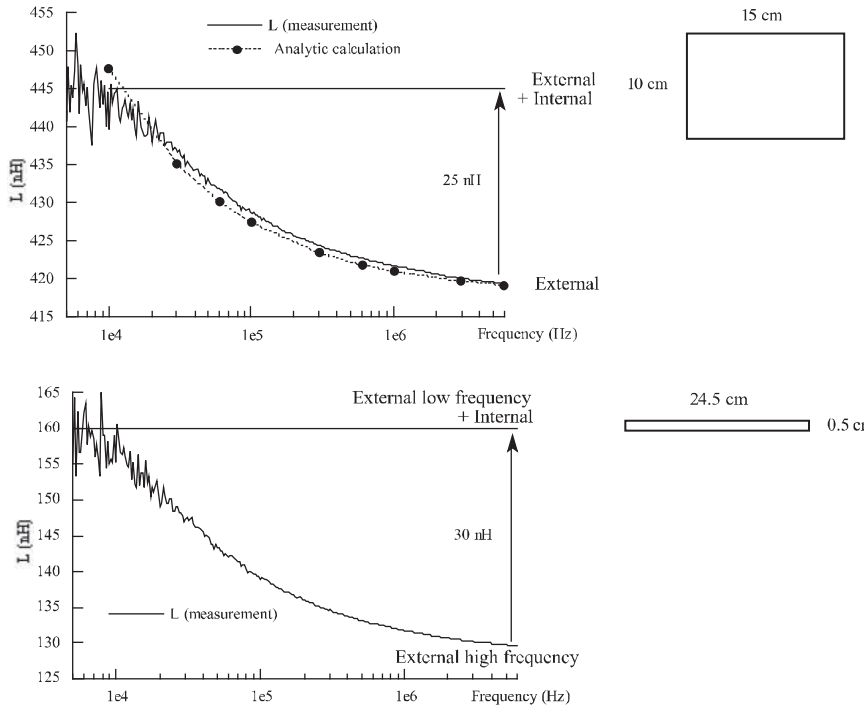


Figure 6.39. *Change of internal and external inductances depending on the frequency*

For conductors of rectangular section, internal inductance becomes negligible if one dimension is very low compared to the other, as shown in Table 6.2. The variation of inductance with frequency in the case of thin ribbons (printed circuit or plates) must therefore be attributed to the external inductance.

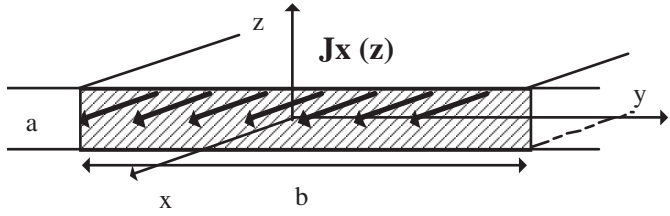


Figure 6.40. *Flat current in a conductor of very low thickness*

a (mm)	b (mm)	a/b	R (mΩ/m) 1 MHz	Li (nH/m) 1 Hz	Li (nH/m) 1 MHz
0.0035	12.5	0.0028	61.2	0.6	0.6
0.0661	6.61	0.0100	63.4	2.0	2.0
0.15	2.9	0.0520	74.6	9.3	7.1
0.21	2.1	0.1000	86.6	16.3	10.4
0.33	1.32	0.2500	111.5	31.0	14.2
0.47	0.94	0.5000	123.4	43.0	15.7
0.66	0.66	1.0000	128.4	48.3	16.3
r = 0.373		–	120.8	50.0	17.5

Table 6.2. *Simulations with "finite elements" for a constant surface ab (R low frequency = 39 mΩ). Also case of wire with given radius r*

It is interesting to note that for the printed circuit board traditionally used in power electronics, 210 µm thick, where it is common to encounter tracks of 1 cm wide, the value of the internal inductance will be lower than 4.4 nH/m. For power boards, where the total length of connections does not exceed 20 cm, internal inductance does not exceed the nanohenry. The wires of circular or square sections have a neighbor behavior.

6.4.2. *The printed circuit board or the isolated metal substrate (IMS)*

The effect of a ground plane located below a track is well known to reduce the inductance of a loop of electrical circuit, whether the plane is electrically connected or not to the rest of the assembly.

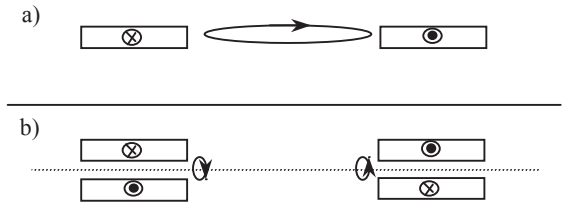


Figure 6.41. *Change of the inductance of a loop by introducing a ground plane*

Indeed, if we consider a loop (Figure 6.41a), composed of a conductor and return back, the embraced surface can therefore become consistent, inductance that results is therefore high. Now (Figure 6.41b), put a ground plane below the conductors. The theorem of images leads us to replace the ground plane by a loop travelled by the same currents in the opposite direction. Soon, it appears that there are compensation flows between a conductor and its image. This way, there is no longer a big loop which radiates but two extremely flat loops (twice the spacing between the conductor and the ground plane), which constitute inductance of the original loop. It is therefore easy to see that the inductance is greatly reduced (Figure 6.42).

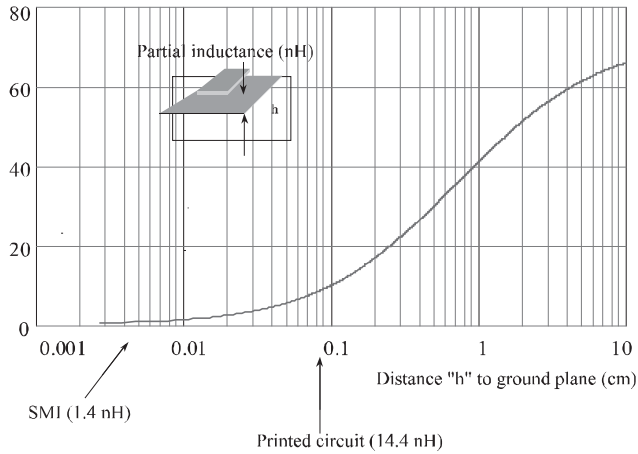


Figure 6.42. *Increase of partial inductance of a conductor with the remoteness of the ground plane*

In terms of application in power electronics, the IMS uses this feature perfectly which leads us to obtain tracks whose partial inductance rarely exceeds 10 nH. The

voltage surge at the opening of semiconductor components are therefore not to be feared with this type of technology, provided the appropriate packages are used.

6.4.3. *Massive conductors*

In the applications of very high power (more than a few megawatts), or more exactly when the current reaches very large values (more than 1,000 Amps), connections with massive conductors are used. It is necessary to be able to connect in parallel converters, and several constraints of mechanical congestion lead us to use such interconnections. It is faster and more convenient to make the connection between two pieces using massive conductors than studying a bus bar which has to answer very specific criteria for partial discharge, etc. This method of connection is widely used in power electronics at industrial frequency (bridge rectifiers for electrolysis, manufacture of aluminum, etc.) or simply in electrical engineering (bars for transformer supply, etc.). In these cases, the intrinsic value of loop inductance is not important but the perfect knowledge of inductance wiring is predominant in the correct distribution of currents between devices in parallel.

The way to reduce inductance of the loop is to maximize face to face surfaces and increase the conductor section (Figure 6.43). However, we must be aware that we cannot change this inductance significantly.

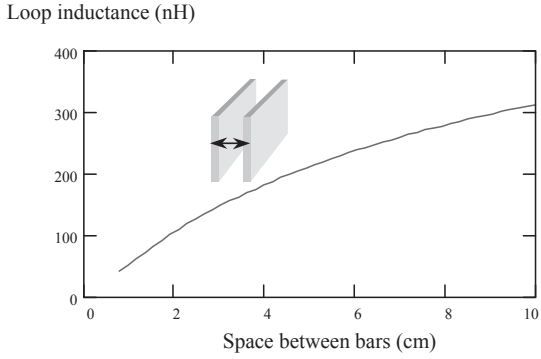


Figure 6.43. *Evolution of the partial inductance of a loop made of go and return massive conductors, depending on their distance*

6.4.4. *Bus bars*

The bus bars are sandwiches of copper and insulating materials pressed and glued. The extreme proximity of conductors increases the partial mutual inductance

which comes to subtract the partial inductance of each bar. This explains perfectly how we can obtain through this process little inductive wiring.

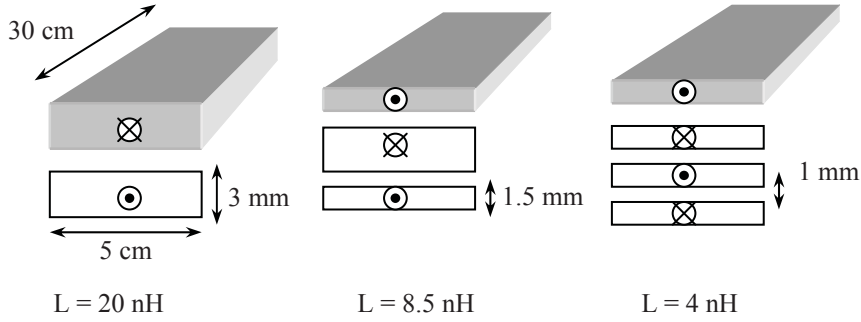


Figure 6.44. *Some ideas to win more nH! (at constant copper volume)*

Nevertheless, the idea to compensate the magnetic flux created in copper at the closest by interspersing plates of way and return flow, as shown in Figure 6.44, shows that it is possible to earn a few nanohenrys but this stacking increases slightly the sizes of the device and especially leads to a much more expensive component. It should be noted that the dielectric layers are all of the same thickness and that the current densities are the same in all conductors.

The weakness of the bus bars lies in the problems of partial discharges which often take place in the corners that can present this type of interconnection.

6.5. Experimental validations

The more frequent use of modeling as an "*a priori*" design tool, requires many validations on realistic configurations. In the case where the device exists, it is sometimes possible to make characterizations of interconnections in the actual operating configuration of the device or, at least, in a configuration extremely close. However, in general, the measure of interconnections remains delicate, mainly because the measured values are, fortunately, particularly low. It is not always easy to close the loop to be measured by a foreign connection to the device and with less impedance than it.

Two large families of measurements are possible in a practical way to achieve the evaluation of interconnections [CLA 96]. The offline measures, themselves separated into several categories, are:

– Measures of impedances with specific devices (impedance measurement bridge for example). This technique is interesting because it gives the value of the impedance according to the frequency. In order to form a loop, the connection under test may be closed either by a short circuit (not always easy to achieve and sometimes with significant impedance) or by decoupling capacitors, which themselves, if they can be exactly of the same value, exist in the final assembly.

– Measures by reflectometry (time or frequency), for example, vector analyzers or temporal reflectometry (TdR). The main drawback of these methods is the low accuracy when the impedance to be measured is far away form characteristic impedance of measuring apparatus (50 Ω most often). As a result, very low impedances due to the connections will not be determined with precision, except at very high frequency. Now, this is the inductive behavior, visible at rather low frequency, which is important for a power electronics designer (forecast of voltage surges).

– Measures by resonance: either with the decoupling capacitors used in the application or possibly with others. We must of course know exactly their values. It determines the tuning frequency of the system (actual impedance at that frequency), which leads to the value of inductance sought.

– Measures making the ratio V/(di/dt). In an "off line" approach, di/dt is injected by an external generator. Note that it is sometimes possible to move the voltage sensor throughout the connection to assess the inductive contribution of each piece. Take care at this stage that the voltage which is measured is expressed by $V = L\frac{di}{dt} + \sum_{i \neq j}^{j} M_{ij} \frac{di_j}{dt}$. Thus, in the general case, we will not have access to the value of inductance unless we can effectively ignore the mutual couplings Mij.

– "Online" measures, fairly close to the actual operating conditions of the device or even in operation, can also be used.

The ratio V/(di/dt), during commutation, can of course give useful information on inductances, concerning mutual inductances some precautions can be taken as previously said. One of the important applications is the determination of housing inductance of a controlled IGBT-type semiconductor.

We can also think of an oscillatory discharge. Decoupling capacitors are charged generally under a reduced voltage and the short circuit is realized using the semiconductors of the power structure. Given the orders of magnitude, it is not always easy to obtain an oscillating wave discharge which remains easy to identify.

The identification results are not always very accurate and can present an error by the fact that the short circuit created by semiconductors is not instantaneous.

The necessary conclusion is that none of these measures is really better than the others. Our preference is still for measures on impedances bridge which has the advantage of allowing a display of the impedance depending on the frequency. In addition, some of the mistakes are more easily quantifiable in terms of abacuses provided by the manufacturer. The only large inaccuracies are due to the possible short circuits used to close the loop.

Figure 6.45 shows the comparison between model and measurement, on inductance between the emitter and collector of an IGBT in its package. This validation of the overall modeling of inductive package confirms the interest of the approach.

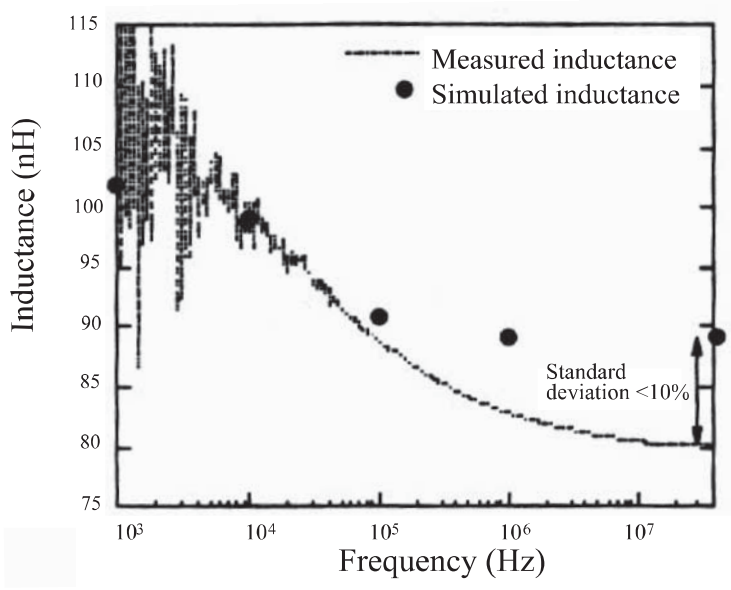


Figure 6.45. *Comparison simulation – measure on an IGBT package (old generation)*

For more complex connections requiring a 2D approach, the example of Figure 6.46 is that of a three-phase UPS installed to supply AC machines. In addition to InCa3D modeling, we conducted several measurements using different methods that we summarized in Table 6.4. It may be noted that it is also necessary to model any piece belonging to the switching cell which is also involved in the measurement. In particular, it was necessary to characterize internal inductances of semiconductor packages. The measurement does not allow us to differentiate the

inductive importance of the bus bar in the total loop. We had to remove the simulation results of the package from the measure to obtain the results presented.

	Resonance	Short circuit Impedance bridge	Oscillating Discharge	Simulation
Inductance	20.5 nH	13.5 nH	9 nH	9 nH

Table 6.3. *Values of inductance of the commutation cell: measures and simulation*

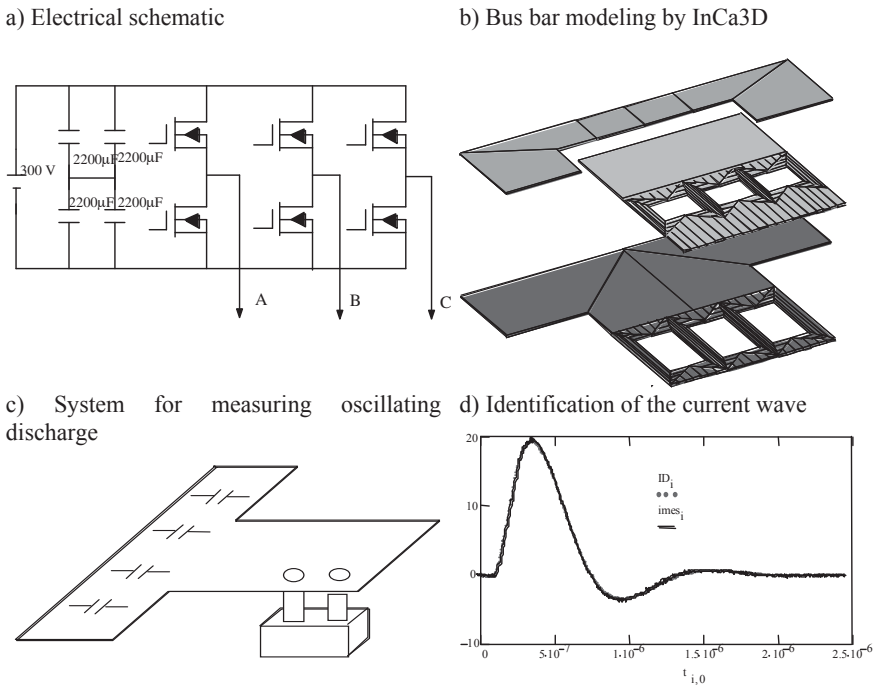


Figure 6.46. *Example of measurement for characterization of a bus bar*

As a conclusion, we can see that there is already a great dispersion of results depending on methods of measurement and it would be very hasty to conclude that oscillatory discharge is the best method because it gives the nearest result from simulation, itself subject to errors.

6.6. Using these models

In this section, we will show how to use electrical equivalent schematics provided by modeling. Indeed, it is possible to obtain global values and/or local values according to the post-treatment involved. Of course, depending on the studied structure, the analyses will be more or less easy and will lead to more or less data processing.

6.6.1. *Determination of equivalent impedance*

As modeling provides an electrical equivalent schematic including localized constants made of resistances, inductances and mutual inductances, then it is logical to try to reduce this figure to determine the impedance of all or part of the structure. This impedance then serves to make a study of waveforms of the power electronics structure. However sometimes the complexity of the structure is such that one impedance is not enough to show all the connections of the device. The scale model is then more complicated and we will see in the following section that the calculation methods are not the same as for the simple case of a single impedance (section 6.5.1.1).

6.6.1.1. *Between two points*

In this section, we will give two examples illustrating the approach to determine the impedance of the commutation loop. The 1D assumption was used in the first instance and the 2D assumption for the second (for the connections grid).

Here is a brief recap of the different steps of the approach [CLA 97]:

1. entering the geometry of the device from plans by the graphic pre-processor InCa3D;

2. evaluation with InCa3D of all parasitic elements, inductances and mutual couplings;

3. post-treatment with InCa3D to possibly reduce the equivalent electrical diagram;

4. simulation of the electric model thus obtained. The system which now needs to be simulated is of reasonable complexity (at least the switching cell composed of a voltage source, an inductance, a diode and a switch). We can of course simulate more complex systems that are more complete and thus allow any change in geometry.

6.6.1.1.1. First example

The first example that we present is modeling a switching cell in the form of a Power Block package.

Figure 6.47 shows the modeling process of the switch function:

– capture of geometry (Figure 6.47c);

– modeling with an electrical equivalent schematic with localized constants (Figure 6.47d). Here, as conductors are mostly linear and, more important, as it is possible to make assumptions on the path of current lines, a 1D mesh was adopted;

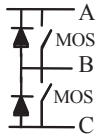
– – reducing the electrical equivalent circuit given by PEEC modeling. This is to determine the equivalent impedance from two points of the switching cell (Figure 6.47e). Note that this impedance results in the serial and parallel combination of different portions which, remember, are all linked to each other, which requires some developments of matrix calculus [ROU 94] and the introduction of the frequency;

– simulation and obtaining global waveforms of module (Figure 6.47f). In the final simulation schematic, mesh inductance includes therefore the case that we just evaluated through InCa3D, the inductance of voltage source (decoupling capacitors) and the one of the bus bar between the capacitors and the Power Block.

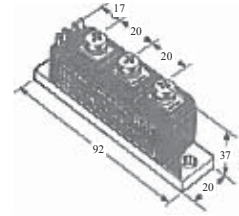
6.6.1.1.2. Second example

Now let us take a much more complex example in the form of an interconnection bus bar with a large and flat geometry, which needs to make a 2D mesh (Figure 6.48) as described in section 6.3.2. As a result of the InCa3D modeling, a network of resistors and inductances are all coupled, but difficult to use directly by the power electronics engineer.

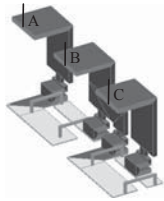
a) Electric function of the studied Power Block



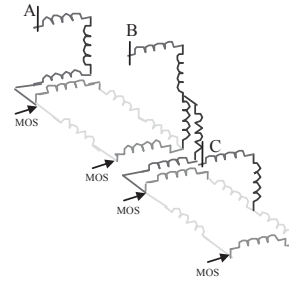
b) External aspect of the Power Block



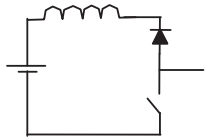
c) Geometry of internal connexions described on InCa3D



d) Electric schematic from modeling on InCa3D (all are coupled inductors)



e) Generic diagram for simulation



f) Accurate simulation obtained from accurate model of connection and component: opening a MOSFET

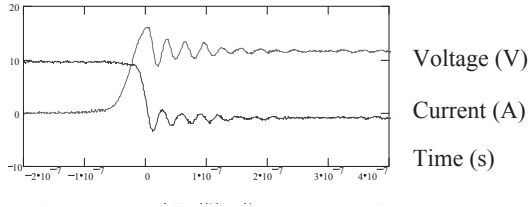


Figure 6.47. *Approach for extracting a cell switching: from capture of geometry to simulation*

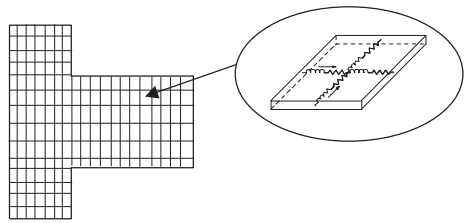


Figure 6.48. *2D mesh of plates of the bus bar*

The application of a network theory is not justified in this example. We are looking only for the impedance between two points, input and output, of the bus bar.

A simple harmonic analysis with SPICE, for example (Figure 6.48), gives the evolution of the electrical characteristics of the bus bar depending on the frequency (Figure 6.49).

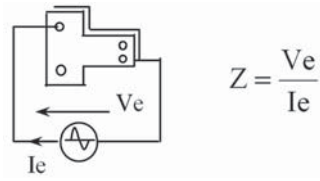


Figure 6.49. *Impedance of bus bar depending on the frequency*

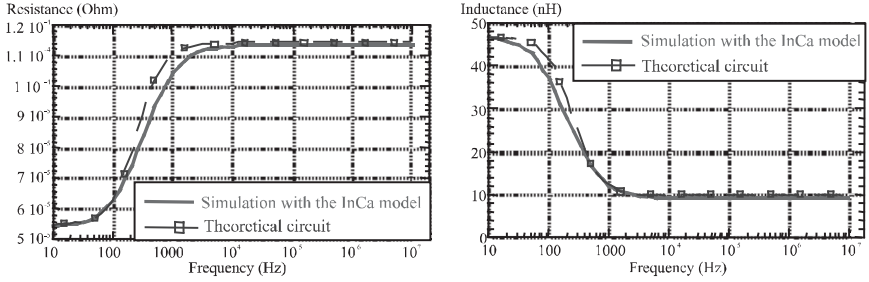


Figure 6.50. *Frequency characteristics by using a SPICE simulation, device measurement*

More specifically, Figure 6.50 shows the evolution of resistance and inductance depending on the frequency. These values are only valid for a limited range of frequencies, in agreement with the spatial meshing of the bus bar (Figure 6.48). This phenomenon appears especially on the resistance whose value reached a limit around 10 kHz, while in practice it continues to grow with frequency. Variations of inductance are much smaller amplitudes, which does not allow us to distinguish the limit of correct digitization, and enables us to accept good values of inductance obtained for frequencies above 10 kHz.

From these impedance curves, it is possible to deduce a simplified electrical equivalent circuit involving only two resistances and two non-coupled inductances (Figure 6.51). Clearly, it is easier to make a temporal simulation with this last model than with the one obtained by InCa3D simulation which contains several hundred coupled LR series circuits. A finer model, but also more costly in simulation time, can be made by adding parallel LR cells in series.

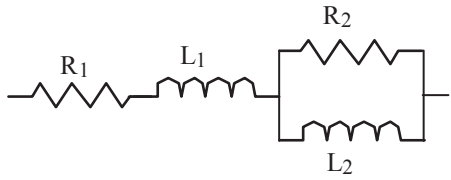


Figure 6.51. *Simplified electrical equivalent schematic whose characteristics are independent of the frequency*

In the case of 2D modeled structures, post-treatment can be very long and costly in terms of memory space, because the electrical pattern that has to be reduced to a simple impedance can be very dense.

In many cases, a power electronics designer will be tempted to use an approach to solving circuit equations based on the method of potential nodes, as proposed by the SPICE software. However, the latter is not well suited to many inductors, and analysis of the circuit related to the current is better suited as we will show in what follows.

6.6.1.1.3. Analysis of electrical circuit [PIE 99]

After applying the PEEC method, we obtain a matrix system $\mathbf{U} = \mathbf{Z} \cdot \mathbf{I}$ which dimension equals the number of subdivisions. At the end of this circuit analysis a reduced relationship $u = z \cdot i$ must be obtained, where z is the equivalent impedance between two points of the structure, which will allow us to study the overall behavior of the system.

We have chosen a systematic topological analysis, which uses Kirchhoff's laws (law of nodes and law of mesh). These laws do not depend on the type of components (active or passive, linear or non-linear), but only on the directed graph of the circuit. For example, Figure 6.52 shows an electric circuit and its associated graph.

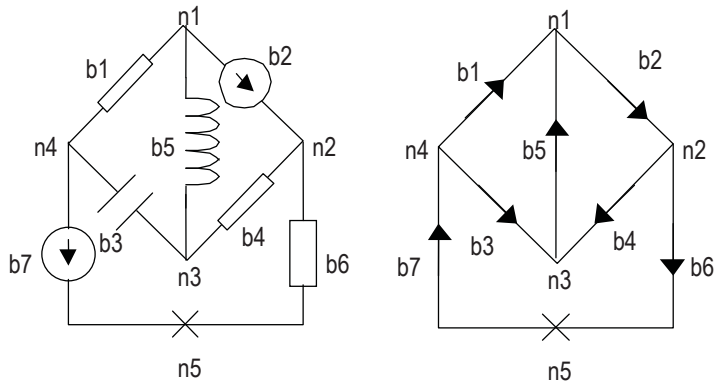


Figure 6.52. *Electrical circuit and its associated graph*

The electrical circuit is composed of 7 components that are represented in the associated graph with directed segments. The points of connections, 5 on this example, which are terminals of components, are topological nodes. Oriented segments in the direction of reference are called branches.

The mesh concept is also defined. It is a closed loop, oriented in a reference direction, which follows the branches, such a way the branches are travelled at least once. For our example, there are 6 meshes as we can see in Figure 6.53. However, it appears that these meshes are redundant and do not form an independent system. It will therefore be required to find the number of independent meshes for describing the system.

Broadly speaking, if we consider the graph of an electrical circuit with b branches and n nodes, the system of independent integral and differential equations for the calculation of voltages and currents in components includes $n - 1$ equations for nodes and $b - n + 1$ equations for meshes. It should be noted that the number of branches b is greater than the number n of nodes, which may be a factor in the choice of the calculation algorithm.

In the previous case, we must find 3 independent meshes (because b = 7 and n = 5). For the following development, our independent 3 will be meshes m1, m2 and m3.

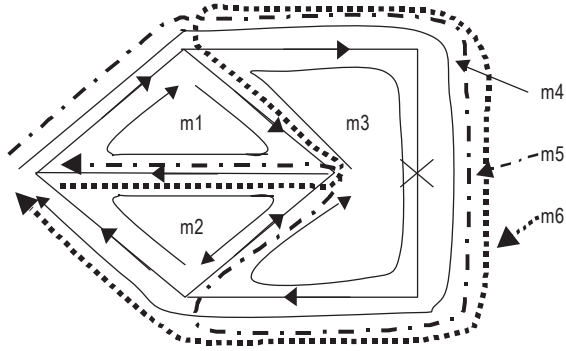


Figure 6.53. *Electrical meshes*

To implement the system of equations to be solved, several well-known values must be introduced. The incidence matrix N, also called the nodes to branches matrix, is defined as follows:

$$\mathbf{N} = \begin{bmatrix} \alpha_{11} & \alpha_{12} & \cdots & \alpha_{1b} \\ \alpha_{21} & \alpha_{22} & \cdots & \alpha_{2b} \\ \vdots & \vdots & \ddots & \vdots \\ \alpha_{n1} & \alpha_{n2} & \cdots & \alpha_{nb} \end{bmatrix} \quad avec \quad \alpha_{ij} = \begin{cases} 1 & \text{, if branch j leaves node i} \\ -1 & \text{, if branch j arrives at node i} \\ 0 & \text{, if branch j is not connected to node i} \end{cases}$$

With this matrix N, we can write the law of nodes: $\mathbf{N} \cdot \mathbf{I} = \mathbf{0}$, with I the vector of branch current, with dimension b.

Matrix N is not regular. To transform it, we need to delete a line and we obtain the reduced incidence matrix N' which is regular. This operation corresponds to the choice of a reference node.

We can always write the relationship: $\mathbf{N}' \cdot \mathbf{I} = \mathbf{0}$

Consider the matrix $\mathbf{M} = \begin{bmatrix} \beta_{11} & \beta_{12} & \cdots & \beta_{1b} \\ \beta_{21} & \beta_{22} & \cdots & \beta_{2b} \\ \vdots & \vdots & \ddots & \vdots \\ \beta_{m1} & \beta_{m2} & \cdots & \beta_{mb} \end{bmatrix}$, with m = b – n +1

and:

$$\beta_{ij} = \begin{cases} 1 & \text{, if branch j belongs to mesh i and they are oriented in the same direction} \\ -1 & \text{, if branch j belongs to mesh i and they are oriented in the opposite direction} \\ 0 & \text{, if branch j does not belong to mesh i} \end{cases}$$

The matrix M will be called in the following matrix mesh-branch.

We can write the mesh law: $\mathbf{M} \cdot \mathbf{U} = \mathbf{0}$ with U the vector of branch voltages of dimension b.

In the above presentation, we have ignored the components of the circuit. We will take them into account in expressing Ohm's law on each branch. Two dual methods exist.

The branch currents are a function of branch voltages. In systems that we describe, it is always possible to write Ohm's Law:

$$\mathbf{I} = \mathbf{Y} \cdot \mathbf{U}$$

with:

– I: branch currents vector;

– U: branch voltages vector;

– Y: admittances matrix related to the branches.

Vectors I and U are not completely composed of unknown variables. Some ii and uj may be determined by the structure: they are current and voltage sources. In this approach, the unknown is vector U. The current sources will be isolated in a vector I_g. The previous law becomes:

$$\mathbf{I} = \mathbf{Y} \cdot \mathbf{U} + \mathbf{I_g}$$

with I_g the vector of current generators.

To illustrate this, we take the example of Figure 6.53 and we assume that the generators are current generators. Then we have the following terms:

$$\mathbf{I_g} = \begin{bmatrix} 0 & I_1 & 0 & 0 & 0 & 0 & I_2 \end{bmatrix}^t$$

and:

$$\mathbf{Y} = \begin{bmatrix} \frac{1}{R_1} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & jC\omega & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{R_2} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{jL\omega} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{R_3} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

The branch voltages are a function of branch currents.

For this approach, we express Ohm's Law $\mathbf{U} = \mathbf{Z} \cdot \mathbf{I}$, with:

– U: vector of voltage branches;

– I: vector of current branches;

– Z: impedance matrix relative to each branch.

As in the previous case, there may be voltage and current sources.

The unknown here is the current vector I. The voltage sources are encountered in the vector U_g.

We obtain: $\mathbf{U} = \mathbf{Z} \cdot \mathbf{I} + \mathbf{U}_g$

with U_g the vector of voltage generators.

This time, we assume that the generators are voltage generators. Then we have the following terms:

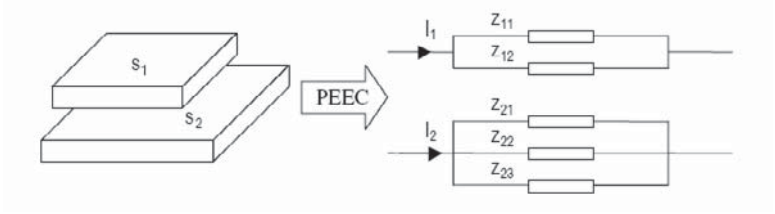
$$\mathbf{U}_g = \begin{bmatrix} 0 & E_1 & 0 & 0 & 0 & 0 & E_2 \end{bmatrix}^t$$

and:

$$\mathbf{Z} = \begin{bmatrix} R_1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{jC\omega} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & R_2 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & jL\omega & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & R_3 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

Once the different values are defined, we will explain later the impact of the two previous approaches. We will explain the reasons of our choice.

To show the principle of the two methods, we will take a simple example: 2 straight bars, which we model in 1D, respectively in 2 and 3 elements in Figure 6.54. Here, the bars were isolated from the converter



with $z_i = r_i + j\ \omega\ l_i$

Figure 6.54. *PEEC modeling*

In this case, we want to assess the electrical equivalent pattern of each bar and the inductive coupling between them. To this end, two fictitious components are added. These can be considered as impedance sensors (Figure 6.55), i.e. devices that measure the equivalent impedance of connections: for the specific case of an impedance only resistive, this is an ohmmeter.

We try to identify elements of the impedance matrix defined as follows:

$$\begin{bmatrix} U_1 \\ U_2 \end{bmatrix} = \begin{bmatrix} Z_1^1 & Z_1^2 \\ Z_2^1 & Z_2^2 \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}, \text{ with } Z_2^1 = Z_1^2 .$$

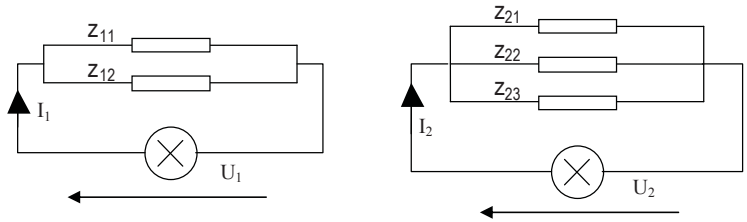


Figure 6.55. *Adopted model*

The associated graph with this electric system is presented in Figure 6.56.

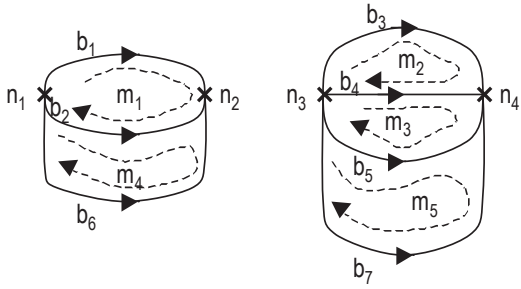


Figure 6.56. *Associated graph*

Starting from this graph, we can define nodes Ni $\left(i \in \{1 \ldots n\}\right)$, branches Bi $\left(i \in \{1 \ldots b\}\right)$ and independent meshes Mi$\left(i \in \{1 \ldots m\}\right)$. The number s of impedance sensors is also defined (here, s = 2). For our example we have n = 4, m = 5 and b = 7.

Note Z the matrix of impedance obtained by modeling with the PEEC method.

$$\mathbf{Z} = \left[\begin{array}{cc:ccc} R_{l_1} + j\omega L_{l_1} & j\omega M_{l_1}^{l_2} & j\omega M_{l_1}^{2_1} & j\omega M_{l_1}^{2_2} & j\omega M_{l_1}^{2_3} \\ j\omega M_{l_1}^{l_2} & R_{l_2} + j\omega L_{l_2} & j\omega M_{l_2}^{2_1} & j\omega M_{l_2}^{2_2} & j\omega M_{l_2}^{2_3} \\ \hdashline j\omega M_{l_1}^{2_1} & j\omega M_{l_2}^{2_1} & R_{2_1} + j\omega L_{2_1} & j\omega M_{2_1}^{2_2} & j\omega M_{2_1}^{2_3} \\ j\omega M_{l_1}^{2_2} & j\omega M_{l_2}^{2_2} & j\omega M_{2_1}^{2_2} & R_{2_2} + j\omega L_{2_2} & j\omega M_{2_2}^{2_3} \\ j\omega M_{l_1}^{2_3} & j\omega M_{l_2}^{2_3} & j\omega M_{2_1}^{2_3} & j\omega M_{2_2}^{2_3} & R_{2_3} + j\omega L_{2_3} \end{array}\right]$$

The notation is as follows:

– $M_{A_i}^{B_j}$ which is the mutual coupling between element i of bar A and element j of bar B;

– R_{A_i} which is the proper resistance of element i of bar A;

– L_{A_i} which is the self inductance of element i of bar A.

Note that $M_{A_i}^{B_j} = M_{B_j}^{A_i}$.

Analysis related to voltages: in this approach, the unknown will be the vector of branch voltages U. We will use the laws concerning the matrix N' of incidences of branches at nodes and Ohm's Law expressed through admittances. The impedance sensors are, for this method, current generators. We have:

$$\mathbf{I}_g = [0 \quad 0 \quad 0 \quad 0 \quad 0 \quad I_1 \quad I_2]^t \quad \text{and} \quad \mathbf{Y} = \begin{bmatrix} & & 0 \\ & \mathbf{Z}^{-1} & \vdots \\ & & \vdots \\ 0 & \cdots & 0 \end{bmatrix} \begin{matrix} \\ \\ b-s \\ \\ s \end{matrix}$$

$$\begin{matrix} & b-s & s \end{matrix}$$

The combination of the previous equations gives: $\mathbf{N}' \cdot \mathbf{Y} \cdot \mathbf{U} + \mathbf{N}' \cdot \mathbf{I}_g = \mathbf{0}$.

If we choose a node reference by independent system, we can define the vector V of potential differences between each node and its associated reference node. V is size (n - s) and is linked to the vector U of voltage with the equation: $\mathbf{U} = \mathbf{N}'^t \cdot \mathbf{V}$.

In our case, we took nodes n_2 and n_4 as nodes of reference.

We obtain equality as follows:

$$\mathbf{N}' \cdot \mathbf{Y} \cdot \mathbf{N}'^t \cdot \mathbf{V} + \mathbf{N}' \cdot \mathbf{I}_g = \mathbf{0}$$

To simplify the equation, we note: $\mathbf{Y}_n = \mathbf{N}' \cdot \mathbf{Y} \cdot \mathbf{N}'^t$.

For the example studied, we have:

$$\mathbf{Y}_n = \begin{bmatrix} Y_{1_1}^{1_1} + Y_{1_2}^{1_2} + 2Y_{1_2}^{1_1} & Y_{1_2}^{1_1} + Y_{2_2}^{1_1} + Y_{2_3}^{1_1} + Y_{2_1}^{1_2} + Y_{2_2}^{1_2} + Y_{2_3}^{1_2} \\ Y_{2_1}^{1_1} + Y_{2_2}^{1_1} + Y_{2_3}^{1_1} + Y_{2_1}^{1_2} + Y_{2_2}^{1_2} + Y_{2_3}^{1_2} & Y_{2_1}^{2_1} + Y_{2_2}^{2_2} + Y_{2_3}^{2_3} + 2Y_{2_2}^{2_1} + 2Y_{2_3}^{2_2} + 2Y_{2_3}^{2_1} \end{bmatrix}$$

with $Y_{A_i}^{B_j}$ the admittance between element i of the bar A and element j of the bar B.

The equation becomes: $\mathbf{Y}_n \cdot \mathbf{V} + \mathbf{N}' \cdot \mathbf{I}_g = \mathbf{0}$.

In order to obtain the potential of current generators, and hence find the equivalent impedance of each system, as well as mutual between two systems, we must reverse Yn.

Thus, we express V as follows: $\mathbf{V} = -\mathbf{Y}_n^{-1} \cdot \mathbf{N}' \cdot \mathbf{I}_g$.

For mesh voltages, we obtain the equation:

$$\mathbf{U} = -\mathbf{N}'^t \cdot \mathbf{Y}_n^{-1} \cdot \mathbf{N}' \cdot \mathbf{I}_g$$

We call Zb the matrix $-\mathbf{N}'^t \cdot \mathbf{Y}_n^{-1} \cdot \mathbf{N}'$.

Recall that the vector Ig is a vector composed mainly of 0, except s last terms that are equal to the currents set by the impedance sensors. The matrix Z_b can be broken down as follows:

$$\mathbf{Z_b} = \left[\begin{array}{c:c} & \\ \hdashline & \mathbf{Z_c} \end{array}\right] \begin{matrix} \updownarrow b-s \\ \updownarrow s \end{matrix}$$

$$\leftrightarrow b-s \quad \leftrightarrow s$$

Written in expanded form:

$$\begin{bmatrix} u_{1_1} \\ u_{1_2} \\ u_{2_1} \\ u_{2_2} \\ u_{2_3} \\ \hdashline U_1 \\ U_2 \end{bmatrix} = \left[\begin{array}{ccccc:c} & & & & & \\ & & & & & \\ & & & & & \\ & & & & & \\ & & & & & \\ \hdashline & & & & & \mathbf{Z_c} \end{array}\right] \cdot \begin{bmatrix} i_{1_1} \\ i_{1_2} \\ i_{2_1} \\ i_{2_2} \\ i_{2_3} \\ \hdashline I_1 \\ I_2 \end{bmatrix}$$

Z_c is the matrix of impedances sought in the case of a reduction.

In summary, Z_c is obtained as a result of several operations:

– inversion of the matrix Z (dimension (b - s) x (b - s));

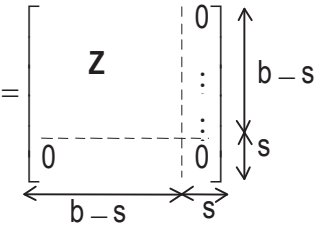
– inversion of the matrix Y_n (dimension (n - s) x (n - s)).

Before discussing the advantages and disadvantages of this method, we will first present its dual analysis.

Analysis related to currents: for this analysis, the unknowns are the mesh currents. Thus, we will use the laws associated with the mesh-branch matrix M and Ohm's law expressed with the impedance matrix. This time, impedance sensors are voltage generators.

U_g and Z involved in this case are as follows:

$$\mathbf{U}_g = [0 \quad 0 \quad 0 \quad 0 \quad 0 \quad E_1 \quad E_2] \quad \text{and} \quad \mathbf{Z} = \begin{bmatrix} & & 0 \\ & \mathbf{Z} & \vdots \\ 0 & & 0 \end{bmatrix}$$



The mesh-branch matrix M is defined so that it is regular. Recall the dimensions of the matrix are m × b.

$$\mathbf{M} = \begin{bmatrix} 1 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & -1 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & -1 \end{bmatrix}$$

Similarly, we define the vector composed of Im mesh currents (dimension m × 1).

This was for our example: $U=\begin{bmatrix} u_{1_1} & u_{1_2} & u_{2_1} & u_{2_2} & u_{2_3} & U_1 & U_2 \end{bmatrix}^t$.

$$\mathbf{I} = \begin{bmatrix} i_{1_1} & i_{1_2} & i_{2_1} & i_{2_2} & i_{2_3} & I_1 & I_2 \end{bmatrix}^t$$

$$\mathbf{I}_m = \begin{bmatrix} i_{m_1} & i_{m_2} & i_{m_3} & i_{m_4} & i_{m_5} \end{bmatrix}^t$$

Vector Im is calculated from vector I expressing the law of meshes, using the matrix M, which gives the equation: $\mathbf{I} = \mathbf{M}^t \cdot \mathbf{I}_m$.

The combination of the previous equations gives:

$$\mathbf{M} \cdot \mathbf{Z} \cdot \mathbf{M}^t \cdot \mathbf{I}_m + \mathbf{M} \cdot \mathbf{U}_g = \mathbf{0}$$

For simplicity, we note: $\mathbf{Z}_m = \mathbf{M} \cdot \mathbf{Z} \cdot \mathbf{M}^t$ and $\mathbf{U}_m = \mathbf{M} \cdot \mathbf{U}_g$.

Here,

$$\mathbf{Z}_m = \begin{bmatrix} Z_{1_1} - 2Z_{1_1}^{1_2} + Z_{1_2} & Z_{1_1}^{2_1} - Z_{1_2}^{2_1} - Z_{1_1}^{2_2} + Z_{1_2}^{2_2} & Z_{1_1}^{2_2} - Z_{1_2}^{2_2} - Z_{1_1}^{2_3} + Z_{1_2}^{2_3} & Z_{1_1}^{1_2} - Z_{1_2} & Z_{1_1}^{2_3} - Z_{1_2}^{2_3} \\ Z_{1_1}^{2_1} - Z_{1_2}^{2_1} - Z_{1_1}^{2_2} + Z_{1_2}^{2_2} & Z_{2_1} + Z_{2_2} - 2Z_{2_1}^{2_2} & Z_{2_1}^{2_2} + Z_{2_2}^{2_3} - Z_{2_1}^{2_3} - Z_{1_1} & Z_{1_2}^{2_1} - Z_{1_2}^{2_2} & Z_{2_1}^{2_3} - Z_{2_2}^{2_3} \\ Z_{1_1}^{2_2} - Z_{1_2}^{2_2} - Z_{1_1}^{2_3} + Z_{1_2}^{2_3} & Z_{2_1}^{2_2} + Z_{2_2}^{2_3} - Z_{2_1}^{2_3} - Z_{1_1} & Z_{2_2} - 2Z_{2_2}^{2_2} + Z_{2_3} & Z_{1_2}^{2_2} - Z_{1_1}^{2_3} & Z_{2_2}^{2_3} - Z_{2_3} \\ Z_{1_1}^{1_2} - Z_{1_2} & Z_{1_2}^{2_1} - Z_{1_2}^{2_2} & Z_{1_2}^{2_2} - Z_{1_1}^{2_3} & Z_{1_2} & Z_{1_2}^{2_3} \\ Z_{1_1}^{2_3} - Z_{1_2}^{2_3} & Z_{2_1}^{2_3} - Z_{2_2}^{2_3} & Z_{2_2}^{2_3} - Z_{2_3} & Z_{1_2}^{2_3} & Z_{2_3} \end{bmatrix}$$

and $\mathbf{U}_m = \begin{bmatrix} 0 & 0 & 0 & -E_1 & -E_2 \end{bmatrix}$.

The introduction of the two previous equations leads to:

$$\mathbf{Z}_m \cdot \mathbf{I}_m + \mathbf{U}_m = \mathbf{0}$$

Calculations allow us to write both following equalities:

$$i_{m_4} = i_{1_1} + i_{1_2} = I_1$$

$$i_{m_5} = i_{2_1} + i_{2_2} + i_{2_3} = I_2$$

As we wish to express equivalent impedances between two points, we have to find out Z_c such that:

$$\mathbf{Z}_c \cdot \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} E_1 \\ E_2 \end{bmatrix}$$

Obtaining Z_c will be carried out using a method able to make partially triangular the matrix Z_m, for example, the Pivot Gauss method. This allows the equality:

$$\begin{bmatrix} 1 & x & x & x & x \\ 0 & 1 & x & x & x \\ 0 & 0 & 1 & x & x \\ 0 & 0 & 0 & Z_{c11} & Z_{c12} \\ 0 & 0 & 0 & Z_{c21} & Z_{c22} \end{bmatrix} \cdot \begin{bmatrix} i_{m1} \\ i_{m2} \\ i_{m3} \\ i_{m4} \\ i_{m5} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ E_1 \\ E_2 \end{bmatrix}$$

We can extract the matrix Z_c and therefore equivalent impedances of each independent system.

In summary, the result is obtained using a partial triangular matrix Z_m (dimension $m \times n$).

Comparison of the two analyses: at the beginning of the analysis in relation to the voltages, the analytical aspect is lost while we keep it up until we make the triangular matrix operation in the analysis related to the currents.

To compare the two types of analysis previously exposed, we will recall in a summary table the characteristics of each method.

analysis in relation to the voltages	**analysis in relation to the currents**
Inversion of two matrices: $(b-s)\times(b-s)$ $(n-s)\times(n-s)$	Triangular operation on a matrix $m\times m$

Table 6.4. *Operations for current and voltage methods*

We can conclude that in terms of calculation cost, the analysis related to voltages is much more expensive than that related to currents and the two inversions as the

voltage method looses the advantage of analytical formulae used by the PEEC modeling.

For these two main reasons, the method of analysis related to the currents seems the most appropriate. We keep together as far as possible analytical formulae, which will be an advantage during a phase of structural optimization of converters of power electronics. We can now present the complete modeling synopsis (Figure 6.57).

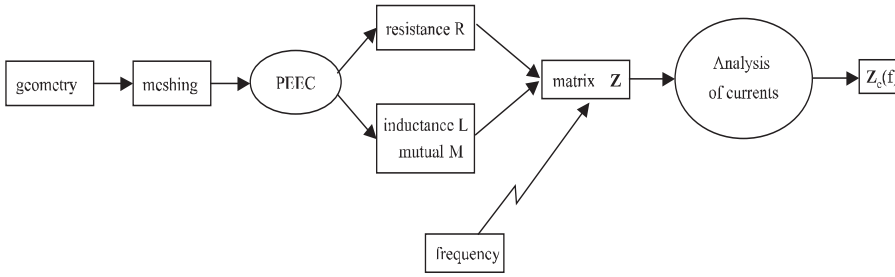


Figure 6.57. *Overview of modeling*

Until the construction of matrix Z, the frequency is not involved in modeling. Now, for the reduction of the schematic, we cannot avoid the influence of frequency. Thus, if we want to perform a frequency analysis, it will require as many partial triangular operations as number of calculation points desired.

If we take the example above, the obtained matrix Z_c includes extra-diagonal terms whose real part is low compared to the real part of the diagonal terms. This is often negligible, so that we can easily translate this result as an electric schematic with localized constants, able to be introduced in a simulation software to obtain the electrical waveforms over all the studied structure.

However in some cases, the real part will not be neglected. We will not be able then to find a representation with located elements in this impedance matrix. In fact, there are no simple components to translate a resistive coupling.

This justifies the following section in which a particular method for dealing with this problem and therefore which generalizes the translation of the equivalent impedance into an electric schematic is detailed.

6.6.1.2. *Between several points*

To be able to model these connections, two problems must be solved: a 2D meshing must be available to treat plates more or less complex, including notches, holes… At the moment, the two softwares, InCa3D – developed by G2elab – [CLA 96] and Fasthenry, software from MIT [KAM 94], are based on a uniform discretization of plates, which generates a large number of components. It must therefore be able to reduce equivalent schematics from this 2D approach, what has been explained in the preceding section.

The connections such as "plates" are not used between two points only. Therefore, an electrical equivalent schematic must be proposed to reflect these multiple accesses. This is the second aspect that will be discussed during this section.

Let us imagine a bus bar simply defined by Figure 6.58, with 8 connection points (4 per plate). According to the mode of presentation of the PEEC method, the most natural schematic will consist of 6 coupled impedances; indeed, on each plate, a point can be chosen as an arbitrary reference, and it radiates from this point to the others. It was therefore required to determine each of these impedances, using InCa. The problem occurs on the terms of couplings between these impedances: terms of resistive couplings appear in addition to conventional mutual inductances.

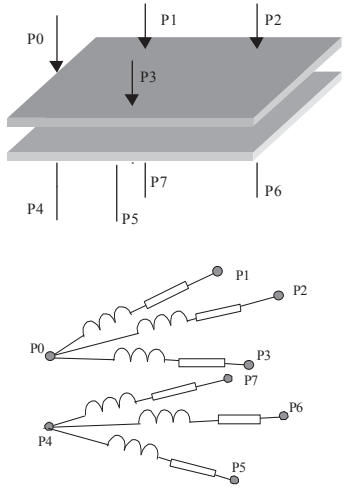


Figure 6.58. *Simple bus bar illustrating the problem of multiple accesses. A possible representation involving resistive coupling (for clarity, no coupling is represented)*

The physical interpretation within a single plate is rather direct: if a supply is applied between two points, a voltage will be induced between two others, which will be both inductive and resistive (current lines may go between these two points and cause a voltage drop). Regarding the case of two separate plates, the explanation lies in the eddy currents induced in the other plate when two points of the first one are supplied. Then there is indeed a common, and therefore resistive, voltage drop.

The "mutual resistance" does not exist in the electrical simulators, any more than the complex elements (complex mutual inductance to represent the resistive linkages): another representation must be adopted if we want to reflect all the phenomena involved in the bus bar.

Using a standard "transformer" approach (because it is here a transformer with n windings), it is possible to move from this "star of branches" representation to another type of "polygonal" representation, using decoupled elements. The method is described below.

We detail the approach on the example in Figure 6.58 using a formalism close to that of the preceding section.

Let us call ni the number of nodes on the plate number i. Here there are two plates; they will be $(n_1 - 1 + n_2 - 1)$ coupled inductances, i.e. $n_L = n_1 - 1 + n_2 - 1$ self-inductances ($n_L = 6$) and $n_M = \sum_{i=1}^{n_L - 1} i = \frac{n_L (n_L - 1)}{2}$ mutual inductances ($nM = 15$). The PEEC approach is to establish an impedance matrix Z, complex square matrix of dimension $(n_1 - 1 + n_2 - 1)$ and thus symmetric with $n_L + n_M$ complex elements. Z connects branch currents to branch voltages referenced in points P0 to plate 1 and P4 to plate 2.

$$\begin{bmatrix} V_1 \\ V_2 \\ \\ \\ V_{n_1-1+n_2-1} \end{bmatrix} = [Z] \begin{bmatrix} I_1 \\ I_2 \\ \\ \\ I_{n_1-1+n_2-1} \end{bmatrix}$$

To ensure the change of base and go to "polygonal" representation we need a single reference linking these two points. We find then $n_L = 6$ branch voltages, referenced to the common node "P0P4".

The chosen representation is then to replace the problem of n_L coupled inductances by a system of $n_L + n_M$ decoupled inductances.

The total number of nodes of the problem is then $n = n_1 + n_2 - 1$ ($n = 7$). In addition, we then connect all the nodes 2 by 2 by a non-coupled inductance. We obtain b branches with $b = \sum_{i=1}^{n-1} i = \frac{n(n-1)}{2}$ (b = 21 branches).

Ohm's Law is then written:

$$\begin{bmatrix} U_1 \\ U_2 \\ \\ \\ U_b \end{bmatrix} = [Z_{diag}] \begin{bmatrix} J_1 \\ J_2 \\ \\ \\ J_b \end{bmatrix}$$

where Z_{diag} is the diagonal matrix of dimension b × b containing the items sought.

The only problem is that we have connected the two plates. To find again the necessary galvanic isolation, three perfect couplers of unit ratio are then inserted at terminal points P0P4, P1, P2 and P3, to provide isolated accesses to the equivalent schematic (Figure 6.59).

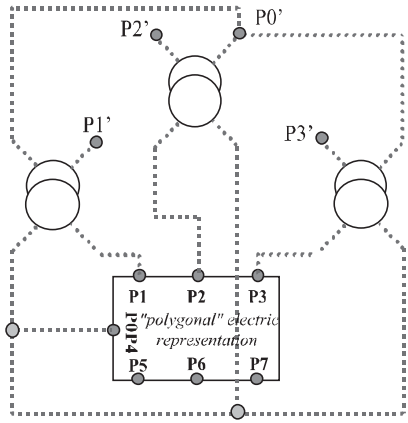


Figure 6.59. *Passage to "polygonal" representation, for example in Figure 6.58 with insulation of the two plates. The access to the model are points P0' to P3', and P5 to P7*

The representation assured, it remains to determine the values of decoupled impedances. The passage is not easy, insofar as we must identify $n_L + n_M$ terms of a matrix $(n_1 - 1 + n_2 - 1) \times (n_1 - 1 + n_2 - 1)$ with b diagonal elements from the "polygonal" matrix processed this way.

Anyone who has already made the passage, for a two windings transformer, from a two coupled inductance representation to the classic "leakage inductance, magnetizing inductance and ratio of transformation" version knows that these calculations, without being complicated, are not immediate as it is to identify term to term two matrices of different sizes. It is easy to find by matrix projection the coupled impedances from the decoupled elements, but the reverse is a little trickier, and it is precisely this sense of passage that we are attempting [SUA 99].

We are actually looking for a formula for transition from Z to Z_{diag}.

For that we are going to intervene in 2 matrices.

Call P_i the matrix which is linking the outgoing currents I_i $\left(i \in [1\ ;\ n_1 - 1 + n_2 - 1]\right)$ to branch currents J_j $\left(j \in [1\ ;\ b]\right)$ of dimension $((n_1 - 1 + n_2 - 1) \times b)$ and P_v the matrix which is linking branch voltages U_j $\left(j \in [1\ ;\ b]\right)$ to simple voltages V_i $\left(i \in [1\ ;\ n_1 - 1 + n_2 - 1]\right)$ of dimension $(b \times (n_1 - 1 + n_2 - 1))$.

This is:

$$\begin{bmatrix} I_1 \\ I_2 \\ \\ \\ I_{n_1-1+n_2-1} \end{bmatrix} = [P_i] \begin{bmatrix} J_1 \\ J_2 \\ \\ \\ J_b \end{bmatrix} \quad \text{and} \quad \begin{bmatrix} U_1 \\ U_2 \\ \\ \\ U_b \end{bmatrix} = [P_v] \begin{bmatrix} V_1 \\ V_2 \\ \\ \\ V_{n_1-1+n_2-1} \end{bmatrix}$$

If we call $Y = Z^{-1}$ the admittance matrix of the schematic with coupled inductances, then we obtain the following relationship: $Y = P_i\, Y_{diag}\, P_v$.

As Y is symmetric, then $tP_v = P_i$.

In addition, by reversing Y_{diag}, we obtain the matrix Z_{diag} desired. The problem is that we have to identify Y_{diag} term by term.

The matrix P_i will be completed using the node law. The matrix P_v is derived from the law of meshes or from the relationship linking it to P_i.

If there is yj $(j \in [1\ ;\ b])$ the terms of Y_{diag}, then it is easy to obtain an expression of the terms of Y, with certain conventions to take when describing the two schematics (coupled inductances or polygon).

Conventions:

– the common node is noted 0 and output points are noted 1 to $(n_1 - 1 + n_2 - 1)$;

– currents I_i correspond to the currents flowing from these points;

– branches and hence branch currents will be numbered as follows:

- branch 1 from node 0 to node 1, branch 2 from node 0 to node 2… , branch $(n_1 - 1 + n_2 - 1)$ from node 0 to node $(n_1 - 1 + n_2 - 1)$,

- branch $(n_1 - 1 + n_2)$ from node 1 to node 2…

With these conventions, we can fill in Y as follows:

Upon its diagonal, we put the terms y_1 to $yn_1 - 1 + n_2 - 1$. They then complete the superior triangular part line by line with the following terms (from $yn_1 - 1 + n_2 - 1$ to y_b) by adding a minus sign. Then we complete the diagonal by subtracting from the already written term the sum of other terms of the line.

$$[Y] = \begin{bmatrix} y_1 + \sum_{j=n}^{2n-3} y_j & -y_n & \cdots & \cdots & -y_{2n-3} \\ -y_n & y_2 + y_n + \sum_{j=2n-2}^{3n-6} y_j & & & -y_{3n-6} \\ . & & & & \\ . & & & & \\ . & & & & -y_b \\ -y_{2n-3} & -y_{3n-6} & & -y_b & y_{n-1} + \sum_{j=0}^{n-2} y_{2n-2-(2j+1)} \end{bmatrix}$$

Identification is then easy between Y obtained by reversing Z and Y_{diag}. It is sufficient to begin with the extra-diagonal terms of Y (terms of Y_{diag} directly with reverse sign) and then, by simple addition, complete by using the diagonal terms of Y. A simple inversion of Y_{diag} gives us the matrix Z_{diag} sought.

Note that certain terms may be negative. This is not a problem: any impedance measured between each of the outside access points is always positive, which is the only physical constraint.

There follows an example of processing for a schematic with 3 coupled inductances.

Let us see what this approach gives in the case of a schematic with 3 coupled inductances. This gives a polygon schematic with 6 branches (Figure 6.60).

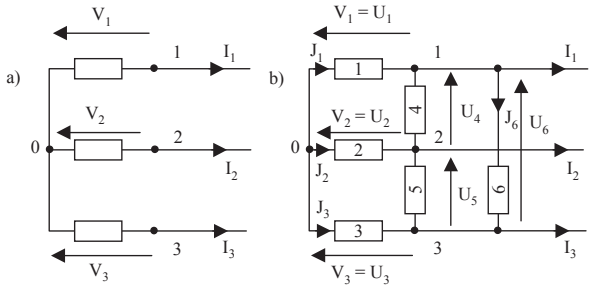


Figure 6.60. *a) Schematic with 3 coupled inductances, b) "polygonal" representation*

We obtain:

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & -1 & -1 & 0 \\ 0 & 1 & 0 & 1 & 0 & -1 \\ 0 & 0 & 1 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} J_1 \\ J_2 \\ J_3 \\ J_4 \\ J_5 \\ J_6 \end{bmatrix} \text{ and } \begin{bmatrix} U_1 \\ U_2 \\ U_3 \\ U_4 \\ U_5 \\ U_6 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \\ -1 & 1 & 0 \\ -1 & 0 & 1 \\ 0 & -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}$$

let us write:

$$[Y_{diag}] = \begin{bmatrix} a & 0 & 0 & 0 & 0 & 0 \\ 0 & b & 0 & 0 & 0 & 0 \\ 0 & 0 & c & 0 & 0 & 0 \\ 0 & 0 & 0 & d & 0 & 0 \\ 0 & 0 & 0 & 0 & e & 0 \\ 0 & 0 & 0 & 0 & 0 & f \end{bmatrix}$$

then:

$$[Y] = \begin{bmatrix} a+d+e & -d & -e \\ -d & b+d+f & -f \\ -e & -f & c+e+f \end{bmatrix}$$

Then we identify the terms of Y with the result of the inversion of Z to know the 6 unknown variables of the polygon schematic.

As a conclusion, if we know how to model the plates, the method described above provides an equivalent schematic able to be simulated by a circuit software of the PSPICE type. Figure 6.61 shows the result of this approach on a relatively complex industrial example: a bus bar connecting 5 IGBT and 6 decoupling capacitors. The bus bar presents 24 accesses (with plus and minus entries of continuous bus). The result thus includes 506 impedances (506 R and 506 L) $\left(C_{23}^{2}\right)$ and 12 couplers, and may be represented as an hyper block in the PSPICE simulator. Note that an approach neglecting resistive coupling leads to a schematic including 22 coupled inductances (which corresponds to a description that would win 506 – 22 = 484 resistances, since mutual inductances remain).

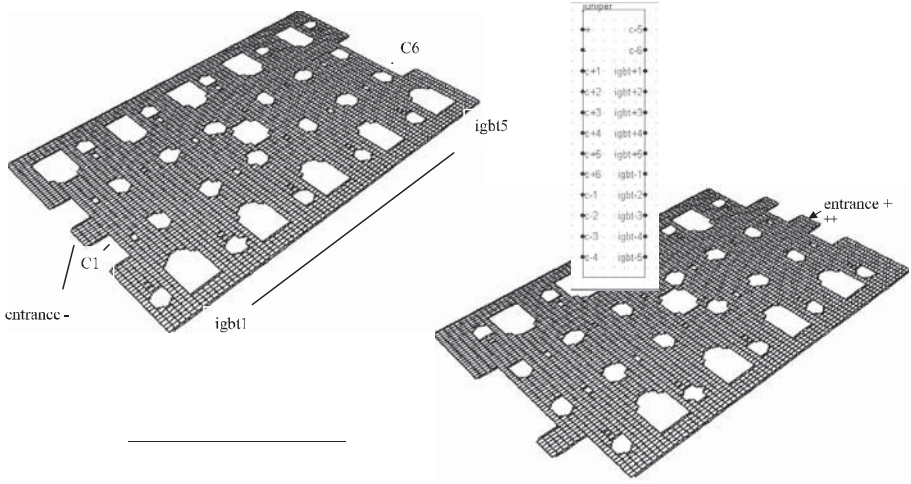


Figure 6.61. *Industrial bus bar involving 5 IGBT and 6 decoupling capacitors, and corresponding PSPICE hyper block*

6.6.2. *Other applications: towards thermal analysis and electrodynamic efforts computation*

The exploitation of equivalent schematics from a PEEC modeling is not the "simple" research of equivalent impedances. Even if these are very useful in order to later carry out an analysis of waveforms of the overall structure, they are not sufficient in the context of a more comprehensive analysis i.e. taking into account other parts of physics.

Indeed, if we refer to the equations in section 6.6.1.2, a simple resolution of the linear system using a direct method such as Choleski gives us access to different currents of meshes. Remember that these currents are actually currents in subdivisions of the mesh device. This resolution is certainly costly in computing time if the mesh is dense but if it is well defined, i.e. adapted to the frequency range of operation of the structure, it must be performed only one time. Thus, if we obtain the current in each of the subdivisions then the current density is immediate with the modeling approach we have adopted.

If we take the example of the bus bar of the Figure 6.61, it is also possible to obtain the distribution of current in each cell after the subdivision of plates (Figure 6.62) when a sine wave generator of voltage with variable frequency is

connected to some ends. It is perhaps interesting to note the current evolution in different parts of the conductor depending on the frequency.

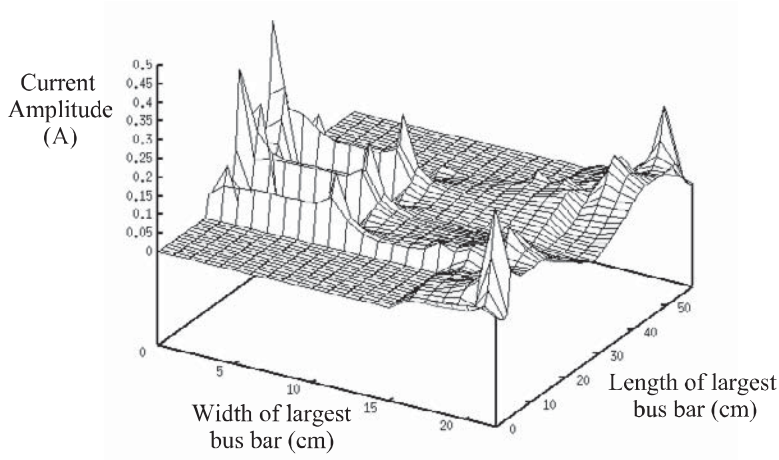


Figure 6.62. *Distribution of current in one of the plates of the bus bar at 10 kHz*

This analysis can be very interesting when we do not know *a priori* the path of current plates lines in a bus bar. Thus we can make geometrical changes (holes, notches, etc.) in conductors to change the routes of power currents and access a more satisfactory operation in terms of power electronics. Gradually, we see the emergence of qualitative design rules that will improve designs which are so far based on essentially empirical approaches.

Moreover, in the case of three-phase structures, the magnitude of the current in each phase is not enough, we must also take into account the phase shift to really evaluate the distribution of current in connections.

The following example shows a three-phase bus bar, each phase consisting of six parallel bars (Figure 6.63), and distribution of the current density in each of them for a given frequency (Figure 6.64) [GUI 00a].

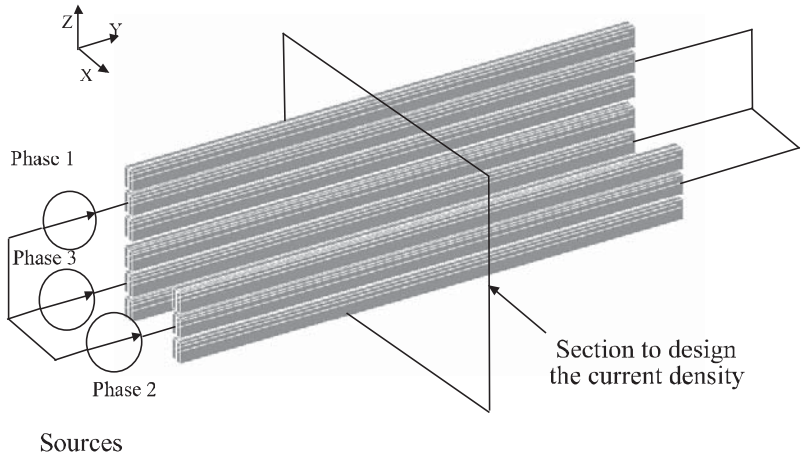


Figure 6.63. *Three-phase structure: set of bars*

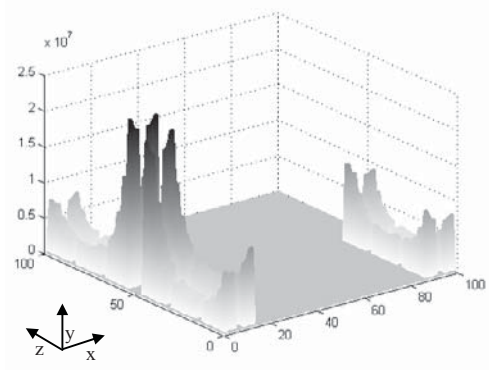


Figure 6.64. *Distribution of current densities in the bars (A/m^2)*

Knowing the current density in conductors is also very useful when we come to other areas of physics which were not previously taken into account in the design phase of the power structures by computer.

6.6.2.1. *Evaluation of losses*

Thus, we can deduce the power dissipated, then it informs us about the thermal aspects of the structure. Already, the display of current densities tells us about the potential hot spots. But now, in order to know the losses, when a three-phase structure is modeled, some currents can be cancelled, making results different from the case of DC operation.

The calculation of the power dissipation is immediate, since we know the current in each mesh subdivision:

$$P_{subdivision} = R_{subdivision} . I_{subdivision}^{2}$$

with:

– $P_{subdivision}$: power dissipated in a subdivision (W);

– $R_{subdivision}$: resistance of a subdivision (Ω);

– $I_{subdivision}$: effective current through a subdivision (A).

Then the sum of all subdivisions gives the total losses of the device.

Note: if the problem is not meshed or inadequately meshed, there will be some mistake on the current, and as the current is high squared, the error is high squared too. It is therefore necessary to treat the mesh correctly, using geometric subdivisions for example, to obtain dissipated powers close to reality.

When losses are calculated using the method previously indicated, it is sufficient to apply the heat equation to determine temperatures at several points. Note that the conduction is easily assessable throughout electrical equivalent models. The convection and radiation are still based on empirical formulations to determine the different constants of the device (coefficients of convection and radiation).

6.6.2.2. *Evaluation of electrodynamic efforts*

6.6.2.2.1. Calculating the induction

Knowing the current in each of the subdivisions, we can calculate the magnetic field B at any point of the device, applying one of the fundamental principles of electromagnetism: the Biot–Savart law. The elementary dB field created by an element d flown by a current I2 at a point M in space (Figure 6.65) is given by the following equation:

$$d\mathbf{B} = \frac{\mu_0 . I_2 . d\ell \times \mathbf{r}}{4.\pi . R^2}$$

with:

– μ_0 permeability of vacuum (= $4\pi 10^{-7}$ H/m);
– r: unitary vector.

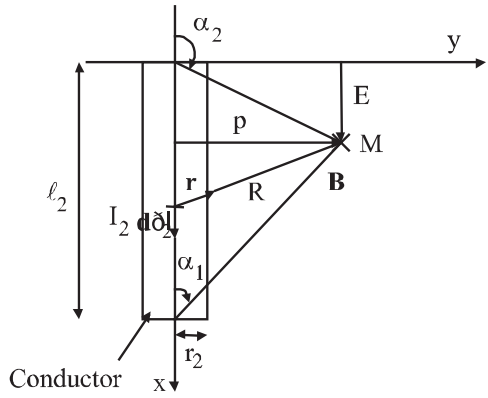


Figure 6.65. *Convention for the calculation of the magnetic field at any point*

This expression gives induction created at M by current element $I_2 d\ell$. This method allows us to calculate the induction created by one or more conductors at all points of space. However, it is possible to observe that when the distance R decreases and tends to 0, induction will move towards infinity. To circumvent this divergence, two cases will be distinguished. The first is obtained when the induction is sought outside of the conductor (for example Figure 6.66, $|p| > r$), the second is obtained when the induction is being sought inside the conductor $|p| \leq r_2$.

In the first case, the expression of B is: $B = \frac{\mu_0 . I_2}{4.\pi . p}\left(\cos(\alpha_1) - \cos(\alpha_2)\right)$.

In the second case, where the induction is being sought inside the conductor, it is necessary not to reflect the entire current flowing through the conductor to avoid the divergence of B which is directly linked to the linear modeling of the wire. For this,

we assume that the current is distributed uniformly in the section of the conductor and that it is circular. It replaces a conductor section most often by a rectangular conductor of the same circular cross-section. After integration, we obtain:

$$B_2 = \frac{\mu_0 . I'_2}{4.\pi.r_2^2} . p.(\cos(\alpha_1) - \cos(\alpha_2))$$

with $I'_2 = J_2 . \pi . p^2$ and $J_2 = \frac{I_2}{\pi . r_2^2}$.

This calculation, immediate when automated, can then obtain the field for the entire device. This may then be useful to take into account the presence of magnetic materials (for example with a finite elements tool) and deduct their impact by superposition.

Validation with a fully digital calculation (finite elements with the Flux3D software) have provided confidence in the previous expressions. An example of such validation is presented Figure 6.66.

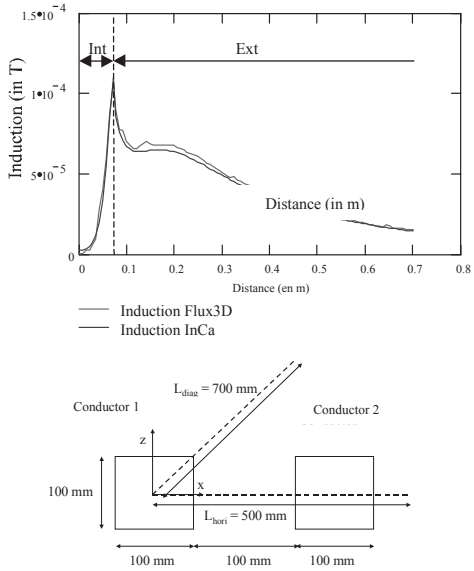


Figure 6.66. *Induction evaluated using the analytical expressions and digitally*

6.6.2.2.2. Calculation of electrodynamics efforts [GUI 00b]

Then the electrodynamics efforts exerted on the plates of a bus bar are immediately deduced, for example under short circuit. Indeed, in this case the destruction of structures occurs (Figure 6.67).

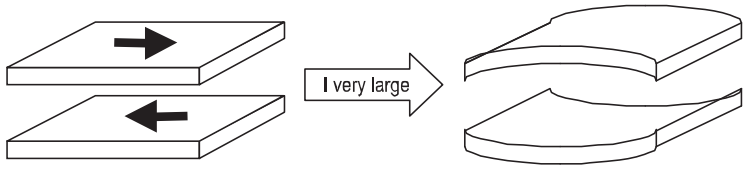


Figure 6.67. *Deformation of bus bars with a very strong current*

Knowing B(M), we can use the Laplace law placed in M, which expresses the variation df of the force exerted on an element d flown by a current I2, immersed in magnetic field B.

To calculate the effort, we use the Laplace law:

$$\mathbf{df} = I_2 \cdot \mathbf{d}\ell \wedge \mathbf{B}$$

Consider the case where currents I1 and I2 are parallel between them, and therefore conductors which carry it too (Figure 6.68). This is the case of the majority of industrial bus bars.

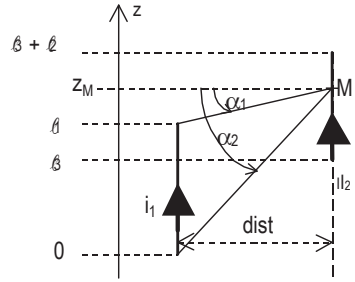


Figure 6.68. *Convention for the calculation of electrodynamics efforts*

After treatment, we obtain an analytical expression which gives the electrodynamics effort between two linear and finished conductors:

$$F = \frac{\mu_o \cdot I_1 \cdot I_2}{4 \cdot \pi \cdot dist} \left[\sqrt{dist^2 + z^2} \right]_{l_3 - l_1, l_3}^{l_3 + l_2, l_3 + l_2 - l_1}$$

with: $\left[f(z) \right]_{z_2, z_4}^{z_1, z_3} = f(z_1) - f(z_2) + f(z_3) - f(z_4)$.

To know effort between two massive conductors, it is required to integrate across the width and the thickness of the conductors the expression above, taking as hypothesis that the current density is uniform in the section of conductors. This calculation has led to very complicated expressions, since primitive forms are elliptical functions.

A question then arises: is it enough to express electrodynamics efforts between two linear conductors in order to know what happens between two massive conductors?

A validation with a numerical calculation showed that it was sufficient to mesh coarsely conductors to take into account the massive behavior of conductors (Figure 6.69), and the overall effort obtained by the sum of the efforts of each mesh is comparable to the effort calculated digitally.

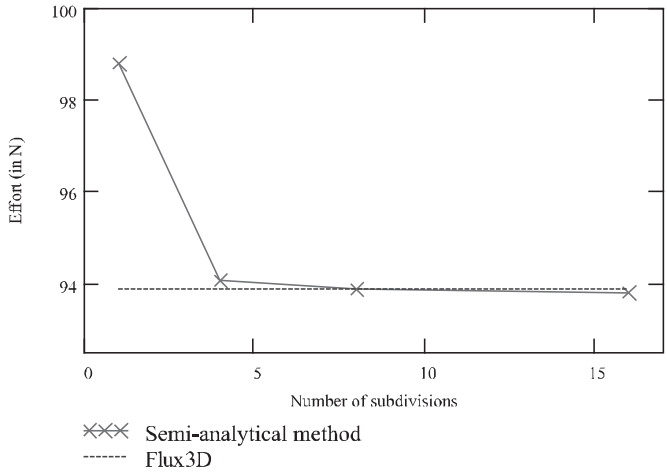


Figure 6.69. *Electrodynamics effort between two massive and parallel conductors*

Similar calculations have been carried out in the case of perpendicular conductors, where we must distinguish between conductors that touch or not. The analytical expression, always in the case of linear conductors, but taking into account a uniform distribution of current in the section, is:

$$F = \frac{\mu_0 . I_1 . I_2}{4.\pi} . \left[\left[\frac{x}{r_1^2} . \sqrt{p^2 + y^2 + x^2} \right]_{l_3}^{r_1} {}_{(y)}^{E-l_1} {}_{(x)} + \left[\text{sign}(x) . \ln \left(\frac{\sqrt{x^2} + \sqrt{p^2 + y^2 + x^2}}{\sqrt{p^2 + y^2}} \right) \right]_{r_1}^{l_3+l_2} {}_{(y)}^{E-l_1} {}_{(x)} \right]$$

The previous expressions of efforts between parallel or perpendicular conductors, with or without contact, involve products of currents ($I_1 \times I_2$). In the case that these currents are complex and they are neither opposed nor in phase, it is necessary to take into account their phase shift. The purpose of this section is to show how we will take it into account.

We want to calculate the product $i_1 . i_2$, with:

$$i_1 = I_1 . \sqrt{2} . \sin\left(\omega . t + \varphi_1\right)$$

$$i_2 = I_2 . \sqrt{2} . \sin\left(\omega . t + \varphi_2\right)$$

The development of this product gives the following result:

$$i_1 . i_2 = I_1 . I_2 . \left(\cos\left(\varphi_1 - \varphi_2\right) - \cos\left(2.\omega . t + \varphi_1 + \varphi_2\right)\right)$$

The average value of the second term of the previous expression is zero. Accordingly, the expressions of electrodynamics efforts when electrical currents are in any phase shift are:

Cases of parallel conductors:

$$F = \frac{\mu_0 . I_1 . I_2}{4.\pi . \sqrt{p^2 + E^2}} . \left[\left[\sqrt{p^2 + E^2 + x^2} \right]_{l_3, l_3 + l_2 - l_1}^{l_3 + l_2, l_3 - l_1} {}_{(x)} \right] . \cos\left(\varphi_1 - \varphi_2\right)$$

Cases of perpendicular conductors without contact:

$$F = \frac{\mu_0 . I_1 . I_2}{4.\pi} . \left[\left[\text{sign}(x) . \ln \left(\frac{\sqrt{x^2} + \sqrt{p^2 + y^2 + x^2}}{\sqrt{p^2 + y^2}} \right) \right]_{l_3}^{l_3 + l_2} {}_{(y)}^{E-l_1} {}_{(x)} \right] . \cos\left(\varphi_1 - \varphi_2\right)$$

Case of perpendicular conductors with contact:

$$F = \frac{\mu_0 . I_1 . I_2}{4.\pi} . \left[\left[\frac{x}{r_1^2} . \sqrt{p^2 + y^2 + x^2} \right]_{(y)\ l_3}^{r_1\ E-l_1} + \left[\text{sign}(x) . \ln \left(\frac{\sqrt{x^2} + \sqrt{p^2 + y^2 + x^2}}{\sqrt{p^2 + y^2}} \right) \right]_{(y)\ r_1}^{l_3+l_2\ E-l_1} \right] . \cos(\varphi_1 - \varphi_2)$$

with I_1 and I_2 effective currents in Amps.

To address the mechanical structure, we must then translate the global efforts between conductors in terms of constraints on connections to incorporate these new data in design tools.

6.7. Conclusion

The purpose of this chapter was to show that, given the current need to take into account the wiring in power electronics as a component like the others, we can propose a method that is both generic and adapted to the design. This PEEC (Partial Element Equivalent Circuit) method not only calculates the values of model interconnection elements (resistance, inductance and mutual inductance), taking into account the frequency and proximity effects but, it provides a better understanding of magnetic phenomena, thus generating design rules to make little inductive connections, depending on the available technology.

It can justify many modern technological solutions dedicated to the “nanohenry hunt” for high power applications, such as bus bar technology, and provides criteria to choose an interconnection geometry rather than another. We show that for a constant volume of copper, a plate will be less inductive than a square bar.

Already, it is possible to add manually in “circuit” software, parasitic capacitances whose evaluation does not raise any particular problem.

The InCa3D software, based on this method, now opens the door to a real CAD technology in power electronics, to quantify, before realization and prototyping, the gain expected on the inductance by a particular geometry interconnection.

In addition, it enables EMC evaluation of an electrical device based on its wiring (coupled with the electrical simulation software SPICE, SABER, SIMPLORER, etc.).

In the future, this software will be able to take into account the mechanical and thermal constraints exerted on the wiring; it will be the complete design tool for wiring technology.

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Chapter 7

Commutation Cell

7.1. Introduction: a well-defined commutation cell

The concept of a commutation cell developed by H. Foch made it possible to describe in a rational manner the operation of the structures of power electronics. It is a powerful analytical approach, which allows us to determine the key players during a comutation. Initially applied only to the study of the overall operation of converters, this approach may also find application in the study of the finer phenomena of switching, if the whole environment of semi-conductors is well represented.

An example to illustrate these words: consider a three-phase voltage inverter produced on printed circuit board (Figure 7.1a). According to the modes of command, a switch will always commutate on an another one under the voltage of the power bus, the load operating as an instantaneous source of current. As a result, the basic commutation cell will always be of the same type on a structural level, the famous "chopper" cell or "inverter" cell according to the terminology (Figure 7.1b). Suppose now that we are interested in the phenomena of commutation or electromagnetic compatibility problems. It is no longer possible to ignore the influence of tracks, decoupling capacitors, packaging of semi-conductors and common mode capacitors. Figure 7.1c then shows a commutation that differs completely from another, since they are not the same elements (semi-conductors, tracks, common mode capacities, etc.), which are important.

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The "switching cell" analysis tool must therefore take into account all the modeling from the beginning.

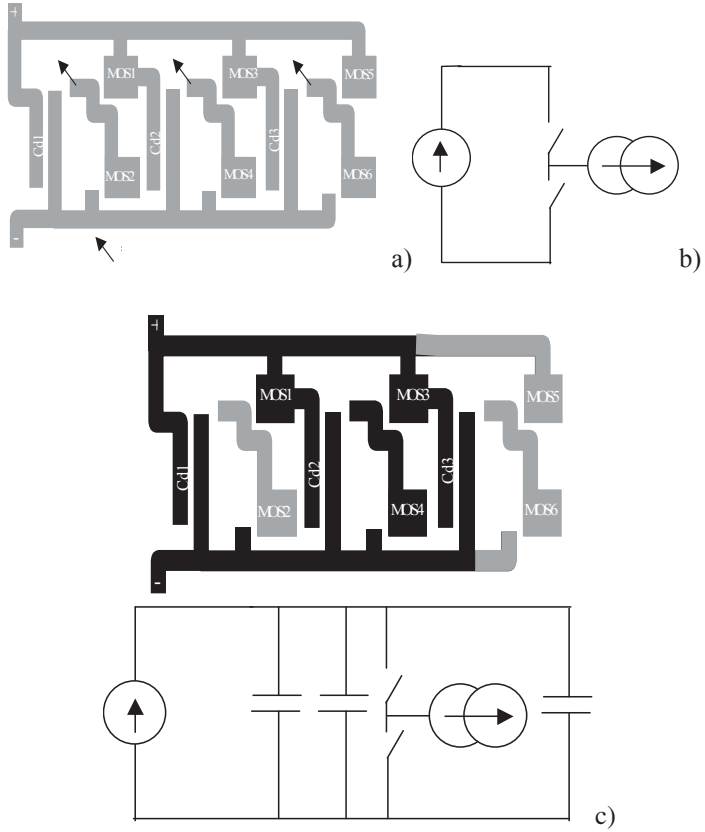


Figure 7.1. *Commutation cells for a three-phase inverter [TEU 97]:*
a) complete converter (with 3 decoupling capacitors);
b) structural commutation cell: identical for any commutation in this structure;
c) "technological" commutation cell during the commutation from MOS 3 to MOS 4

7.2. Some more or less coupled physical phenomena

The study which is conducted in this section is intended to define what must be represented, in a commutation cell, so as to be solved simultaneously. Indeed, the various physical aspects are not of the same degree of coupling, and it is not necessary to take into account everything at the same time; some problems can be resolved in a sequential manner.

Traditionally, we define strong couplings, which would require a concurrent resolution, and weak or unidirectional couplings authorizing a sequential approach. The fields of physics involved in the simulation of a static converter are:

– electromagnetics for any semiconductors and wiring aspects (power, control, conducted and radiated EMC);

– thermal and hydraulic physics (heat sink design);

– thermo-mechanics (differential dilatations, causes of breakage, etc.);

– thermoelectrics (on the one hand, physical parameters of semiconductors and wiring and, on the other, calculation of losses);

– electromechanics (tearing of bus bars in case of a short circuit, forces on supports);

– electrostatics – even electrodynamics – (partial discharges, dielectric breakdowns).

Some aspects can be clearly ranked among the weak couplings; it is evident that mechanical deformation in the wiring of power electronics will have extremely low influence – in normal operation – on the electrical wiring! Similarly, thermo-mechanical aspects can be handled independently of the electrical behavior of devices. The study of dielectrics may also be classified in the category of unidirectional couplings.

That leaves more sensitive aspects which concern the electromagnetic and thermal phenomena. For the pure calculation of a heat sink, hydraulic and thermal considerations, independent from a power electronics circuit, need to be carried out. But to determine the quantities of heat to remove, it is necessary to know semiconductor losses, and therefore the results of a temporal simulation. However, the electrical behavior of switches (and to a lesser extent wiring resistance) depends on their temperature. This is a bidirectional relationship. However, in a vast majority of cases, the efficiency of cooling and thermal constant times are such than an indication of the average operating temperature is sufficient. It therefore seems quite reasonable to predict the thermal state of the system to carry out a complete simulation, and to verify afterwards that – given the calculated losses – the forecast was right. This procedure must converge relatively quickly (2 or 3 iterations) and is much simpler than a complete electro-thermal resolution which is not really justified.

The different fields of physics have been limited to a mere (!) electromagnetic study, but there is still an analysis of various electrical phenomena in a converter. These can be cataloged under “power”, “command”, “conducted EMC” and “radiated EMC”.

It has been shown [YOU 98] that radiation aspects can be deduced from the knowledge of currents in conductors. In addition, the influence of radiated fields by the power signals on the electrical characteristics is negligible at the frequencies considered: the equivalent resistance of radiation at 100 MHz for conventional printed circuit systems does not exceed a few mΩ, which has no significant influence on waveforms.

$$R = 20 \cdot \beta^4 \cdot L1^2 \cdot L2^2$$

with β = wave number = ω/v. For L1 = L2 = 5 cm (radiation loop considered), R = 2.4 mΩ in vacuum (v = c) at 100 MHz.

The "conducted EMC" aspect is a little trickier: it seems fairly clear that the power waveforms depend very little on conducted emissions in most cases, but a few exceptions must be reported. The common mode current, led by strong voltage changes within the structure, flows through the power circuit and is therefore added to the switch current (Figure 7.2). While it is important, the change is significant and may even in some cases lead to malfunction of the mounting [LAP 98].

Without examining cases that are so bad, we are entitled to wonder if the phenomena are decoupled. [TEU 97] showed that in relatively realistic cases, waveforms are actually very dependant on the "EMC" environment to be added to the "power" commutation cell: dV/dt is not affected by the common mode capacities of the power circuit. This is not necessarily the case for the common mode capacity of a drive circuit (direct disruption of the board).

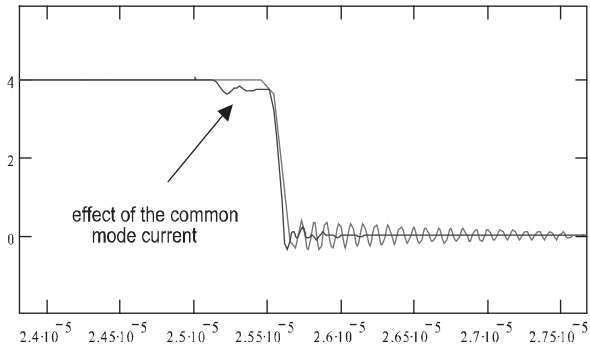


Figure 7.2. *Common mode current in a chopper cell changing the power current. Simulation of power circuit alone and adding a common mode capacitance of 1 nF (deliberately exaggerated value)*

In this case of unidirectional coupling, in a first approach, simulations of a power circuit may be performed, and then these waveforms may be injected in an "EMC" environment to obtain conducted disturbances. Figure 7.3 shows an example of low-coupling "power-EMC".

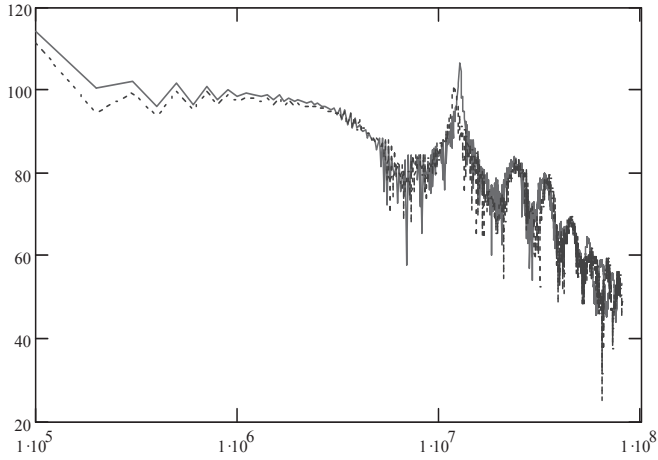
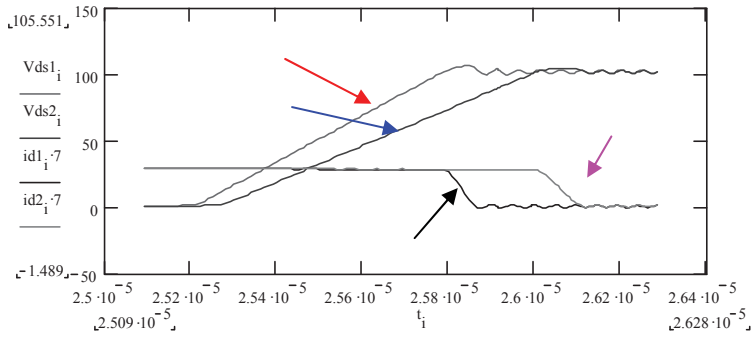


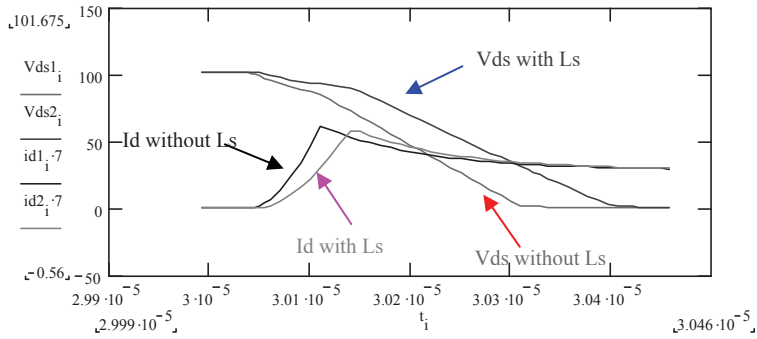
Figure 7.3. *Example of conducted disturbance (voltage on supply terminals on a Line Impedance Stabilizer Network)*

If, however, this assumption were too simplistic, taking into account the environment of the system in order to take account of this "EMC" aspect would be required. It is not too complicated insofar as this is only classic R, L, M, C circuit elements, and not heavy finite element calculations.

As far as other phenomena must be taken into account, the decoupling is no longer possible: these are interactions between semiconductors and wiring. Two examples may illustrate this assertion: the calculation of the voltage surge at the opening of a power switch, and interaction power-command phenomena by common impedance.



a) opening



b) closing

Figure 7.4. *Interaction power-command for an isolated grid component: the term Ls.di/dt reacts on the grid circuit, changing the commutation behavior. It must therefore be considered during the simulation. Simulation conditions: Rg = 50Ω, total mesh inductance 70nH: comparison between Ls = 0 and Ls = 20 nH (+ 50 nH on the mesh in this case)*

Concerning the voltage surge at the opening due to inductance of the switching mesh, Figure 7.5 clearly shows that decoupling is not possible in the case of fast commutations: indeed, the di/dt depends on the mesh inductance, and a simulation that does not take it into account is no longer realistic. Note however that for commutations where the component is greatly slowed down (strong grid resistance), the decoupling can be justified (Figure 7.14).

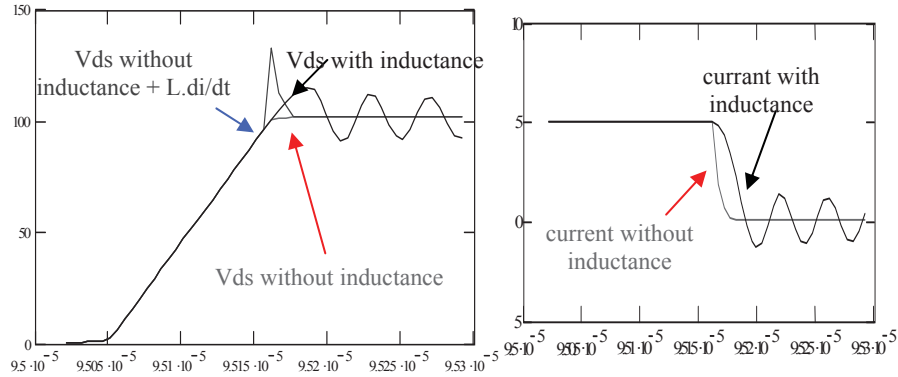


Figure 7.5. *In the case of a fast commutation, it is not possible to calculate the voltage surge at the opening L.di/dt without taking into account the inductor L in the simulation (we note that currents have different slopes) (simulation on PSPICE, MOS IRF.150, Rg = 10 Ω, L = 50 nH)*

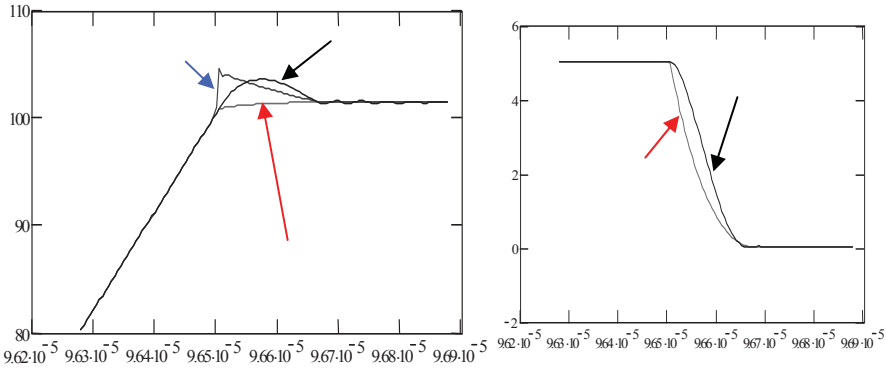


Figure 7.6. *For a commutation where the component is slowed (here 100 Ω as grid resistance), we can calculate the voltage surge afterwards without a too important mistake*

In conclusion, the minimal commutation cell to be simulated includes, in addition to the intentional active and passive elements (semiconductors, capacitors, possible magnetic components), inductive imperfections due to wiring. An indication of the average operating temperature is also necessary. A single commutation can be simulated with models as accurate as possible for each component mentioned.

7.3. The players in switching (respective roles of the component and its environment)

The semiconductor-wiring interactions are always very complex in nature since they involve the two semi-conductors of the commutation cell and electromagnetic environment. We were able to show that even if the determination of parasitic elements involves significant knowledge of electromagnetism and more or less complex resolution methods, the fact remains that their evaluation is linked to the knowledge of the strict geometry of the wiring. The geometric parameters are known with great precision and lead to reproducible results. It is not the same with the active components where, for example, the influence of the manufacturing process is fundamental.

Using finite element type fine modeling seems to us, given the current state of computers, a challenge. That is why we prefer a phenomenological approach quantitatively described by equations revealing analytical equations, efficient for various sensitivity analyses.

In this section, we are limited to the study of hard commutation phenomena, which is very widely used. The behavior of semiconductor commutation may appear easier to handle when commutation is of the "soft type", since the waveforms are governed by the passive components. We should not neglect the poor knowledge of recombination charge phenomena, for example in an IGBT under a voltage which is set through parasitic capacities.

Other restrictions: we are only discussing the MOSFET, the use of bipolar becoming increasingly marginal. Most of our conclusions may be adapted to the case of IGBT (with the exception of the tail current).

The purpose of this part is therefore to "dissect" a commutation cell made from a MOSFET-diode in order to determine "which does what" in a hard commutation, and if necessary, propose simple models which explicitly reflect these players in the commutation. The analyses that will follow are from various fine simulations, the only possible way of exploration. The study focuses on the commutation cell presented in Figure 7.7 below. It may indeed be shown that this representation based on three decoupled inductors is the simplest and most representative of phenomena [AKH 00, JEA 01, MER 96].

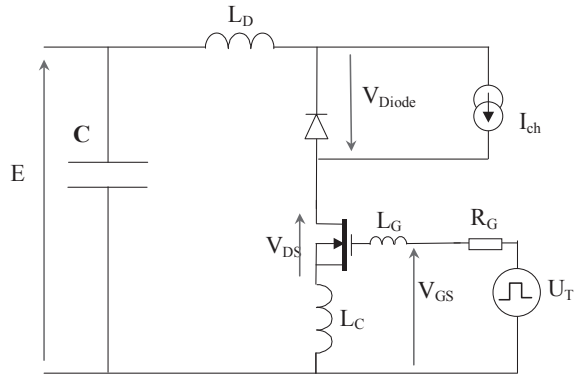


Figure 7.7. *Outline of the studied commutation cell and notations*

7.3.1. *Closure of the MOSFET*

7.3.1.1. *Qualitative analysis*

Figure 7.8 shows waveforms idealized during the closure of the MOSFET. First, the grid circuit is in charge until the grid source voltage reaches the threshold voltage Vth. Then the current source of MOSFET becomes active:

$$Imos = gm.(V_{gs} - V_{th})$$

During this phase, the diode is conductive, it can be concluded that its voltage is zero. The V_{ds} voltage of MOSFET remains relatively constant, there is only the voltage drop $(L_D + Lc).di/dt$ (with notations from Figure 7.7). As soon as the diode begins to "take the voltage" (i.e. as soon as an area of space charge appears), there is competition between the MOS speed, the speed of the diode and the Kirchoff equation governing the power circuit. Indeed, the diode voltage depends on the evolution of the size of the area of space charge. In addition, the grid circuit, as mentioned later, also governs the changing of the MOSFET voltage. Finally, the sum of voltages V_{ds}, V_{diode} and $(L_D+L_c).di/dt$ is kept constant at the value of continuous bus.

When commutation of the diode is completed, the current is constant, and Vds voltage continues to evolve, managed solely by the speed of the grid circuit and the component. The commutation is considered completed when the MOSFET reaches its ohmic area, i.e. that the voltage V_{ds} reaches $R_{dson}*I_o$. We should note that in some cases (low grid resistance or especially slow diode after the recovery), we can see the end of voltage switching before the end of current switching.

A particular case must be reported (Figure 7.9): it is either very fast MOSFET switching or a very strong inductor mesh (limit of switching circuit to aid the closure). In this case, voltage V_{ds} falls very rapidly to zero, due to strong term $(L_D+L_c).di/dt$ (either strong L_D+L_k or strong di/dt). As a result, $V_{diode} \approx 0$, $V_{ds} \approx 0$ and di/dt is therefore determined solely by continuous bus voltage, E and mesh inductance L_D+L_k. The rest of the commutation is completely governed by the diode.

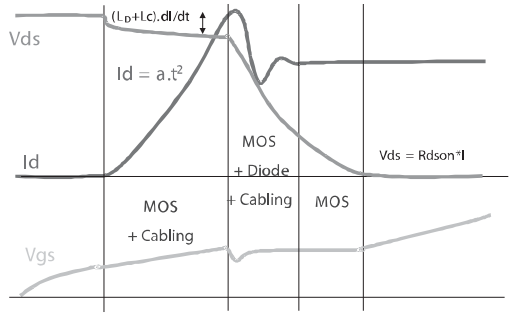


Figure 7.8. *Closing the MOSFET. The areas of dominance*

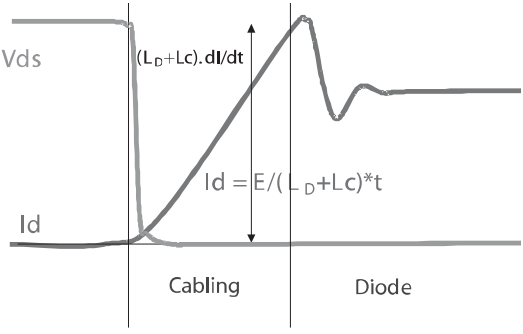


Figure 7.9. *Closing the MOSFET. Case of very fast MOSFET or very inductive wiring*

7.3.1.2. *Quantitative analysis*

The previous qualitative analysis has the merit of showing the different actors responsible for commutation waveforms. We will now examine more carefully the weight of these players during a sensitivity analysis.

We will consider the influence of inductor mesh and grid resistance, settings which are easy to tune. We will study more carefully the impact of semiconductors through their internal characteristics, that are closely related to their design (surface, doping, etc.).

7.3.1.2.1. Influence of wiring and grid resistance

Influence on the current

Here, the simulation allowed to vary easily mesh inductance L_D, and thus to assess the influence of this parameter for different grid resistances. We conducted several simulations (Figures 7.10, 7.11, 7.12). Within each series, we kept constant values of components (inductance and resistance) of the grid, and we vary the value of mesh inductance. In all cases we switched the same current of 7.5 Amps with a voltage of 200 V.

The first series of simulations was carried out with a grid resistance Rg = 2Ω.

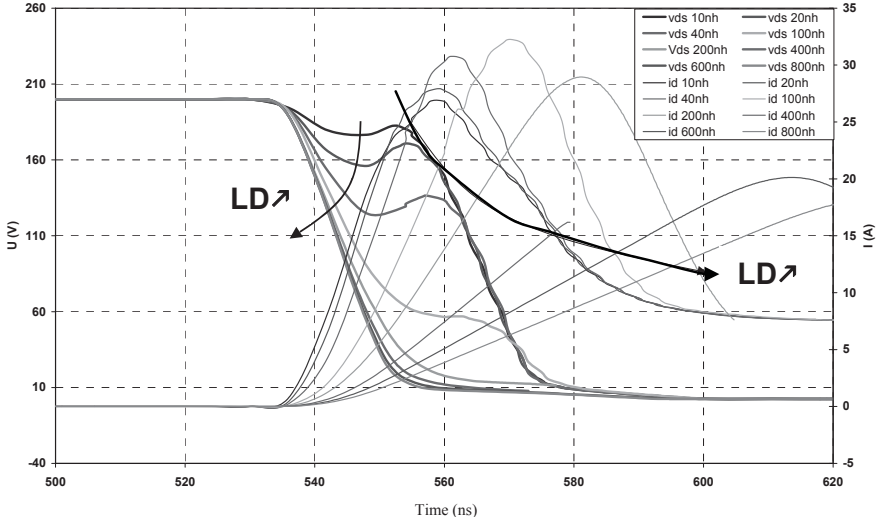


Figure 7.10. *Effect of inductance L_D for a low R_G (2 Ω)*

A second series of simulations was then carried out with a greater grid resistance Rg = 10 Ω.

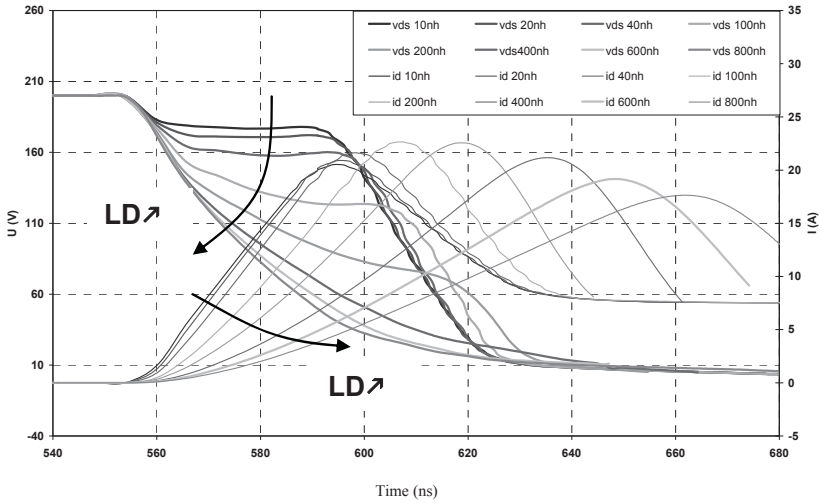


Figure 7.11. *Effect of inductance L_D for an average R_G (10 Ω)*

Finally a series of simulations was made with a more significant grid resistance (Rg = 50Ω).

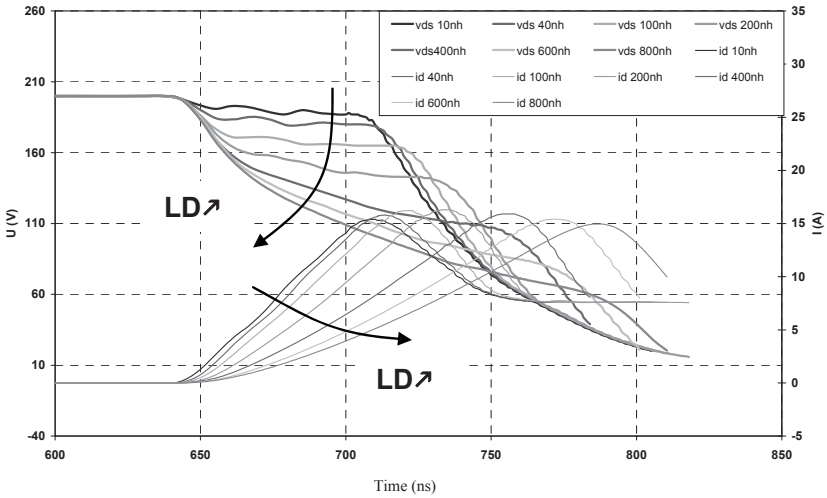


Figure 7.12. *Effect of inductance L_D for a large R_G (50 Ω)*

On the first series of simulations, we can observe that (when the value of inductance L_D increases) the inductive voltage drop equals the commutated voltage (E), and hence the value of dI_D/dt quickly reaches E/L_D. For more significant values of R_G, we find that the voltage drop never reaches the value E. This can be explained by the fact that the full discharge of capacity C_{ds} is required. $V_{GS} = V_{GD} + V_{DS}$, but during the commutation, V_{GS} # constant: to vary V_{DS}, it is required to vary V_{GD} by discharge of capacity C_{GD}. This discharge will be more rapid if the grid resistance R_G is lower.

From the previous curves, we can trace the evolution of dI_D/dt according to Ld (Figure 7.13), considering the area where the dI_D/dt is constant over time.

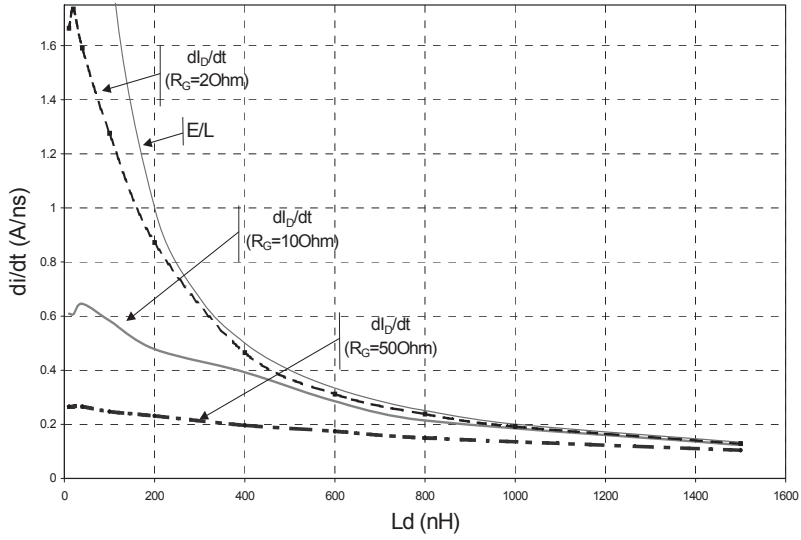


Figure 7.13. *Evolution of dI_D/d_t during the closure*

We note that for the large values of L_D and for low values of R_G, switching speed tends to E/LD: only the wiring then limits the commutation speed.

For large values of R_G, switching speed will be totally dependent on the circuit command and on MOSFET.

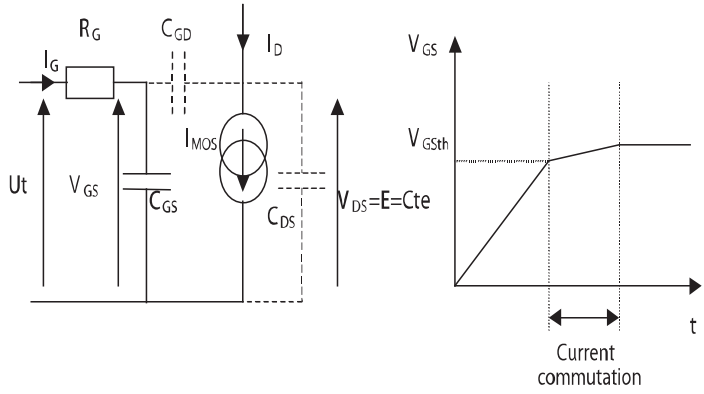


Figure 7.14. *Model of MOSFET for current switching when L_D is low and R_G is large*

During the current commutation, we assume that the voltage V_{GS} varies slightly and is almost V_{GSth}.

We consider that the current I_G is constant and is $I_G = (U_t - V_{GSth})/R_G$. As C_{GS} is much higher than C_{GD}, we consider that all current I_G flows in C_{GS}. Thus, we have:

$$V_{GS} = V_{GSth} + {I_G}/{C_{GS}} \cdot t$$

In addition, as L_D is low (in fact dI_D/dt low), the voltage V_{DS} will be regarded as constant and equal to E (no inductive voltage drop $L.dI_D/dt$). Thus, current through C_{DS} will be zero and therefore we obtain IMOS = I_D.

However, IMOS = $gm(V_{GS} - V_{GSth})$. Thus we have:

$$\frac{dI_D}{dt} = \frac{dI_{MOS}}{dt} = gm \cdot \left(\frac{Ut - V_{GSth}}{R_G \cdot C_{GS}} \right)$$

We note that for low values of L_D, dI_D/dt varies as $1/R_G$ by approximation gm ≈ constant, which is valid in the case of a sufficient level of switched current. The previous formulation will be valid only for large currents.

For larger values of L_D (or lower values of R_G), there is some competition between the two previous influences. [JEA 01, MER 96] then showed that the current switching speed is proportional to: $1/\sqrt{L_D \cdot R_G}$.

From there, we can break the evolution of dI_D/dt into three areas according to the mesh inductance L_D. The borders of these three areas are dependent on grid resistance R_G. They are summarized in the figure below.

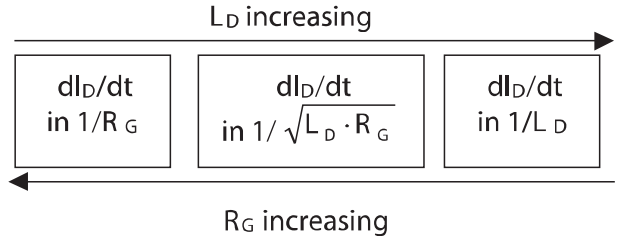


Figure 7.15. *Evolution of the switching speed of current according to R_G and L_D*

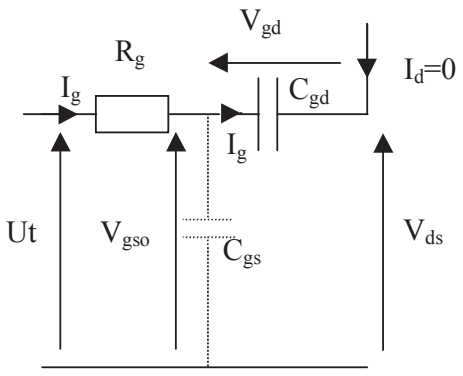
Influence on the voltage

[MER 96] proposed the following approach: we can consider that, at the first order, grid source voltage is maintained at a constant value noted:

V_{gso} ($V_{gso} = V_{th} + I_o/g_m$).

As a result the grid current ig is also constant and equals $ig = \dfrac{U_T - Vgso}{Rg}$.

This grid current charges (or discharges) capacity C_{gd}, causing the descent (or ascent) of voltage V_{ds}.



$$Vds + Vgd = Vgso$$

$$\Rightarrow \frac{dVds}{dt} + \frac{dVgd}{dt} = 0$$

$$ig = Cgd \cdot \frac{dVgd}{dt}$$

$$\boxed{\Rightarrow \frac{dVds}{dt} = \frac{Vgso - U_T}{Rg \cdot Cgd}}$$

Figure 7.16. *Equivalent schematic during the voltage commutation, and formula of the dV/dt*

The formula produced by this simple reasoning shows the role of grid resistance, and MOSFET parasitic capacitance.

7.3.1.2.2. Influence of MOSFET parameters

Parasitic capacities

We have just seen the influence of capacity C_{gd} (or "Miller" capacity) on the speed of evolution in voltage. We can easily show through simulations that if we keep the product $R_g.C_{gd}$ constant, the dV/dt is well preserved. The rest of this section is interested in the switching speed of current.

We will confirm the influence of this or that capacity. Starting from the reference values corresponding to the capacities identified on a MOSFET (IRF450FI), we have multiplied them by a coefficient. This method helps to keep developments consistent.

We can see that C_{GS} and C_{GD} have a strong influence on the moment of the beginning of the commutation. This is consistent with the model from Figure 7.14. Indeed, the first phase of the commutation, prior to the start of the evolution of current or voltage, is made up of the capacity charge C_{iss} ($C_{GS} + C_{GD}$). We note, however, that during the closure, the influence of C_{GD} (C_{rss}) on the moment of the beginning of the commutation, does not seems obvious here. This is because at the beginning of closure, the V_{DS} voltage is significant, and values of C_{rss} are low when V_{DS} is large, compared to those of C_{iss}.

We have identified in Table 7.1 the impact of these changes on the current commutation, including the evolution of (dId/dt) max (switching speed of current).

	Value of $\left(\frac{dI_D}{dt}\right)_{max}$ A/ns		Value of $\left(\frac{dI_D}{dt}\right)_{max}$ A/ns		Value of $\left(\frac{dI_D}{dt}\right)_{max}$ A/ns
Cgs*0.25	1.44	Cds*0.25	1.12	Cgd*0.25	2.12
Cgs*0.5	1.32	Cds*0.5	1.19	Cgd*0.5	1.71
Cgs*2	1.21	Cds*2	1.37	Cgd*2	1.14
Cgs*4	0.9	Cds*4	1.55	Cgd*4	0.88

Table 7.1. *Influence of CGS, CDS, CGD on the evolution of current ID (closure of the MOSFET)*

Regarding the current speed dI_D/dt, only C_{gd} seems to be predominant. This is because during these phases, command voltage (V_{GS}) and power voltage (V_{DS}) are almost constant. However, in full rigor V_{GS} and V_{DS} are not constant, it is therefore normal that the associated capacities (C_{GS} and C_{DS}) have an influence on the speed of change of the switched current.

Source current of the MOSFET

As in the case of capacities, we can confirm the importance of taking into account the non-constant gain *gm* (recall: $I_D = gm \cdot (V_{GS} - V_{GSth})$ is not consistent with non-constant *gm*) of the current source according to VGS. We then looked at the importance of the value of *k* gain on the switching speed of current. In our case, the quadratic modeling $\left(I_D = k\left(V_{GS} - V_{GSth}\right)^2\right)$ is valid for I_D less than about 25 Amps, we have therefore taken care not to exceed this value during simulations using different values of *k*.

The influence of non-linearity in the modeling of the power source is highlighted in Figure 7.17. The gains $I_D = gm(VGS)$ used are shown below. The simulation conditions are as follows: rg = 10 Ω,LD = 40 nH, L_{dio} =10 nH, L_G =20 nH, E = 200 V and I commuted = 7.5 Amps.

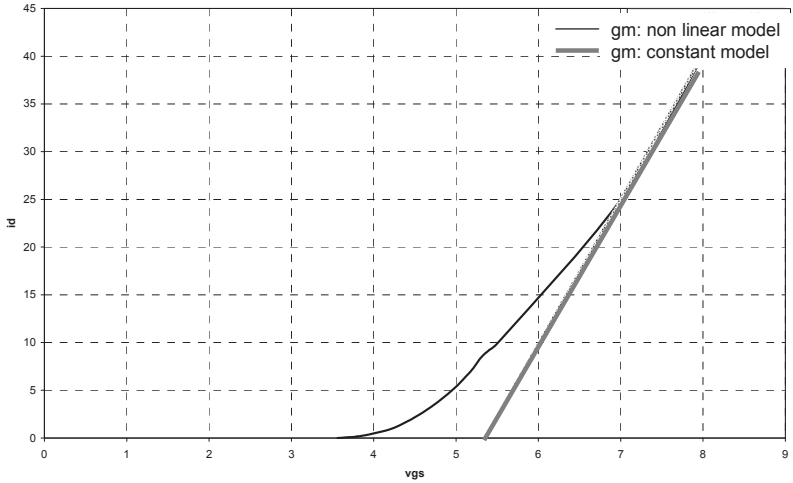


Figure 7.17. *Constant or non linear model for gm. Constant gm leads to linear variation of ID as a function of Vgs*

NOTE. – We note that for significant currents (beyond 25 Amps in this case), *gm* is constant.

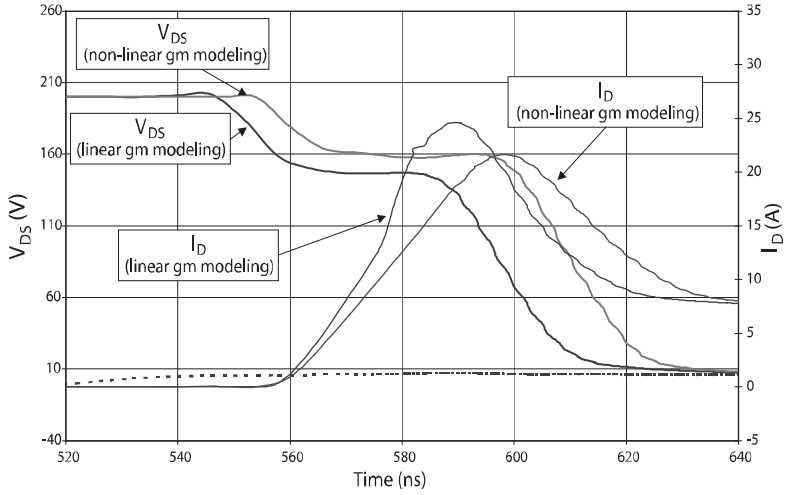


Figure 7.18. *Influence of modeling of the current source of MOSFET*

The non-linearity of the current source (variable gain *gm*) is naturally visible during the current commutation. Regarding the influence of the coefficient *k*, it is necessary to distinguish the closure from the opening of the MOSFET.

At the closing phase it can be seen that the current IMOS is almost equal to the current ID (neglecting the current passing through CDS as VDS is almost constant). Now IMOS depends on VGS, thus *k* gain has a strong influence. Note that this reasoning is valid only if the inductive voltage drop $L_D \cdot dI_D / dt$ is not too significant, i.e. if voltage VDS does not tend to 0: in this case the current would be imposed only by the mesh equation ($E = L_D \cdot dI_D / dt$).

The simulation results are available in the table below.

	Values of $\left(\frac{dI_D}{dt}\right)_{max}$ A/ns
k = 3.5	1.33
k = 5	1.47
k = 7.5	1.62
k = 10	1.74

Table 7.2. *Influence of gain k on current ID evolution (closing MOSFET)*

The gain *k* of the controlled current source is part of the parameters strongly influencing the switching speed of the current at the closure of the MOSFET. The static characteristic of the MOSFET (and its variation depending on the temperature) must be taken into account for associations of components, particularly for the balance of currents when setting in parallel.

7.3.1.2.3. Influence of the diode

We will see here the influence of parameters τ (carrier lifetime), W (thickness of the ν area with low doping) and Sa (active section of the diode).

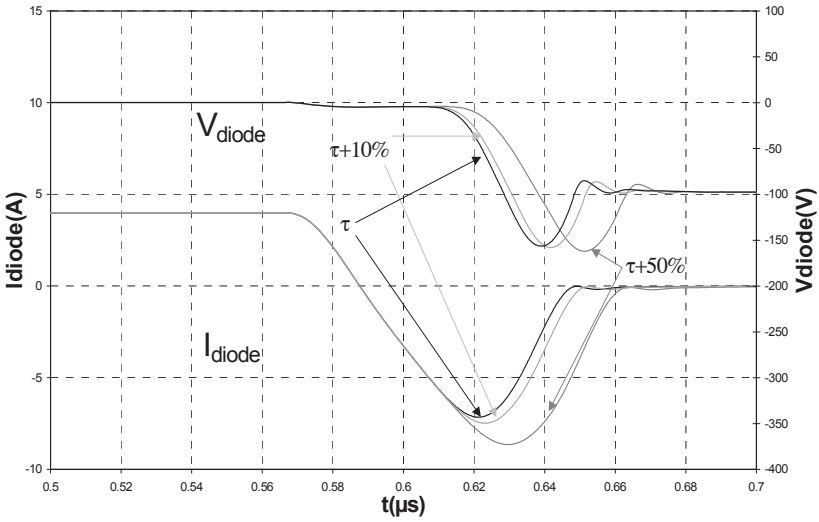


Figure 7.19. *Influence of parameter τ*

Figure 7.19 shows the evolution of currents and voltages depending on parameter τ. Compared to a reference value (corresponding to a real diode), we have increased it by 10% and 50%.

The switching losses increase of 4% (respectively 20%) and the value of the recovery current of 3% (respectively 13%) when the carrier lifetime increases by 10% (respectively 50%). We note that the carrier lifetime τ strongly influences the level of recovery current (Figure 7.19), and hence losses, but the influence on the switching speed of voltage remains negligible. Parameter τ is a parameter that is difficult to estimate (OCVD method [GHE 98]), but its influence on the recovery current is important. It will be relatively easy to determine this by superimposing experimental waveforms on simulated waveforms.

Using a similar procedure to the study of the influence of τ, we see that the thickness of the *W* zone with low doping (zone ν) specifically affects the voltage switching speed. According to Figure 7.20, an increase of *W* leads to increased switching speed. Note also that in our case, increasing *W* also creates a slight decrease in the recovery current, but this is not always the case. Indeed, depending on lifetime τ, the stored charge may increase or decrease with an increase of *W*. In the case of a long lifetime (recovery diode for example), an increase of *W* would

produce an increase in the stored charge, and therefore an increase of the recovery current.

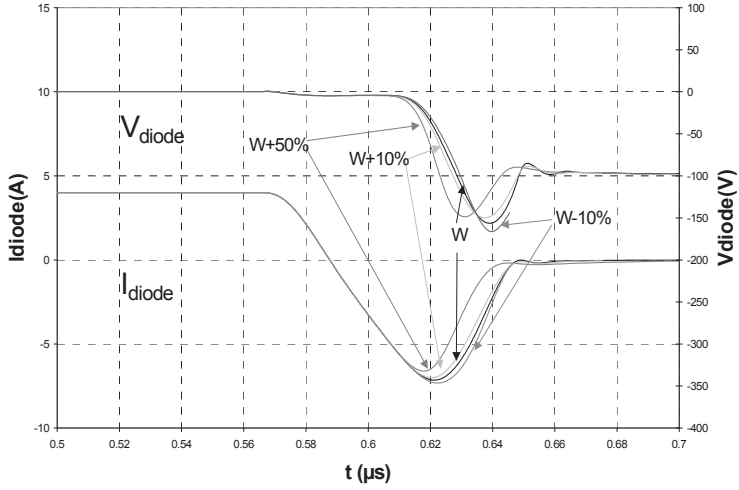


Figure 7.20. *Influence of W (width of the low doped zone)*

We then studied the influence of Sa, the active area of the diode. We note that its increase (Figure 7.21) has little influence on commutation waveforms.

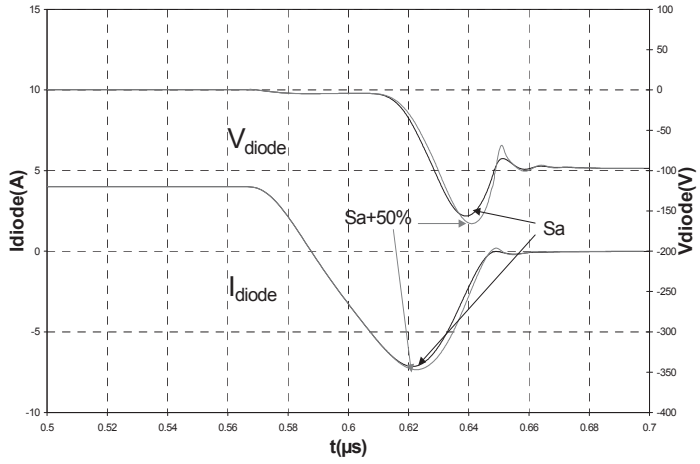


Figure 7.21. *Influence of Sa (active surface of the diode)*

Thus, we found a number of parameters involved in the closure of the diode. The mobility and the parameters of carrier recombination are little changed from one component to another; furthermore, commutation waveforms are not very sensitive to them. The geometric parameters (*W* and *Sa*) are relatively easy to identify using techniques such as spreading resistance (characteristic capacity – voltage c (v)) [GHE 98]. These identification techniques will also inform us on the doping profile of the ν area. In conclusion, we can use the waveforms at the closure of the MOSFET to identify the value of the carrier lifetime τ: this parameter, which is influential during the recovery phase, may be identified by comparing simulation to measurement.

7.3.2. *Opening of the MOSFET*

7.3.2.1. *Qualitative analysis*

Figure 7.22 shows idealized waveforms at the opening of a MOSFET. First, the grid circuit is discharged until the grid voltage reaches the source voltage Vth + Io/gm. At this point, the voltage is maintained at this threshold Vgs value, and the grid current, then roughly constant, ensures the development of voltage Vds via the discharge capacity Cgd. Note we assume here that the diode can change its space charge (hence its voltage) almost instantly or, in other words, it does not limit the rise of MOSFET voltage. Once the voltage Vds reaches the value of the continuous power bus, the diode is under zero voltage and becomes conductive. Then a current commutation occurs within the MOSFET, which will be governed by the component, its grid circuit and the wiring parameters. The commutation ends when the current and voltage oscillations caused by the MOSFET capacitors in the off state and wiring inductance LD + LC are damped. Hence the diode has little influence during this commutation phase (opening), insofar its over voltage during closing is neglected.

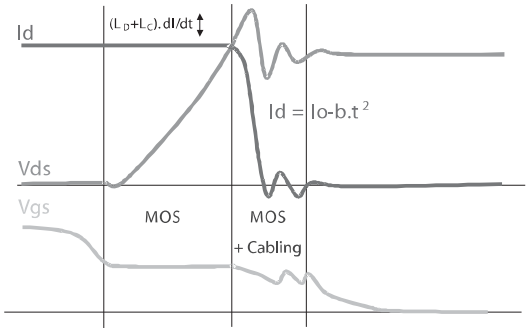


Figure 7.22. *Opening of MOSFET. Areas of dominance*

As for closing, the particular case of an aid circuit to the commutation may be mentioned, even if with hard commutation, no "spontaneous" scenario (without an aid capacitor for the opening) can be observed. In this case, the drain current falls sharply, the aid capacitor to the commutation is then charged by the load current. The voltage slope is then Io/Cds, and becomes independent of the component.

7.3.2.2. *Quantitative analysis*

7.3.2.2.1. Influence of wiring and grid resistance

Influence on the current

The phenomena are not very different from the case of closure: there is a new time competition between component speed (managed by its grid circuit) and the wiring. Figure 7.23 shows, for example, the influence of grid resistance on switching speed dI/dt, and Figure 7.24 that of the influence of inductance LD. It should be noted, as discussed for the closure, that large grid resistance or high mesh inductors slow down current switching speed. Figure 7.24 also shows that for "large" grid resistances, inductance LD has no more influence on the dI/dt.

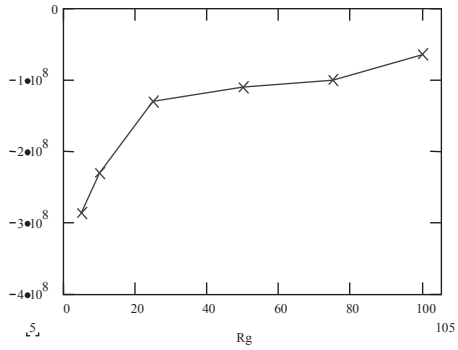


Figure 7.23. *Change in dI/dt depending on the grid resistance (fine simulation)*

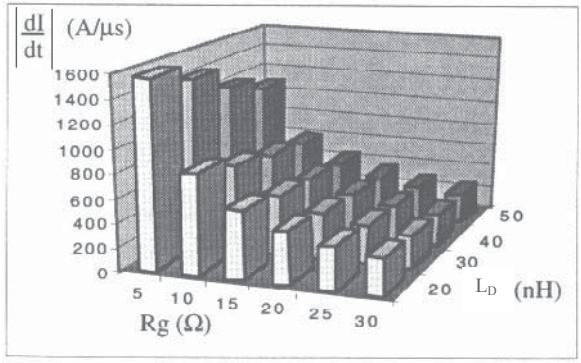


Figure 7.24. *Respective influences of grid resistance and mesh inductance on di/dt at the opening (Lk constant = 5 nH)*

Another example is the influence of the Lc common inductor (defined in Figure 7.7), which is able to make changes in the power current and re-inject on the grid circuit a voltage Lc.dI/dt, which amends the grid current and therefore the switching speed, and may even lead to the restoration of conduction of the component. This phenomenon, shown experimentally in Figure 7.25 may also occur at the closure.

Figure 7.25. *Perturbation of a static converter by the common impedance at the opening of MOSFET (experimental waveforms from [MER 96])*

Figure 7.26 shows the influence of the common inductance of source Lc on the speed of evolution of the current at the opening, but also at the closure.

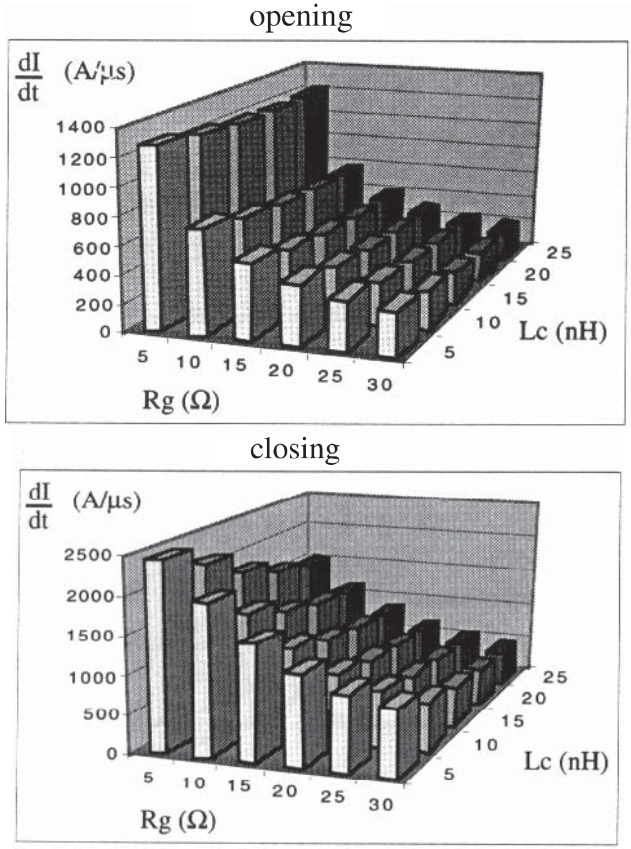


Figure 7.26. *Influence of common inductance L, for a mesh inductor LD + Lc constant, at the opening and closing [MER 96]*

The set of equations to calculate the speed of evolution of the current, to separate the respective influences of the total inductance of the switching mesh (LD + Lc) and of the common inductance Lc, is not particularly simple [JEA 01, LAU 99], and will not be repeated here. Note that [AKH 00] offers elegant wiring solutions to address this problem.

Influence on the voltage

The approach proposed earlier remains valid, as well as the proposed equations, which underlines the role of grid resistance Rg and "Miller" capacity Cgd.

7.3.2.2.2. Influence of MOSFET parameters

Influence of parasitic capacities

First, reiterate the need to take into account non-linearity of these capacities, particularly for low values of VDS [FAR 94]. We have made here two simulations, the first (Figure 7.37a) takes into account the phenomenon of variable capacities, the second does not. We note, in Figure 7.37a that voltage evolves in a non-constant way, whereas in Figure 7.37b, evolution is almost linear for most of the commutation.

This is particularly noticeable on the assessment of switching losses. There is a difference of almost 15% between the two approaches (45.7 μJoule in the case of taking into account the non-linearity, 39.8 μJoule in other cases).

Regarding now the rate of change in voltage (dVds/dt), the relatively simple approach proposed for closure (b) [MER 96], if it is still valid by changing the value of UT, does not take into account the capacity Cds. With such an analysis, we cannot see how an external aid capacitor to the commutation could intervene in the dV/dt. We can find in [JEA 01] a somewhat more detailed analysis in order to take into account a snubber capacitor Cds which aids the commutation.

Regarding the influence of parasitic capacities on the current, Table 7.3 (obtained in the same manner as for the closure) shows the influence of parasitic capacity on the evolution of (dId/dt) max (commutation speed of current).

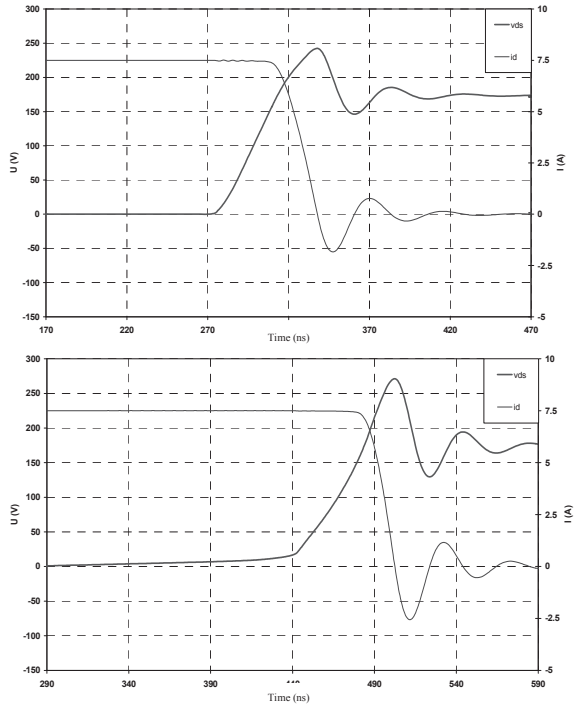


Figure 7.27. *Simulated waveforms at opening of a MOSFET*
(a) taking into account non-linearity of the parasitic capacities
(b) without taking into account non-linearity of the parasitic capacities

	Value of $\left(\frac{dI_D}{dt}\right)_{max}$ A/ns		Value of $\left(\frac{dI_D}{dt}\right)_{max}$ A/ns		Value of $\left(\frac{dI_D}{dt}\right)_{max}$ A/ns
Cgs*0.25	–17.8	Cds*0.25	–19.7	Cgd*0.25	–17.2
Cgs*0.5	–17.4	Cds*0.5	–19.3	Cgd*0.5	–16.9
Cgs*2	–15.8	Cds*2	–13.7	Cgd*2	–15.6
Cgs*4	–14	Cds*4	–9.56	Cgd*4	–14.7

Table 7.3. *Influence of CGS, CDS, CGD on the evolution of current ID (opening of MOSFET)*

As with the closing, the influence of Cgs capacity is very low, since it is under an almost constant voltage. The influence of Cgd is confirmed, as for the closure.

The strong influence of the increase of Cds is certainly justified here by a change of switching behavior ("snubber" effect).

Influence of the current source

In the case of opening, the situation is different from the closure: Table 7.4 shows the low influence of gain *k*. We can attribute this phenomenon to a competition between speed of grid circuit and speed of power circuit. Drive current IG flows through CGD and imposes voltage VDS, the current ID is then imposed by the law of meshes ($E = VDS + L_D \cdot dI_D / dt$). The speed of evolution of this current is the result of a compromise between the equation of the power mesh and the equation of the grid circuit.

	Value of $\left(\frac{dI_D}{dt}\right)_{max}$ A/ns
k = 3.5	–15.8
k = 5	–16.1
k = 7.5	–16.4
k = 10	–16.7

Table 7.4. *Influence of gain k on evolution of current ID (closing of MOSFET)*

7.3.2.2.3. Influence of the diode

The diode as little influence. Figure 7.28 shows the changes in waveforms of current and voltage for 50% variations of parameters τ, *Sa* and *W*.

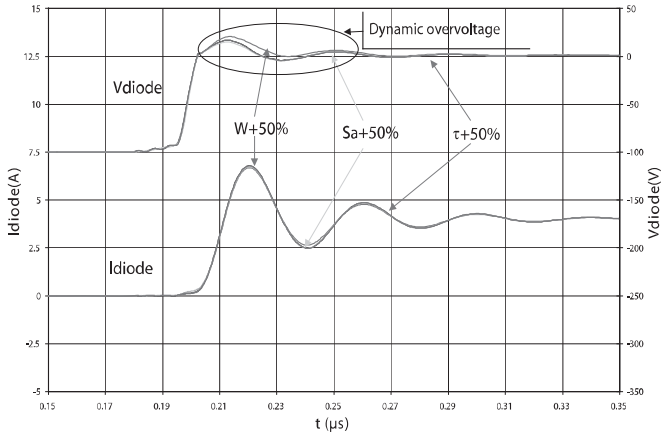


Figure 7.28. *Influence of the diode at the opening of MOSFET*

The above figure shows that changes in the physical parameters of the diode have little influence on commutation waveforms, except on the voltage surge when the diode is switched on [KOL 00]. In particular, we note that the dVDS/dt is controlled by the MOSFET alone.

7.3.3. *Summary*

Based on previous results, we can establish a table summarizing the relative influences of the different elements analyzed (0 = zero, + = little importance, ++ = important, +++ = very important). This table has been completed about dVDS/dt using the results of [MER 96], as well as those developed in the following section.

	CGD	CDS	CGS	LG	LD	k or gm	Iload
dID/dt	+++	++	++	0	+++	+++	0
dVDS/dt	+++	++	+	0	0	+	+

Table 7.5. *Summary of influences for the closure of MOSFET*

	CGD	CDS	CGS	LG	LD	k or gm
dID/dt	++	+++	+	0	+++	+
dVDS/dt	+++	++	+	0	0	+

Table 7.6. *Summary of influences for the opening of MOSFET*

Parameters Ut and VGSth drive the value of current IG through the grid resistance RG, these three parameters therefore influencing the charges and discharges of capacities CGD and CGS, and hence thereby both the early moments of commutation and switching speeds.

Note also that the capacities of the MOSFET influence the switching speeds of voltage. During these phases, the VGS voltage is almost constant, and the influence of capacity CGS will be low. The charge (or discharge) of the CGD capacity determines almost the entire evolution of voltage, its influence will be very important. In some cases, the CDS capacity limits dVDS/dt through the load current at the value Iload/CDS. Its influence may be significant.

7.4. References

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Chapter 8

Power Electronics and Thermal Management

This chapter is devoted to the thermal environment of silicon chips, which is vital during the design of converters.

8.1. Introduction: the need for efficient cooling of electronic modules

The field of power electronics concerns the conversion of electrical energy. Produced mainly by an AC sinusoidal current (50 or 60 Hz), this energy must be adapted to the requests of users. The fields of application of power electronics are large and they range from large industrial powers (electrochemistry, electrometallurgy), to battery chargers of a few watts, which are increasingly used in mobile devices.

Many applications requiring variable frequencies (variation of speed by electric drives, induction heating), or continuous voltages of different values (the continuous transformer does not exist), will also make use of power electronic static converters. Finally, it is often useful to have a high frequency intermediate circuit (from some 10 kHz to about 100 kHz) to reduce the size of passive elements of a converter and consequently to increase the compactness of the devices.

In all these applications, efficiency is absolutely necessary: power electronics differs from traditional electronics. The main constraint of the latter is to preserve

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Chapter written by Corinne PERRET and Robert PERRET.

the integrity of a signal. The technologies of components used for these two disciplines are often very different.

The formatting of electric power is often based on a switching technique, the electronic component working as a fast switch. By controlling the duration of the on-state (the switch conducts), and of the off-state in a periodic process (Figure 8.1), the treatment of electric energy is processed in order to make the characteristics of the source compatible with the characteristics of the load.

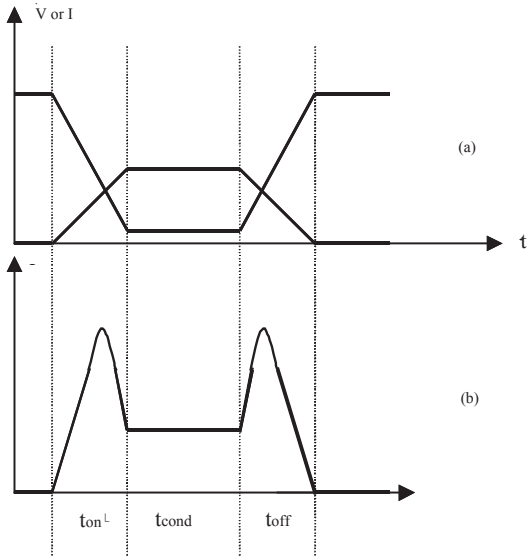


Figure 8.1. *a) Waveforms of voltage and current in a switch; b) instantaneous power dissipated in the switch*

We see in Figure 8.1a that when the switch is conductive, a residual voltage persists at the terminals of the component: this is the cause of conduction losses. Another phenomenon appearing during commutations: at switch-on, there is a time t_{on}, during which there is both a voltage higher than the residual voltage, and a current. Following this is an important instantaneous power (Figure 8.1b) and therefore an expenditure of energy at each switch-on. The same is true for closure, during the time t_{off} [TAN 97].

At blocked-state, in normal operating conditions (Tj < 125°C), leakage currents generate losses that are generally negligible, hence the existing components can be

regarded as perfect. The energy dissipated in the chip can be calculated by integrating the instantaneous power for each period.

Now consider the elementary case of a switching power supply DC/DC whose principle scheme is given in Figure 8.2a.

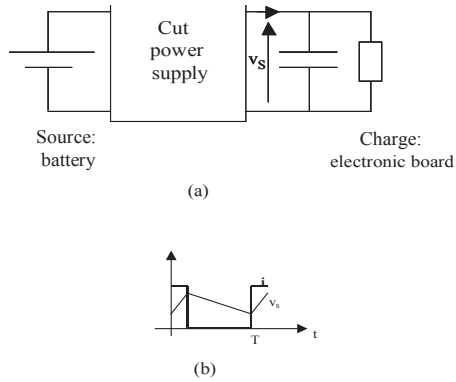


Figure 8.2. *a) Schematic of a DC/DC switching power supply; b) forms of current and voltage*

In this example, we can make a cut on the current i, as shown in Figure 8.2b. The aim is to have a voltage v_s "as continuous as possible". This is achieved with a filter whose RC time constant is the greatest possible compared to the switching period T. It is therefore obvious that as period T shortens, the filter is reduced, that is to say that RC is small, hence the interest of high-frequency (for power electronics, we refer to form kHz to MHz).

As a drawback, the dissipated power during commutations increases proportionally to the frequency. Faster components are therefore (reduced t_{on} and t_{off}) and/or circuit techniques with shifting current and voltage front edges (aids circuit to the commutation, [FOC 98, ROU 90] to reduce as many losses as possible.

It is also necessary to cool the component to maintain its temperature at an appropriate value for operation. The silicon components allow for a maximum temperature of about 120°C to 150°C (note that industrial applications do not exceed 125°C in order to respect the rules of reliability) [MER 00].

Before tackling our main interest, thermal design of the micro-cooler by fluid heat transfer, we will present, in this chapter, the main characteristics of power components that are vital for an understanding of our "all silicon" approach to be

discussed in section 8.2. Finally this chapter will conclude with a reiteration of the heat laws that will be used later in the study.

8.2. Current power components

8.2.1. *Silicon chip: the active component*

Power electronics began with junction components, namely diodes, bipolar transistors and thyristors. Over the past decade, the development of power semiconductors has incorporated isolated grid components (MOS, IGBT). For this last family of components we will design coolers considering currents of 100 A and voltages of about 1 kV. The components of this range typically have the following dimensions: 1 cm × 1 cm for a thickness between 250 and 500 µm. Thus the losses will be generated in the volume of a few tens of mm^3. To evacuate them, given the presence of connections and electrical insulation, only the underside (of 1 cm^2 in this example) is available. A characteristic assembly cross-section for this type of component is shown in Figure 8.3.

We will now consider the origin of individual losses and list the main difficulties encountered to limit them.

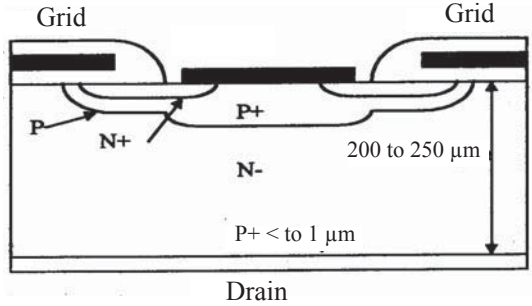


Figure 8.3. *Cut of the silicon chip of an IGBT*

8.2.1.1. *General construction of a power component*

A power component is mainly designed for its voltage strength, which is provided by a layer of silicon slightly doped N^-(10^{13} cm^{-3} to 10^{14} cm^{-3}; resistivity 100 Ω.cm); and relatively thick (a few hundred µm) area of voltage holding. As components of power electronics are of vertical type, this area has a current flow. To make the device a conductor, mobile n or p-type carriers must be injected in vast quantities into the voltage holding area. In the example of a diode, the density

$p = 10^{17}$ cm^{-3}. The presence of this area partly explains the residual voltage, which is even bigger when the voltage to be held during the blocking state is greater. In power components, you obtain residual voltages in the range of 2 V. With a common current density of 100 A/cm², conduction losses are around 200 W/cm².

For these injected charges to complete the role described above, they should not recombine in the voltage holding area. Thus, the length of diffusion must be of the same order of magnitude as the thickness of the area, which corresponds to an important lifetime of p carriers. The presence of the stored charge, which must be injected and eliminated, explains the phenomena observed at switch-on and switch-off. The design of components is therefore a delicate compromise, between residual voltage and importance of stored charge, which directly drives the speed of the power current [ARN 92, LI 98].

8.2.1.2. *Modeling conduction losses*

Whatever the nature of the power component (bipolar, unipolar, mixed), there is, during the conduction, a law between the voltage drop at the terminals, the conduction current and the temperature of the active part, [FAR 94]. The graphs shown in Figure 8.4 clarify the linkages between these three values for three IGBT of the same family. They show the influence of compromises made by the manufacturer between increased speed and reduced voltage drop (voltage existing on terminals of component when in the on-state). The fastest IGBT, Ultrafast, has a dropout voltage almost twice as large as the standard IGBT.

To calculate losses, the characteristic I(V) is usually modeled by a classic linear law:

$$Ve = V_0 + r_0 I$$

where V_0 represents the threshold voltage, and r_0 the dynamic resistance.

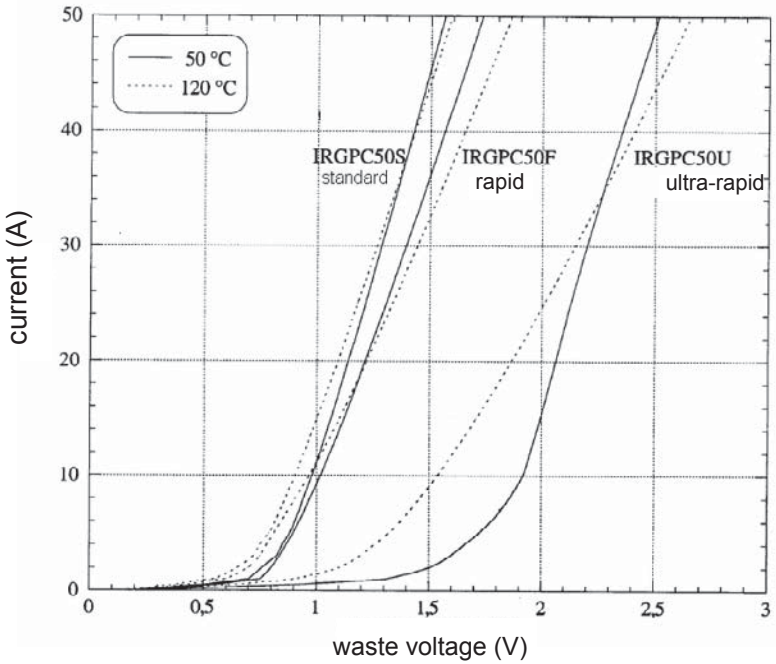


Figure 8.4. *Direct characteristics of standard IGBT, fast and ultra fast at 50°C and 120°C*

As the characteristics of Figure 8.5 show, these parameters change with the temperature of the active part of the component. V_0 decreases with temperature Tj of the area while r_0 increases.

To translate this dependant relationship, we write:

$$V_0 = V_{00} - aTj$$

$$r_0 = r_{00} + bTj$$

From tests run under at least two temperature values, it is possible to identify the values of the four parameters and thus calculate the losses of conduction for a given temperature. If the latter is unknown, we can proceed by iteration.

In conclusion, for the conduction phase, it is quite easy to have a general formula for losses if the temperature and current imposed by the external circuit are known.

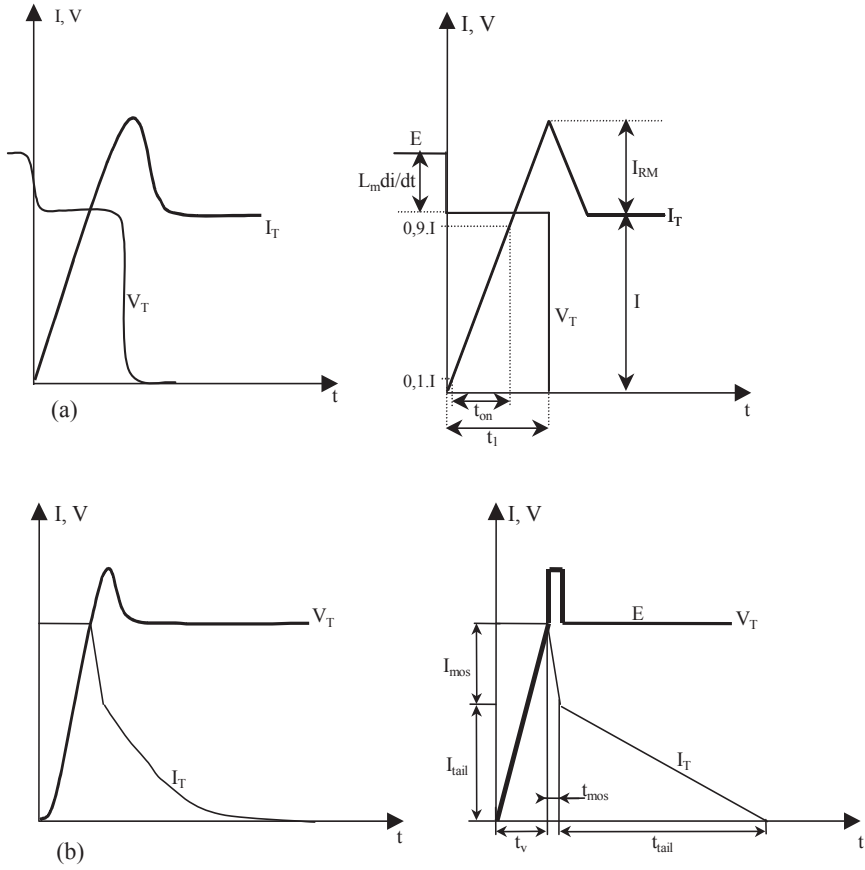


Figure 8.5. *Actual and modeled voltage and current waves, at (a) the closure,and (b) the opening of transistor T of an elementary switching cell (see Figure 8.6)*

8.2.1.3. *Modeling of commutation losses*

For this type of operation, determining losses by a general formula is far more difficult because current and voltage waveforms depend both on electronic components, on their command, on the type of commutation used, and on the external circuit including parasitic elements. Figure 8.6 gives respectively real waveforms and modeled waveforms obtained at the closure and opening of an IGBT, switching with a diode in the case of an elementary switching cell, where L_M represents the parasitic inductance of the mesh (Figure 8.6).

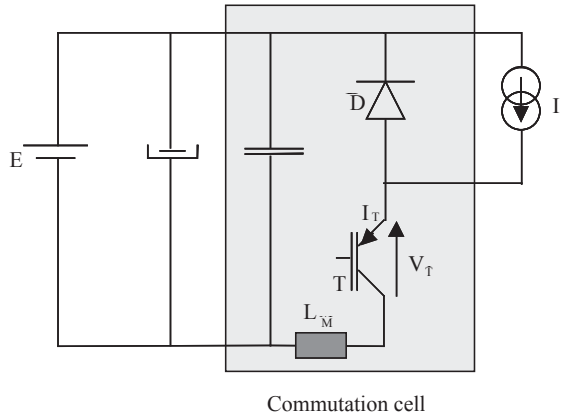


Figure 8.6. *Elementary commutation cell*

In his thesis, S. Raël [RAE 97] offers empirical formulae for estimating the value of energy dissipated in an IGBT at opening (W_{off}) and at closure (W_{on}) (see Figure 8.6).

At closure:

$$W_{on} = k_{on}.E.I\text{-}k'_{on}.I^2 \quad \text{with:} \quad k_{on} = 0{,}4.\frac{t_1^2}{t_{on}}$$

where t_1 and t_{on} are times illustrated in Figure 8.5a.

At the opening, waveforms are more complex and depend very much on the nature of the IGBT used, including the importance of the tail current (current that flows after the end of the grid command and is characterized by I_{tail}). In the experiment described above, we obtain:

$$W_{off} = k_{off}\,EI + k'_{off}I^2$$

$$\text{with:} \quad k_{off} = \frac{t_v}{2} + \frac{2\beta+1}{2(\beta+1)}t_{mos} + \frac{\beta}{2(\beta+1)}t_{tail}$$

$$\text{and:} \quad k'_{off} = \frac{2\beta+1}{2(\beta+1)^2}L_m$$

$$\beta = \frac{I_{tail}}{I_{mos}}$$

With the approaches and characterizations of switching components on an identified circuit (the role of command, of inductance Lm) we obtain formulae for predicting the losses of commutation.

Previous works showed that the values of various parameters also change with temperature (Figure 8.7).

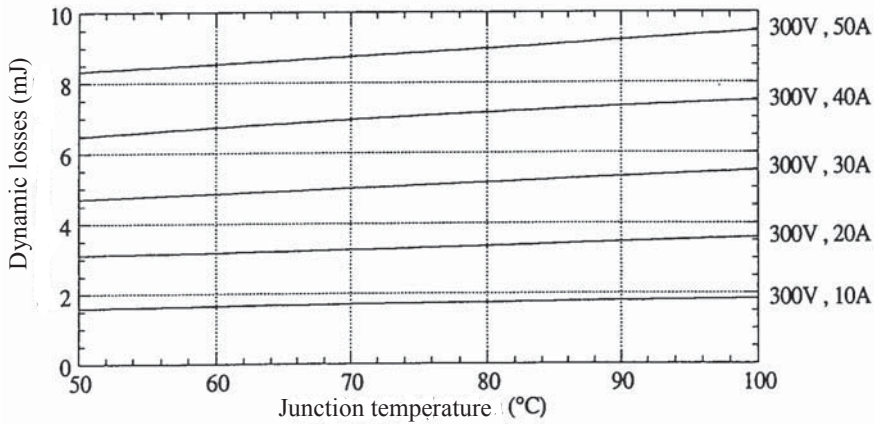


Figure 8.7. *Dynamic losses of a fast IGBT, depending on temperature*

We see that for a component IRGPC50F operating at 300 V, 50 A and 100°C, the losses are around 10 mJ per commutation. Such a component operating at 10 kHz dissipates, therefore, by switching a power of about 100 W, which is quite comparable to the energy dissipated during conduction when the conduction time and blocking time are equal.

8.2.1.4. *Conclusion*

The studies outlined above show that in modern electronic power components, for the voltages and currents considered, energies lost by switching and conduction are of the same order of magnitude: lost power to be evacuated on the rear panel of the silicon chip can reach 300 to 400 W/cm².

8.2.2. *Distribution of losses in the silicon chip*

A question is often asked: how are the losses located in the volume of silicon and, therefore, how is the temperature distributed within the component?

This is a complex issue because losses depend on temperature, which depends itself on cooling [FAR 94, HSU 96].

Losses may be developed in the vicinity of junctions, in load space areas, or in the area of voltage holding, creating for instance very localized hotspots. Measurements of component temperature were taken by an infrared camera, giving an accurate picture of the temperature at each point on the surface, thus establishing a temperature distribution map. The typical gap between the maximum and minimum temperature of a component of 1 cm^2 can reach 30°C.

Knowing and taking into account the allocation of losses and the mapping of temperature in silicon are both interesting and important when considering the electro-thermal behavior of a component, especially in the case of serial or parallel associations, but also for the behavior of components in transitional systems [MAN 97].

If the objective is the design of a cooler adapted to power electronics, able to dissipate 300 to 400 $W.cm^{-2}$, the precise location of losses is not a determining factor: the electronic power component will then be regarded as a surface, uniform, and homogeneous source of heat. The temperature of the chip, known historically by by the incorrect terminology "junction temperature" is defined as the average volume temperature at each point (x, y, z) of the volume of the chip.

$$T_j = \frac{1}{V_p} \iiint T(x,y,z)dV$$

where Vp is the volume of the chip.

8.3. Power electronic modules

8.3.1. *Main features of the power electronic modules*

The "bullet" of silicon in which the component is manufactured cannot be used alone, it must be mounted. Figure 8.8 represents a multi-layer cross-section view of a classic power module.

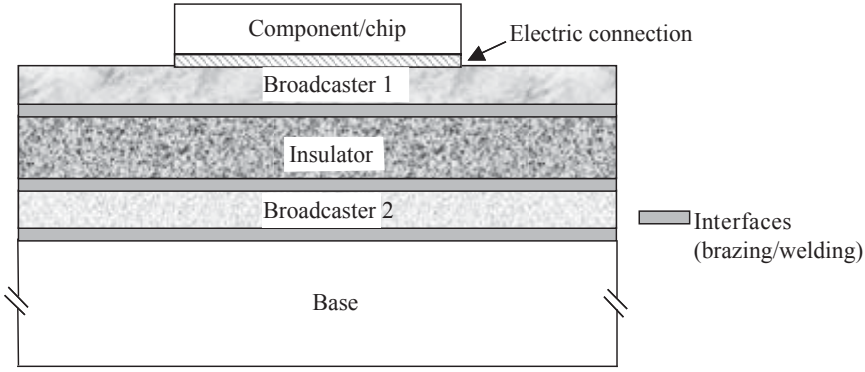


Figure 8.8. *Typical cross-section view of a power module*

As can be seen in Figure 8.8, the classic assembly consists of five layers of different materials, each is linked to the others by a very thin transition (brazing, welding), called an interface. Each of these layers has a particular role.

The first broadcaster (broadcaster 1) is directly under the chip. It must be a good electrical conductor, since it performs the electrical connection between the back of the chip and the outside, but must also be a good heat conductor: it takes part in the evacuation of the heat generated in the chip by allowing the flow of heat to spread and thus to benefit from the increased exchange surface. In the conventional modules, the broadcaster is copper, a material combining the two qualities.

Under the first broadcaster, there is electrical insulation. Its role is to electrically isolate the component from the rest of the module, and in particular from the associated cooler. It also provides electrical insulation between the various components of a single module when, for example, several IGBT are mounted in parallel. The material used must be a sufficiently strong insulator to withstand the voltages applied, but it must also have enough thermal conductivity to allow heat evacuation. Finally, it must have good combination capabilities with copper. The most efficient material seems to be the aluminum nitride (AlN), so that it is currently most often used in modules.

The second broadcaster which is a link with the base (commonly copper), enables good mechanical support, and its rear provides a link with the outside environment, especially with the heat exchanger.

All these materials are assembled together by welding or brazing. These joints have a low thermal conductivity, rather strongly degrading the ability of the module to dissipate the heat generated by the chip.

The module is covered with silicone and the whole is encapsulated in a plastic casing, with the exception of the rear of the basement which will exchange heat with the outside world.

8.3.2. *The main heat equations in the module*

The flow of heat through the module, from the chip to the rear of the basement, flows by conduction: heat transfer from one region to another is due to the temperature difference between these regions. As we have seen above, we consider that the component delivers a uniform heat flux. This flow P, represents the amount of heat crossing a surface per unit of time (expressed in watts):

$$P = dQ/dt$$

where dQ is the amount of elementary energy issued during an elementary time dt.

The heat density vector is also defined, φ, expressed in $W.m^{-2}$, characterizing for each point the direction and the intensity of the heat flux.

$$P = \iint_S \vec{\varphi}.\vec{n}.dS$$

and we write Fourier's law:

$$\vec{\varphi} = -k.\vec{\text{grad}}(T)$$

where k is the thermal conductivity of the material flowed. This is expressed in $W{\cdot}m^{-1}{\cdot}K^{-1}$.

By applying to an element of volume the first principle of thermodynamics and the law of Fourier, and making the assumption that the thermodynamics transformation is under constant pressure, the equation of the heat conduction is established for an isotropic body:

$$\rho C_p \frac{\partial T}{\partial t} = \text{div}(k\,\text{grad}(T)) + q$$

where ρ is the density, Cp the calorific capacity, k the thermal conductivity, and q the volume density of internal sources.

The thermal conductivity k depends on the temperature of the material, which does nothing to simplify the processing of previous equations.

For silicon: $k = 150\ W{\cdot}m^{-1}{\cdot}K^{-1}$ at 25°C, then it decreases as the temperature increases to reach $k = 100\ W{\cdot}m^{-1}{\cdot}K^{-1}$ at 125°C. To overcome this difficulty, one may assume a linear variation for a range of temperatures, or set an adapted constant value.

The importance of choosing materials with good thermal conductivity for the design of the module is clear, as is the negative influence of interfaces. Indeed, since the latter has low thermal conductivity, they are subject to strong temperature gradients that degrade the ability to evacuate the heat by conduction of the module.

To characterize the heat exchange that takes place between the chip and the base, we introduce the concept of thermal resistance, R_{th}, by analogy with the electrical resistance. It links the rise of temperature of the chip, T_j, with the ambient temperature T_a, for a dissipated power P. In permanent operation, it is given by:

$$R_{th} = \frac{T_j - T_a}{P}$$

This resistance is expressed in $K{\cdot}W^{-1}$. The more thermal resistance reduces, the more the chip produces a low heating due to dissipated losses.

Take for example the standard IGBT from Figure 8.8: the thermal resistance of the housing is $0.3K{\cdot}W^{-1}$. For a switching operation corresponding to a dissipation of 100 W, the heating of the chip obtained for a perfect cooling of the base would be 30°C.

In practice, the temperature control on the back side of the base is provided by a cooler, and is qualitatively characterized by a thermal resistance R_{thra}. For example, a standard air cooler has a resistance of $2K{\cdot}W^{-1}$. The IGBT, in the previous example, would, therefore, heat up to 230°C, which is not acceptable for a silicon chip. If we want to limit the heating to 60°C, for example, a cooler with a thermal resistance of less than $0.3\ K{\cdot}W^{-1}$ is required. It may be another air cooler, larger or better ventilated than the previous one.

Thus, we see that to take the current indicated by the manufacturer, an adapted cooler is required. More, the installation of a cooler whose thermal resistance would be $0.05\ K{\cdot}W^{-1}$, a water cooler for example, would allow the recommended current of 15 A to be exceeded, even doubled, for a temperature of 60°C [GIL 99, SCH 99].

The distribution of heat flow and temperature inside the module is completely conditioned by the heat exchange which will take place between the rear of the basement and the environment, i.e. ambient air or the associated cooler, the exchange being a convection.

8.3.3. *Cooling currently used for components of power electronics*

We have seen that postponement of housing the cooler is absolutely necessary, and may even be very beneficial in terms of increasing nominal current or operating frequency.

There are several kinds of coolers, but the principle is the same for all: submit a maximum exchange surface with a fluid that will absorb the heat. The exchange is by thermal convection, which is a process of transferring energy through the movement of molecules. We talk about natural convection when this movement is due to a simple difference in temperature within a space (the hot air going up, leaving room for cold air, for example) and forced convection when the movement is imposed by external action, by a pump or a fan.

This book does not look at the mechanics of fluids in a precise manner, but only to the heat exchange between the solid wall and fluid defined by a coefficient linking the heat flux φ through the wall and its temperature. The coefficient is called the coefficient of thermal exchange, h, and is defined as follows:

$$h = \frac{\varphi}{T\text{-}T_a}$$

This coefficient is expressed in $W \cdot m^{-2} \cdot K^{-1}$. We will return to this coefficient with more details in the following section.

In most cases, in power electronics, coolers are air type, forced convection, or water type. Water was chosen for its very good thermal capacity and its very simple use. It can be used in a closed loop, as long as the increase in temperature between input and output channels is controlled, which is very interesting in the case of embedded systems. On the other hand, water is not a good electrical insulator, and the establishment of an electrical insulator between the base and the cooler is often necessary. To avoid this insulation layer, which degrades the thermal performance of the housing, the water can be deionized. We can also make use of dielectric fluids (inert fluor, liquid nitrogen, etc.). Handling is cumbersome and low gain in terms of thermal performance compared to the design involving a layer of insulation makes their use unfavorable.

When the fluid is chosen, there are two possibilities for forced convection. It may be single or double phase:

– In the case of a single exchange phase, the fluid, liquid or gaseous, does not change phase during its circulation in the cooling device. A pump imposes a speed and its temperature rises as it progresses in the cooler. A compromise must be found between the speed of the fluid (including a best value which maximizes the evacuation of the heat) and the loss of pressure in the channels which are directly proportional to the cost and size of the pump.

– In the case of a double phase exchange, the heat absorbed modifies the state of the fluid which rises from the liquid state to a gaseous state: liquid and steam coexist [HEW 69]. Under the effect of heat, the temperature of the liquid rises to reach the saturation temperature, the liquid will then begin boiling. A secondary cooling system called the condenser cools the steam, thereby reducing fluid in the liquid state. These coolers have good performances, but they are not yet widely used in power electronics, mainly because of their design difficulty [MEY 98].

After going through the different techniques of coolers, we will speak now about a copper channel cooler, operated by forced convection water, single phase, because it is at present the cooling device most responsive to the needs of power electronics (e.g. size, performance, instrumentation) [TUC 81].

To increase the exchange surface (S_c), for a given chip surface (S_p), channels are designed in the copper base. In this case, the exchange surface Sc is defined as the sum of all channel surfaces: S_c = number of channels x length x width x height, i.e. $S_c = n \cdot l_c \cdot D \cdot L_y$. These parameters are defined in the schematic in Figure 8.9.

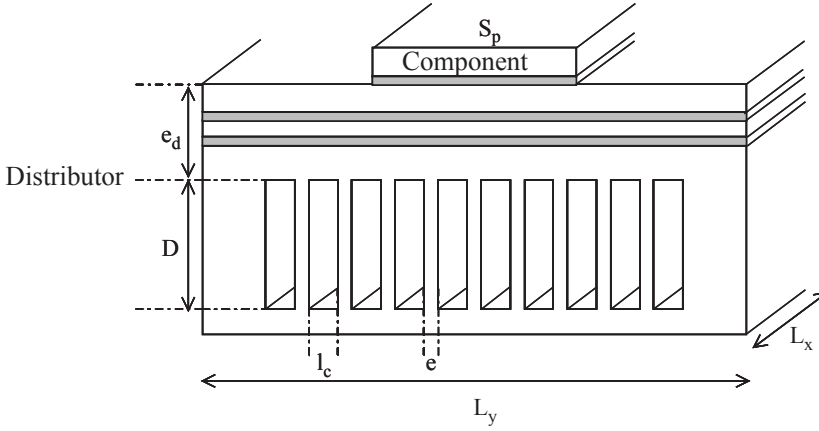


Figure 8.9. *Layout of a copper cooler including key geometric parameters*

The water flows through these channels. The performances are as follows: with a pump of 0.9 W power, the water flow is 1.3 $l \cdot min^{-1}$ for a loss of pressure of about 0.4×10^5 Pa. The cooler is able to evacuate a power corresponding to a reduced density on the component $350 W \cdot cm^{-2}$ for a junction temperature rise of 60°C. These results are obtained from a configuration where the chip and the water are not electrically isolated from one another. The cooler has been designed in LEG in collaboration with the CEA/GRETh and Alstom ([RAE 97] and [MEY 98]).

The performance of such coolers was further improved by C. Gillot who proposes double-sided cooling in his thesis [GIL 99].

This cooling method is very effective, but as we shall see, it has several drawbacks which we would like to overcome in this study.

As we have said previously, there are several layers of different materials between the chip and the cooler: silicon chip, copper broadcaster, AlN of insulation and different solders (Figure 8.8), and finally the copper cooler. All these interfaces deteriorate thermal performance and generate mechanical fatigue: the different materials have different thermal behaviors since they do not have the same coefficient of thermal expansion, thereby reducing the lifetime of the system by thermal fatigue.

In addition, the cooler is carried out in a copper base whose weight can be a problem, especially for use in embedded systems.

Finally, with this type of cooler, as with coolers of older generations: the component and the cooler are designed independently of one another, limiting the manufacturer of component for the level of the maximum current; and thus excluding the hypothesis of a collective achievement of an integrated converter, where you could find in a single bloc, the power part, the command and the cooler.

For these reasons, and especially the latter, this question was proposed as the subject for a thesis, and a "*full silicon*" type solution was suggested.

8.3.4. *Towards an "all silicon" approach*

The design of a full silicon cooler has been studied in the thesis of [PER 01]. Indeed, this new approach can solve a number of problems encountered during the implementation and use of copper micro-coolers. Although from a purely thermal point of view silicon is less efficient than copper (its thermal conductivity is almost two and half times lower ($150 W \cdot K^{-1}$ compared to $360 W \cdot K^{-1}$), it nevertheless

presents several advantages providing for consideration a micro-cooler with good performances in several respects.

First, the mechanical strength of silicon and the methods of engraving allow the creation of channels and fins whose critical dimensions (width, depth, etc.) are much smaller than those supported by copper. This allows a considerable increase in the exchange surface available for a given chip surface. Although it is more difficult to handle, being more fragile, the silicon micro-cooler has the advantage of being lighter than copper.

However, the greatest advantage of this cooling technique is without doubt that it involves the use of a single material: the chip and its cooler are both in silicon. Either the chip is carried on a silicon base on which channels will have been etched, or channels are made directly into the back of the chip. Indeed, the achievement of micro-coolers is fully compatible with a classic CMOS technology. All this leads to two positive important advancements: the chip can be delivered directly from the white room with its integrated and adapted cooler, and all problems of thermal fatigue are eliminated at the same time as with the different solders that are usually inserted between heating and cooling sources. This is also a way to consider the components of high integration we are talking about. Many works are underway to achieve this [SAN 97].

Finally, as we said earlier, the establishment of a dielectric layer between the chip and the refrigerant fluid, in the case of copper, degrades thermal performance significantly. Here, the silicon can again provides an improvement: the electrical insulation made by insertion of a thin layer of silicon oxide (Figure 8.10). This oxide has two advantages: it is a very good dielectric (low thickness is necessary) and its coefficient of thermal expansion is substantially the same as silicon: its presence does not therefore introduce significant thermo-mechanical constraint.

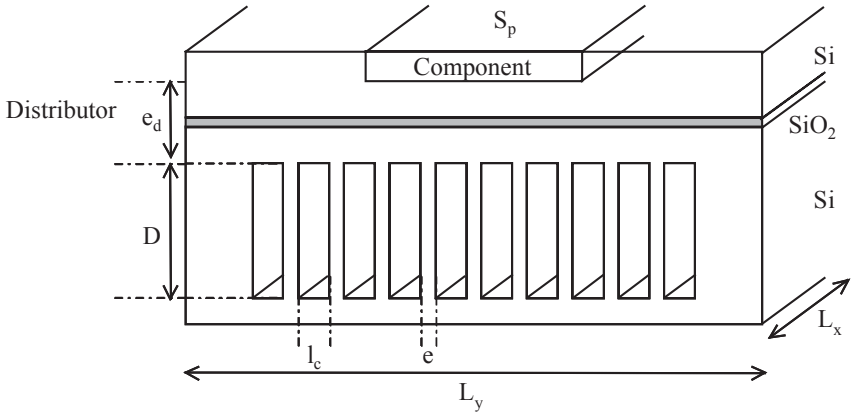


Figure 8.10. *Isolation of the electrical part from the thermal part by incorporating a layer of silicon oxide (of a few microns)*

To illustrate these remarks, therefore, we will study the cooling of a single chip, with the assumptions made above: the flow of heat is considered as an injection surface of heat in the cooler. The principle is water forced cooling, with mono-phase convection.

To give an idea of the size of micro-coolers, here are the magnitudes of each geometric parameter (Figure 8.10):

– D: depth of a channel: 400 to 800 μm;
– lc: width of a channel: 80 to 150 μm;
– e: width of a wing: 80 to 150 μm;
– Lx: length of a channel: 2 cm;
– Ly: width of a grid of channels: 2 cm;
– n: number of channels: 60 to 130.

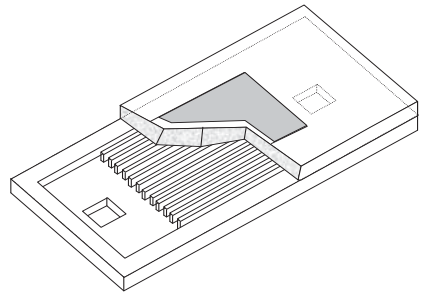


Figure 8.11. *Schematic of a cooler created in silicon*

Figure 8.11 presents a cross-section view of the cooler.

The fluid is water, chosen for its good thermal performance and its ease of use. We summarized in Table 8.1 thermal and hydraulic constants of water, coolant fluid used in this study.

Density ρ	995 $kg{\cdot}m^{-3}$
Viscosity μ	0.000651 $kg{\cdot}m^{-1}.s^{-1}$
Thermal conductivity kl	0.628 $W{\cdot}m^{-1}{\cdot}K^{-1}$
Calorific capacity Cp	4.178 $J{\cdot}kg^{-1}{\cdot}K^{-1}$

Table 8.1. *Thermal and hydraulic constants of water*

8.3.5. *Conclusion*

We have seen that power components are becoming more efficient in terms of speed, which compared with their losses appear to be constant or even increasing. In addition, compacting makes cooling more difficult. Significant progress has been made on the coolers that currently have good performances. However, designs of components and coolers remains independent, which is harmful. An approach integrating the cooler module is an attempt to answer this problem, with the "all silicon" approach being a step further in this direction.

8.4. Laws of thermal and fluid exchange for forced convection with single phase operation

8.4.1. *Notion of thermal resistance*

As we have already mentioned, the thermal resistance is analogous with the electrical resistance: where the electrical resistance connects the current to the fall of voltage between its terminals, thermal resistance establishes a link between the flow of heat entering a system and the temperature difference between two points of the system, hence the "thermal Ohm" law recalled here:

$$Rth = (Tj - Ta)/P$$

In our case, the evacuation of the heat is carried mainly by the cooler (radiation is neglected). The total thermal resistance is the sum of three terms:

– thermal resistance due to heat conduction through the R_{diff} of the broadcaster; the broadcaster as part located between the chip and the top of the channels (Figure 8.10). It is made from one or more materials as previously mentioned;

– convection resistance reflecting the exchange between the channel walls and the fluid, R_{conv}; and

– capacitive resistance representing a rise of temperature of the fluid between the channel input and output, R_{cap}.

8.4.1.1. *Thermal resistance of diffusion, R_{diff}*

Two cases are different in regard to the broadcaster resistance: the heat flow is unidirectional (resistance with one dimension), or it is two-dimensional (resistance with two dimensions). We define here two surfaces (Figure 8.12):

– the chip surface, S_p:

$$S_p = L_{px} \cdot L_{py}$$

– and the surface of the broadcaster cooler's, S_d:

$$S_d = L_{dx} \cdot L_{dy}$$

where L_x and L_y are the dimensions of the chip and broadcaster.

The first case is relevant when the component and the cooler have the same size ($S_p = S_d$) and in the second when the cooler is larger than the component ($S_p < S_d$).

8.4.1.1.1. Dissemination resistance with one dimension

In the simple case of a single layer broadcaster, i.e. made of a single material, this resistance is the easiest to define, since it is only to describe the passage of heat flow through a uniform material (Figure 8.12.a):

$$R_{diff} = \frac{e_d}{k_d . S_d}$$

where e_d is the thickness of the broadcaster, k_d is the thermal conductivity expressed in $W \cdot K^{-1} \cdot m^{-1}$, and S_d the surface flowed by the flux.

In this case, it is easy to reduce the importance of this resistance by reducing the thickness of the broadcaster, within the mechanical limits of the system, of course.

When the broadcaster is made up of several layers, we add the dissemination resistances of each layer:

$$R_{difftotal} = \sum_{i=1}^{n} R_{diffi} = \sum_{i=1}^{n} \frac{e_{di}}{k_{di} . S_d}$$

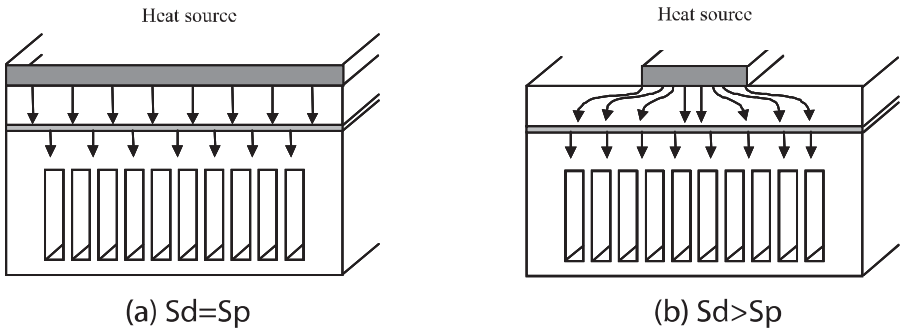


Figure 8.12. *a) Unidirectional heat flow, b) dissemination of heat flow*

8.4.1.1.2. Dissemination resistance with two dimensions

Let us study now when the heat flow is two-dimensional (Figure 8.12b). This occurs when the component is smaller than the cooler, and is amplified when the broadcaster incorporates a thermal barrier. As we have said before, to achieve a cooler where the silicon component and the fluid will be electrically isolated, we

will need to integrate a layer of silicon oxide inside the broadcaster. Due to its low thermal conductivity, this layer will cause heating, but it will also "slow down" the flow of heat and thus force it to disseminate in the area above it. The barrier is a negative result of the thermal cooler's performance, but a well-optimized design can reduce this defect. Indeed, if the surface of the cooler is sufficient and if the position of the insulation layer and its thickness are carefully selected, the exchange can be improved by the simple fact that the flow of heat encounters a bigger surface than in the cases of a one dimensional flow. We can now see that a compromise is required when adding an electrical insulator, between its thickness, its position in the broadcaster and the surface of the cooler. A more complete modeling must be effectuated for each configuration.

8.4.1.2. *Thermal resistance by convection, R_{conv}*

As we have said, convection means the exchange between the walls of channels and fluid. We defined above the concept of heat exchange coefficient h. The convection thermal resistance is inversely proportional to this coefficient:

$$R_{conv} = \frac{1}{h.S_c}$$

where S_c is the surface of heat exchange, i.e. the surface of the channel walls.

The difficulty in characterizing the heat convection is to determine the value of coefficient h. It depends on many parameters such as the convection mode (natural or forced), the geometry of the cooler (plan, with rectangular or circular channels, etc.), the nature of the flow (laminar or turbulent) and its thermal and hydraulic operation. It can be seen, considering the number of parameters, that there is no exact formulation of this coefficient for all cases. In general, its value is taken into empirical tables.

It is vital that the thermal resistance be improved to enhance the overall performance of the cooler. There are two methods using parallel to achieve the reduction of this thermal convection resistance: increasing the exchange surface S_c adapting critical dimensions of channels and fins, and increasing the thermal exchange ratio amending the form of channels, the flow system, and so on.

8.4.1.3. *Capacitive thermal resistance, R_{cap}*

This thermal resistance varies slightly from the other two: the first two take into account differences in temperature in the flow of heat plane, the latter is on the rise

in temperature of the fluid between the channel inputs and outputs, i.e. in a plane perpendicular to the flow of heat. This temperature rise is due to the amount of heat absorbed by the fluid during its passage. It depends on the nature of fluid, its calorific capacity, and the flow imposed on it:

$$R_{cap} = \frac{1}{2.m.C_p} = \frac{T_m - T_e}{P} = \frac{T_S - T_e}{2P}$$

In this equation, m is the mass flow of fluid, C_p its calorific capacity, T_e temperature of the fluid at the channel entrances, T_s the temperature of the fluid at the channel exits, and T_m the average of these two temperatures.

The thermal resistance must be limited especially in the structure we would like to use, the closed loop. In this case, a secondary cooling system is necessary to ensure the fluid entering the channels is always at the same temperature T_e. If the temperature of the fluid at the exit of the main cooler is limited, the secondary cooling circuit is simpler and less expensive.

8.4.1.4. *Square thermal resistance R_c*

To facilitate comparisons between the performances of different micro-coolers, designers are accustomed to using a thermal resistance per area unit, which they call square resistance R_c, expressed in $K \cdot W^{-1} \cdot m^{-2}$. We note for example:

$$R_{ctot} = R_{tot} \times S_p$$

with S_p, the surface of the heating source.

8.4.1.5. *Total square thermal resistance, R_{ctot}*

The total square thermal resistance is the sum of three square resistors:

$$R_{ctot} = R_{cdiff} + R_{cconv} + R_{ccap}$$

We can now see all the compromises that will be needed to reduce total thermal resistance without increasing too many other constraints: choice of the thickness of the broadcaster between dissemination and the thermal barrier; compromise between the reduction of critical dimensions and mechanical constraints; compromise between an increased rate of flow of the fluid, for a reduced rise in temperature, and a minimum loss of pressure; choice of flow system of the fluid, etc. All these issues will be resolved during the global optimization of the cooler.

8.4.2. *Laws of convective exchanges from a thermal and hydraulic point of view: the four numbers of fluids physics*

In the preceding section, we saw that the convection part is essential to the performance of coolers. In this part, we will revisit the laws calculating the coefficient of thermal exchange h and characterizing the fluid flow (loss of pressure, nature of the flow, etc.).

These laws are expressed in terms of four dimensionless numbers traditionally used by specialists.

8.4.2.1. *The Reynolds number*

The flow can be laminar or turbulent. In the first case, the fluid flows in the form of nets parallel to the walls; in the second, the concept of a net no longer exists, and the movement of fluid particles is uncertain.

To find the flow system, this Reynolds number, Re, must be incorporated, which depends on the density of the fluid ρ, its viscosity μ and the hydraulic diameter of the channels, D_h, as follows:

$$Re = \frac{\rho.v.D_h}{\mu}$$

with $D_h = \frac{4.s}{p} = \frac{D.l_c}{2.(D + l_c)}$ in the case of rectangular channels,

with s and p respectively the section and perimeter of the channel, D its depth and l_c its width.

This Reynolds number defines the transition from a laminar flow to a turbulent flow. The value corresponding to this transition is well established for channels and micro-channels (flow is laminar if Re < 2,300, otherwise turbulent, for channels of dimensions in the order of a millimeter). However, in the case of micro-channels (critical dimensions of about 100 microns or less), this limit is not clearly known. In literature, the hydraulic designers evaluate it, according to the methods used, from Re = 400 to Re = 5,000 ([MOH 97, PEN 94, ZHU 97]). That is why, as a first step, we will not make any assumption on the flow system instead we will try to determine it by a more experimental approach.

8.4.2.2. *The Prandtl number*

The flow can be established thermally and/or hydraulically. We talk about thermally or hydraulically established system, when the temperature profile, or the speed of the fluid in the channel no longer depends on its position along the channel. The distance between the channel entrance, and the position from which the profiles no longer evolve is called length of establishment. The Prandtl number, Pr, gives information on the establishment of flow. This dimensionless quantity is defined by:

$$\mathrm{Pr} = \frac{\mu C_p}{k_l}$$

where μ is the viscosity of the fluid, C_p its calorific capacity and k_l its thermal conductivity.

For the design of coolers, the flow is always regarded as being thermally and hydraulically established. This assumption is necessary in order to facilitate the stationary state design. Knowing that the heat exchange is still slightly better when the flow is not established, if this hypothesis is not verified, the design result will simply underestimated compared to reality.

8.4.2.3. *Friction coefficient and pressure losses*

When considering a flow of fluid, there is also the loss of pressure between input and output of channels. This loss of pressure depends on the coefficient of friction C_f, speed v, density of the fluid ρ, length of the channels L, and their hydraulic diameter D_h, such that:

$$\Delta P = \frac{4.C_f.L}{D_h.}.\rho\frac{v^2}{2}$$

The coefficient of friction C_f, can be calculated by two empirical formulae, one for a laminar flow system:

$$C_f = \frac{4.7 + 19.64\,G}{R_e} \quad \text{with} \quad G = \frac{\left(\frac{D_h}{l_c}\right)^2 + 1}{\left(\frac{D_h + 1}{l_c}\right)^2}$$

where G is a dimensionless parameter determined experimentally, taking into account the form factor in the case of rectangular channels.

For a turbulent flow system:

$$C_f = (0.0929+1.01612\ Dh/L).Re^{-0.268-0.3193Dh/L}$$

8.4.2.4. *Nusselt number*

This number depends on the channel geometry and the nature of the fluid flow. In the laminar system and where the flow is established thermally and hydraulically, it is possible to calculate the Nusselt number analytically, as long as the speed profile in the channels is known, and then the heat equation is solved. In the case of cylindrical channels, it is relatively easy, but for more complex sections, such as rectangles, it quickly becomes complicated, and we prefer then to determine the Nusselt number empirically [TAI 89]. To this end, there are an array of experimental values of the Nusselt number according to ratios in formed channels [KAY 80]. It is possible, as demonstrated by [BEJ 84] to obtain from these experimental values, an analytical equation of Nusselt according to the geometric parameters of the channels. Two cases are distinguished:

– the four walls of the channels are involved in the heat transfer;

$$Nu = -1.047+9.326G$$

– the fourth wall, the bottom of the channel, is adiabatic;

$$Nu = -14.859 + 65.623\ G – 71.907\ G^2 +29.384\ G3$$

These formulae are valid when we make the assumption that the flow of heat is uniformly shared on the walls involved in the exchange.

In the turbulent system, the Nusselt number is less sensitive to the geometry of the channels. There are many correlations to approach analytically approaching the Nusselt number. We consider those of [GNI 76] that are valid irrespective of the boundary conditions on the walls:

$$Nu = 0.0214.\ (Re^{0.8} – 100).Pr^{0.4},\ \text{when}\ 0.5 < Pr < 1.5\ \text{and}\ 10000 < Re < 5.10^6$$

$$Nu = 0.012.\ (Re^{0.87} – 280).Pr^{0.4},\ \text{when}\ 1.5 < Pr < 500\ \text{and}\ 3000 < Re < 10^6$$

The Nusselt number is directly linked to the coefficient of thermal exchange h by the formula:

$$Nu=\frac{h.D_h}{k_l}$$

This formula is valid in the case of rectangles, with $\delta = D_h/lc > 1$.

Depending on the nature of systems, we can draw curves $h(\delta)$:

$$h(\delta) = \frac{k_l . Nu(G(\delta))}{D_h(\delta)}$$

We note, while the coefficient of heat exchange h is growing with δ in the case of a laminar flow (Figure 8.13), it decreases in the case of turbulent flow (see Figure 8.14).

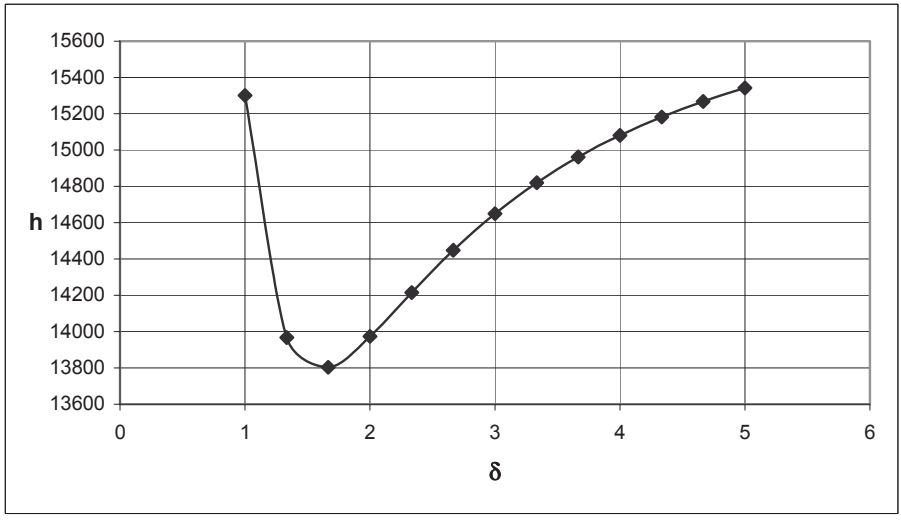


Figure 8.13. *Change of the coefficient of thermal exchange h according to the ratio $\delta = D_h/lc$ (depth divided by channel width) in the case of laminar flow*

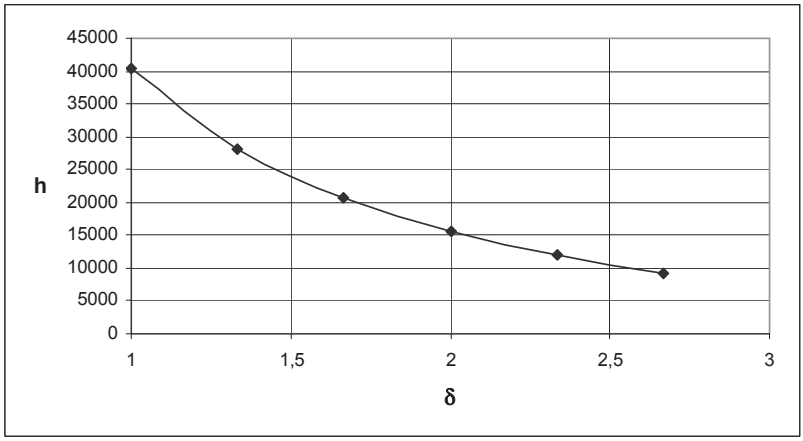


Figure 8.14. *D/lc change of the heat exchange coefficient h according to the ratio $\delta = D_h/lc$ (depth divided by channel width) in the case of a turbulent flow. Curve is limited to <2.5 because for higher values, flow becomes laminar*

There are several other formulae giving Nusselt values, which may be multiplied by 2, [BEJ 84, GNI 76, KNI 92, TAI 89]. All these formulae are provided with an error of 20%, and for areas corresponding to different Reynolds numbers.

$$Nu = 0.027.Re^{0.8}.Pr^{0.33}$$

The Nusselt number is directly linked to the square convection resistance since:

$$R_{convc} = \frac{1}{h} = \frac{D_h}{k_1 Nu}$$

8.4.2.5. *Conclusion*

In this chapter, we recalled key relationships that can aid the design of a micro-channel cooler with a coolant fluid. The more comprehensive calculation is done in the referenced bibliography. In the next chapter, we will develop the calculation of the distribution of temperature in the module, the cooler being represented by the exchange ratio h.

8.5. Modeling heat exchanges

To carry out this modeling, analytical methods are typically involved, as semi-analytical or digital methods. Below, we describe the two last approaches on examples treated within a research group.

8.5.1. *Semi-analytical approach*

Calculating of temperature distributions or heat flows in the operating devices, is based on solving the equation of heat in the three dimensions of the devices volume [PET 95, SZE 97]. However, solving this equation is generally not easy when one proposes to take into account the boundary conditions that are necessary for describing the realistic operating conditions that apply to this device for cases that have immediate practical interest. The heat equation is a partial differential equation. The analytical methods of solving the latter are essentially based on two techniques that can reduce the problem with three dimensions to a problem with one dimension. There are:

– methods based on the use of Green's functions associated with real sources and image sources; and

– methods based on the use of integral transformations adapted to the lateral limit conditions set for the problem.

8.5.1.1. *The methods based on the use of integral transformations.*

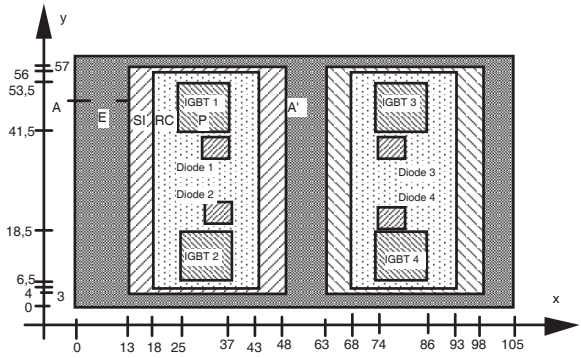
There are scopes for preferential application of each of these methods depending on the problem to be addressed. Thus, a problem where lateral limit conditions have little importance is easy to deal with using the first method (Green's functions), while the second method (transformation) is more suited for solving problems where the lateral limit conditions play a crucial role.

Whatever method is adopted, the analytical solution is finally obtained in the form of a series involving more or less terms and, in cases of practical interest, can only be operated with numerical calculation. That is why we prefer to use the term semi-analytic method. In the following, we will show how it is possible to apprehend with realism, the calculation of distributions of temperature and heat flux, based on a semi-analytical method using the Fourier transformation. The structure on which this method can be applied is the already complex hybrid power module with several chips. The time needed to calculate the distribution of temperature or heat flow through the proposed method can be surprisingly short. For simplicity and

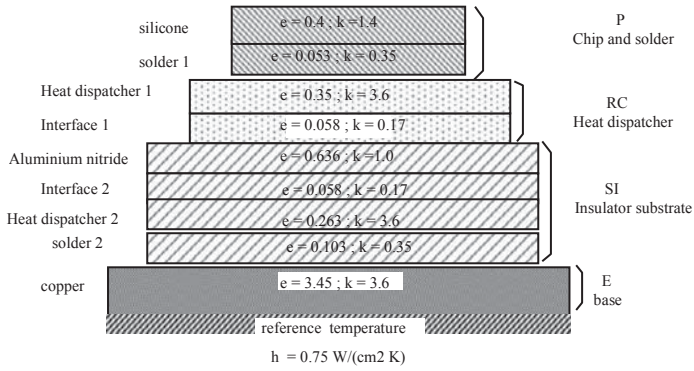
brevity, however we will reduce our demonstration, to the semi-analytic calculation of distributions of temperature obtained under the static system of power dissipation.

8.5.1.2. *Stating the problem – key assumptions*

Figure 8.15 provides a schematic overview of top views and cross-section views of a hybrid power module with IGBT and diodes. As shown in Figure 8.15b, it is assumed that this module is cooled in an effective manner on its underside because of the large power dissipation which is often characteristic of this device in normal operation [BEL 97].



(a) Top view (all sizes in mm)



(b) Cross-section view following AA' (e in mm, k in $W \cdot cm^{-1} \cdot K^{-1}$)

Figure 8.15. *Schematic view of a hybrid power module*

From the thermal point of view, this module can be regarded as an assembly of various layers of rectangular form materials, characterized by different thermal conductivities and diffusivities. In this assembly we must also not underestimate the role of interfaces between layers, which even of practically negligible width, may have, because they are non-ideal, a considerable weight in the thermal behavior of the whole. If one considers the flow of heat dissipated in the active areas of the components, this will be in a preferred direction "z" while allowing the flow of heat to flourish more or less locally following the other two directions (x and y), depending on the flowed materials. It is assumed that the underside of the assembly exchanges heat with a heat sink, maintained at a temperature of reference. This exchange of heat is characterized by a convective coefficient of exchange, h, expressed in $W \cdot cm^{-2} \cdot K^{-1}$ and whose dimension is identical to the heat conductance per area unit, g, that characterizes the heat exchange between two adjacent layers separated by a non-ideal thermal interface.

If the cooling established at the bottom of the structure is really effective (forced air convection or circulation of a coolant liquid), one can ignore the heating power evacuated from the top and the side edges of the structure by natural convection and radiation. These last two mechanisms for the exchange of heat are indeed characterized by exchange factors that are very low if the temperature of the structure remains within acceptable limits in practice. In these circumstances, we may make a simplifying assumption, considering that all sides in contact with the environment are adiabatic, with the exception of the lower side which is in contact with the heat sink.

As the thickness of active zone (100 microns) is generally very small compared to the total thickness of the pile, it is convenient to consider that dissipated heat is on a surface rather than in a volume. This allows us to use a simplified form of the equation of heat, and impose the flow of heat as a limit condition on the surface at the limit of active zones, which are located in the immediate vicinity of the upper surface of the pile.

Moreover, if we considers the side view given in Figure 8.15b, it may be noted that a detailed analysis of the thermal behavior of the entire structure must take into account the fact that the latter is divided into parallelpiped blocks, each of them including multiple plane layers interfaced one over the other. Thus the analysis of the structure outlined in Figure 8.16 is used to identify 13 blocks which are:

– the eight chips and underlying welding (block "P");
– the two dispatchers of heat (blocks "RC");
– the two insulating substrates (blocks "SI");
– the copper base (block "E").

The mathematical formalization of the calculation of temperature across a structure as described in Figure 8.15 must therefore be divided into two stages:

– calculating the distributions of temperature and flow in each of the blocks which constitute the complete structure;

– taking into account the thermal interaction between various blocs according to their relative positions.

8.5.1.3. *Principle of calculating of temperature and flow distribution in a block*

Figure 8.16 shows the mathematical problem of heat flowing in a block [LET 93]. The distribution of heat flow is assumed to be known on the upper side (in the plane $z = 0$) and the distribution of temperature is assumed to be known on the underside of the block (in the plane $z = z_n$). We must first calculate the distribution of temperature at the top of the block, and the distribution of heat flow to the lower surface. When both values are determined, we can remove one or the other of these quantities in any internal plan of the block if necessary.

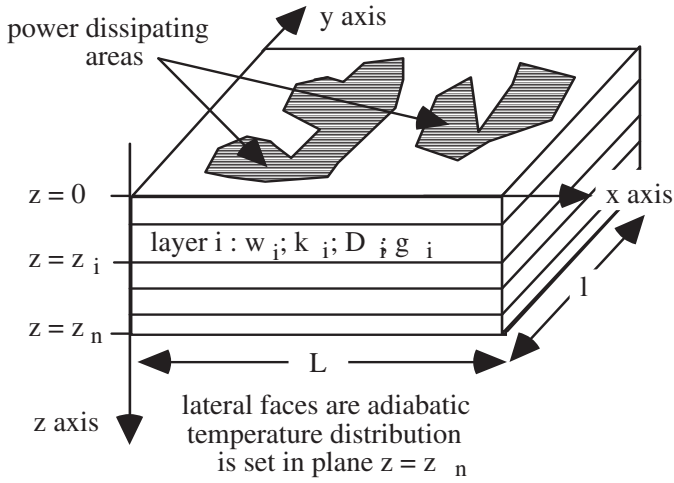


Figure 8.16. *Geometric and thermal description of a multi-layered block*

If the assumptions made above are correct – the flow of heat is imposed on the upper side of the block and the distribution of temperature is defined on the lower

surface, with the other sides of the structure being adiabatic – we must solve the following system of equations:

$$\begin{cases} \text{Heat equation in layer i: } \nabla^2\theta_i = 0 \\ \text{Thermal conductivity at interface i: } k_i \left.\frac{\partial\theta_i}{\partial z}\right|_{z=z_i} = k_{i+1} \left.\frac{\partial\theta_{i+1}}{\partial z}\right|_{z=z_i} \\ \text{Thermal conductivity at interface i: } \theta_{i+1} = \theta_i + \frac{k_i}{g_i}\left.\frac{\partial\theta_i}{\partial z}\right|_{z=z_i} \\ \text{Boundary condition in z = 0: } \mathrm{p(x,y)} = -k_1 \left.\frac{\partial\theta_i}{\partial z}\right|_{z=0} \\ \text{Boundary condition in z = z}_\mathrm{n}\text{: } \theta_n(x,y,z_n) = \theta_{ref}(x,y) \\ \text{Boundary condition on lateral sides: } \left.\frac{\partial\theta_\mathrm{i}}{\partial \mathrm{x}}\right| = 0 \text{ , } \left.\frac{\partial\theta_\mathrm{i}}{\partial \mathrm{y}}\right| = 0 \text{ , } \forall \mathrm{i} \end{cases}$$

Using an appropriate linear transformation, we can transform in each layer the Laplace equation into a regular differential z equation. Given the boundary conditions on the lateral sides, this transformation is in this case turned into a double cosine transformation which must be applied to distributions of temperature $\theta_i(x, y, z)$ [DOR 96] as follows:

$$\Theta_i(n_x, n_y, z) = \frac{1}{Ll}\int_0^L\int_0^l \theta_i(x,y,z)\cos\left(n_x\frac{\pi}{L}x\right)\cos\left(n_y\frac{\pi}{l}y\right)dxdy$$

Laplace equations in each layer i are transformed into:

$$\frac{d^2\Theta_i}{dz^2} = m^2\Theta_i \quad \text{with} \quad \mathrm{m}^2 = \left(n_x\frac{\pi}{L}\right)^2 + \left(n_y\frac{\pi}{l}\right)^2$$

where n_x and n_y are wave numbers, with theoretical values between 0 and infinity, and m can be defined as a spatial pulse.

As the double cosine transformation is linear, all conditions of continuity and boundary conditions defined for distributions of temperature and flow also apply to transformations of these distributions. The solution of the equation for the layer i can be written:

$$\Theta_i(m,z) = C_i(m)e^{+mz} + C'_i(m)e^{-mz}$$

For a solution, we should in principle calculate the coefficients $C_i(m)$ and $C'_i(m)$ for each layer i using the continuity and boundary conditions equations imposed in $z = 0$ and $z = z_n$. This provides the expression of the transformation of temperature $\Theta_i(n_x, n_y, z)$ or flow $\Phi_i(n_x, n_y, z)$ being determined in the plane where we want to calculate the solution, this expression can be further evolved by the following reverse transformation:

$$\theta_i(x,y,z) = \frac{4}{Ll}\sum_{n_x=0}^{\infty}\sum_{n_y=0}^{\infty}\Theta_i(n_x,n_y,z)\frac{\cos\left(n_x\frac{\pi}{L}\right)\cos\left(n_y\frac{\pi}{l}\right)}{\left(\delta_{n_x,0}+1\right)\left(\delta_{n_y,0}+1\right)}$$

In practice, the direct and inverse transforms will be discrete and carried out by numerical methods, which as *a priori* excludes the possibility of infinite wave numbers. A highest value must be retained for wave numbers depending on the maximum spatial resolution you want to deal with. For this limitation, one can directly apply Shannon's sampling theorem. For example, if we seek to obtain a spatial resolution equal to Δx and Δy following x and y respectively, the maximum wave numbers n_{xmax} and n_{ymax} should verify the following inequalities:

$$n_{\text{xmax}} \geq 2\text{L}/\Delta\ ,\ n_{\text{ymax}} \geq 2\text{l}/\Delta.$$

8.5.1.4. *Calculation of temperature or flow distribution in a block*

In practice, there is no particular need to look for direct expressions of coefficients $C_i(m)$ and $C_i'(m)$ in each layer i. And it may be noted that these factors can be eliminated by involving transformed distribution expressions of temperature and flow ((Θ_{iE}, Φ_{iE}) at the entrance to the layer i (at $z = z_{i-1}$) and (Θ_{iS}, Φ_{iS}) at the output of the layer (z = zi). You can then write the relationship matrix as follows:

$$\begin{pmatrix}\Theta_{iE}\\ \Phi_{iE}\end{pmatrix} = \left[\text{A}_\text{i}(m)\right]\cdot\begin{pmatrix}\Theta_{iS}\\ \Phi_{iS}\end{pmatrix} \text{ with } \left[\text{A}_\text{i}(m)\right] = \begin{bmatrix}\cosh(me_i) & \dfrac{\sinh(me_i)}{mk_i}+\dfrac{\cosh(me_i)}{g_i}\\ mk_i\sinh(me_i) & \dfrac{mk_i}{g_i}\sinh(me_i)+\cosh(me_i)\end{bmatrix}$$

where $[\mathbf{A_i}(m)]$ is the chain matrix (according the theory of quadrupoles) representative of the layer *i* which gives distributions of temperature according to distributions at the output of layer *i*.

The major advantage of the introduction of formalism to the theory of quadrupoles at this level is to treat a block with any number of layers without difficulty. It should be noted that for a number of layers equal to *n* whose thickness and thermal conductivities are known, we can link the transformed entry distributions (Θ_S, Φ_S) to those of the exit (Θ_S, Φ_S), by a chain matrix $[\mathbf{A}(m)]$ that we calculate directly, using the product of elementary chain matrices whose coefficients are calculated for each layer in the following order:

$$[\mathbf{A}(m)] = [\mathbf{A_1}(m)] \cdot [\mathbf{A_2}(m)] \cdot \ldots\ldots \cdot [\mathbf{A_n}(m)]$$

Such a procedure offers the advantage of guaranteeing a perfect numerical calculation, even if the calculation of the chain matrix of a complex structure, formed by a succession of many layers and for very large wave numbers is required.

For example, suppose we want to calculate the distribution of temperature at the surface of the block where the distribution of dissipated power is known, and where the distribution of temperature is imposed on the underside of the block. By applying the previous formalism of quadrupoles to the thermal problem, it becomes:

$$\begin{pmatrix} \Theta_E \\ \Phi_E \end{pmatrix} = [\mathbf{A}(m)] \cdot \begin{pmatrix} \Theta_S \\ \Phi_S \end{pmatrix} \Rightarrow \begin{cases} \Theta_E = \dfrac{1}{A_{22}(m)} \Theta_S + \dfrac{A_{12}(m)}{A_{22}(m)} \Phi_E \\ \Phi_S = \dfrac{1}{A_{22}(m)} \Phi_E - \dfrac{A_{21}(m)}{A_{22}(m)} \Theta_S \end{cases}$$

where [A(m)] is the chain matrix of the complete block and $A_{ij}(m)$ designate the coefficients of this chain matrix.

The procedure for practical calculation will be facilitated and will proceed as follows:

1) The transformations of θ_S and ϕ_E are made digitally by applying a Fast Fourier Transform algorithm, which allows us access to the *m* spectrum of these quantities.

2) The output we want to calculate is established using the adequate relationship of the *m* spectrum.

3) The inverse transformation of this new m spectrum is proceeded, and this provides the distribution of the sought after quantity.

Such a procedure allows for the quick calculation of temperature or flow map, even in cases where a high spatial resolution is required. For example it takes between 15 and 20 seconds to calculate a temperature or flow map of 128 by 128 points [DOR 97]. It should be noted that in many problems, the spatial resolution of the calculation in a block may be limited, thus accelerating the calculation procedure speed. We can of course, without any particular difficulty, complicate the calculation process to access the distributions of temperature or flow in a plan located anywhere in the block. In practice, it may be particularly interesting to calculate the distributions of temperature at the interfaces between layers so as to reveal the flow of heat on each layer.

8.5.1.5. *Extension of calculation to a complex assembly of blocks, s*

Regardless of the complexity of the defined block assembly, we can show that the procedure of calculation can be reduced to the implementation of a recurring basic procedure, which is to look for the flows at the interface between two superimposed blocks, as shown in Figure 8.17.

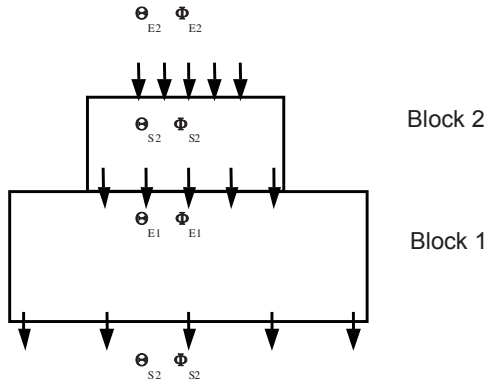


Figure 8.17. *Schematic view of a basic assembly of two blocks*

The search for the distribution of flows to the interface between blocks 1 and 2 is iterative and implements a relaxation algorithm for which a simplified chart is given in Figure 8.18.

As shown in Figure 8.18, we can see that the algorithm uses a weight coefficient set between 0 and 1 whose choice is crucial for two reasons:

– it is often necessary to obtain the convergence of iterative processes;

– it sets the speed of convergence of iteration.

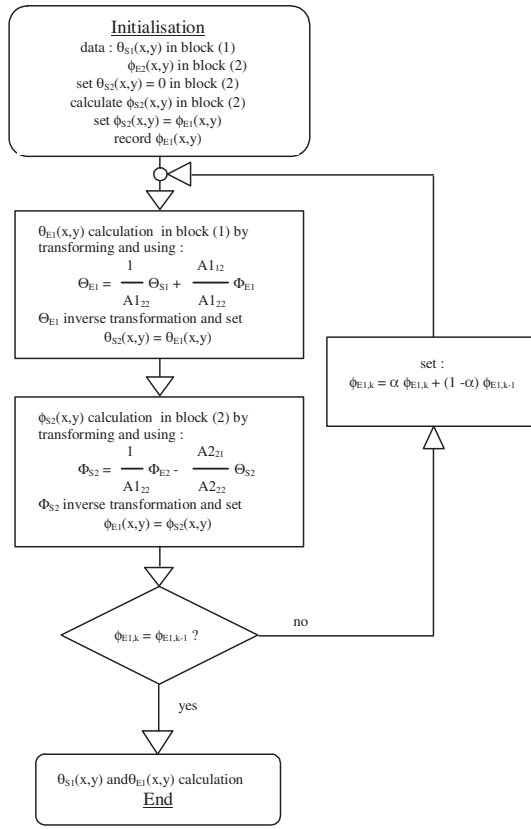


Figure 8.18. *Simplified iterative procedure for 2 blocks*

The practice of numerical calculation shows that there is no convergence problem during assembly, such as the upper block (2) has a lower conductance than the lower block (1), and in these conditions, the coefficient may be made equal to 1, leading to the fastest convergence. Now, when block (2) is a better heat conductor than block (1), the choice of a weight coefficient equal to 1 leads to a divergence in the calculation. The convergence can be restored if we reduce the weight coefficient ($\alpha < 1$); the choice of its value, however, reduces the convergence speed of the iterative process, often very a low factor, ensuring the convergence of computing after a very high number of iterations. To establish an optimum weight coefficient

value and ensure convergence of the iterative process within a minimum number of iterations, a more serious analysis of its dependence on the thermal properties of blocks 1 and 2 is required. By finely analyzing the iterative process between the two blocks, whose lateral dimensions are identical (to be able to apply the same transformation), we can show that transformed $\Phi_{E1,k}$ entering the block 1 during iteration number k is

$$\Phi_{E1,k}\alpha\left(\frac{1}{A2_{22}}\Phi_{E2}-\frac{A2_{21}}{A2_{22}A1_{22}}\Theta_{S1}\right)\left(1+q+q^2+...+q^k\right), q=\left[1-\alpha\left(1+\frac{A2_{21}A1_{12}}{A2_{22}A1_{22}}\right)\right]$$

where $A1_{ij}$ and $A2_{ij}$ designate chain matrix coefficients of blocks 1 and 2 respectively.

This expression shows that $\Phi_{E1,k}$ is the sum of the terms of a geometric progression, with reason q, which actually depends on the weight coefficient chosen and on the thermal properties of blocks 1 and 2, via the chain matrix coefficients on these blocks. The calculation process will converge if the module of q remains below 1, which leads to the inequality:

$$\alpha<\frac{2}{1+\frac{A2_{21}A1_{12}}{A2_{22}A1_{21}}}$$

The coefficients $A1_{ij}$ and $A2_{ij}$ of chain matrices depend on the spatial pulsation m. It is necessary to ensure that inequality is respected in the worst case i.e. for the maximum value of the spatial pulsation m (hence the biggest wave numbers corresponding to the transformation are made on the distributions of temperature and flow within these two blocks). In cases where the lateral dimensions of blocks are different, we can make a similar mathematical analysis, but the practical operation of the results of this analysis is too difficult to implement. It is better to choose a weight coefficient according to criterion α simply ensuring that in the upper block (2) the maximum spatial pulsation remains less or equal to the maximum value defined for the lower block (1).

The extension of the calculation procedure does not become a problem if you divide the complete structure of the model into sub-assemblies under the same level of interconnection. In referring to the case of the structure outlined in Figure 8.15b and going back from the base to the chips, we can successively define the following subassemblies:

– level 1: there is 1 subset formed by the base “E”, which supports both insulating substrates, “SI” right and left;

– level 2: there are 2 subassemblies formed by the insulating substrate "SI" right and left that support heat dispatchers "RC" right and left, respectively;

– level 3: there are also two subassemblies formed by heat dispatchers "RC" right and left that support chips $IGBT_1$, $IGBT_2$, D_1 and D_2 and there are chips $IGBT_3$, $IGBT_4$, D_3 and D_4.

Such a decomposition may be made on any structure and each defined subset may be individually treated with the algorithm of the Figure 8.18. An identical algorithm can be implemented to find the flow into the base that supports all other blocks. We simply note that when a subset is characterized by a weight factor α less than 1, the convergence of calculation can be assured if we proceed for this subset with local iterations preserving the stability of the local calculation.

8.5.1.6. *Computer implementation and a calculation example*

In order to apply the calculation principles developed in the preceding sections, a computer program called LAASTHERM was developed. In its current version, this program can treat structures with a maximum of 100 blocks spread over 10 levels of interconnection. A set of 300 layers can be freely distributed among the 100 blocks and the power dissipation on each block can be accurately described through a set of 1,000 rectangular shape basic sources that can be arranged on the upper surface of this block. The LAASTHERM software also makes a pre-analysis of thermal properties for each of the blocks which have been defined and determines:

– for each block, the minimum spatial resolution required;

– for each level of interconnection, the weight coefficient α, which will be chosen for the stability of local iterative calculation.

Figure 8.19 gives a calculation example of the temperature and flow distributions, made by LAASTHERM for the structure described in Figure 8.15a (geometric structure and thermal data) and for the following distribution of power dissipation:

– $IGBT_1$, 140 W; D_1, 70 W; $IGBT_2$, 120 W; D_2, 60 W;

– $IGBT_3$, 100 W; D_3, 75 W; $IGBT_4$, 130 W; D_4, 80 W.

Figure 8.19a gives the general map of surface warm-up; such as an infrared camera would reveal in a view from above, whose case had been opened. Figures 8.19b and 8.19c show the heat flow distribution maps, leaving the dispatcher heat

"RC" and the insulating substrate "SI" of the right side of the module. Figure 8.19d shows the distribution of heat flux that leaves the underside of the base. The spatial resolution is 16 by 16 points for all blocks, except Block "RC" for which it is 16 by 32 points and the base "E" for which it is 32 by 32 points. The calculation time required to obtain all these results is less than a minute on a workstation.

8.5.2. *The numerical models*

In this section, we will outline the two digital simulation softwares that we used. Other softwares are marketed, especially Ancys that many designers recommend.

8.5.2.1. *Flux 3D*

8.5.2.1.1. Description

The Flux 3D software developed at Electrical Engineering Laboratory in Grenoble [SAB 86] allows us, through the module Fluxtherm, to solve the equation of heat in a system, in permanent system. The user must define the geometry of the problem, creating points and lines, surfaces and volumes. He must assign physical properties to these areas and volumes (for example, in our case, the thermal conductivity of silicon and water). Then comes the important step of meshing: this is a finite element software: each line of the geometry includes points more or less close together according to the desired accuracy of calculation. The software then creates a mesh whose elements are tetrahedrons. The last step is to implement the boundary conditions on the borders of the system. The convection is characterized by the heat exchange conditions along the walls where the convection takes place: the user must provide the value of coefficient h.

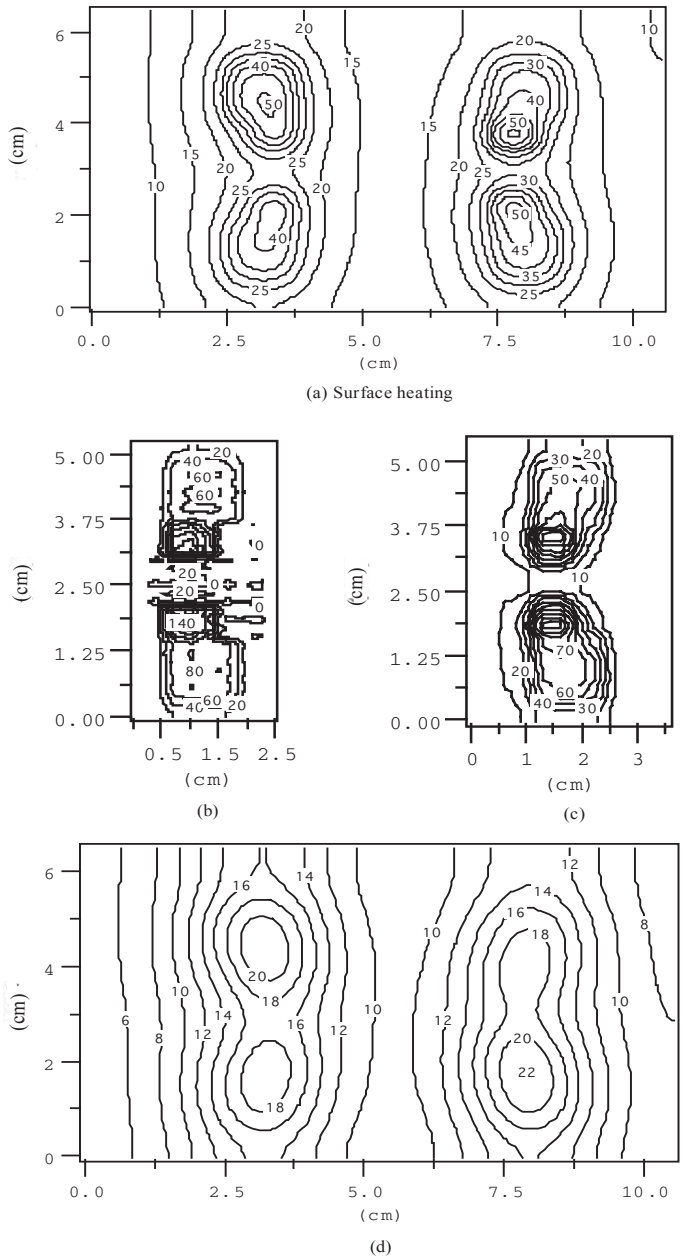


Figure 8.19. *Calculated temperature and flow distributions*

The simulation gives, as the main result, the temperature at any point in the field under study: we deduce the average volume temperature of the junction, which in turn allows us to calculate the square thermal resistance of convection and diffusion:

$$R_{cconv} + R_{cdiff} = \frac{[\frac{1}{V}\iiint_{v} T(x, y, z).dV - T_a]}{\varphi}$$

8.5.2.1.2. Advantages

The Flux 3D software provides two major attributes for modeling thermal electrical devices, namely:

– This software promotes research into electro-thermal coupling (module Flux Chip) [RAE 97]. However, in this study, which deals mainly with design of micro-coolers, we will not take this opportunity and we will instead, consider the power dissipated as a given value.

– Typically, the default of finite element software leads to long computing times when the mesh is dense, as is the case if one wants to have a good consideration of interface phenomena. Indeed, they require the very thin mesh areas, leading to numerous elements and therefore equations to solve. In Flux 3D, the problem is greatly simplified by the potential introduction, of superficial elements with breaks to represent very thin areas (skirmishes, brazing). Their introduction provide precision areas with very different thicknesses.

8.5.2.1.3. Defects

Finite element softwares like Flux 3D essentially present three limitations:

– warm up and moving fluid are not taken into account: the fluid is considered as isothermic. The convection is therefore governed solely by the coefficient h, which is difficult to assess, and needs to be imposed by the user;

– the time of calculation, which nevertheless remains high (about ten minutes to several hours if we simulate the cooler in its entirety);

– the need for a new meshing when changing the geometry of the cooler, makes this method badly-suited to the design.

8.5.2.2. *Flotherm*

8.5.2.2.1. Description

The software was developed by the Flomeric Company to model the thermal and hydraulic aspects encountered in various applications ranging from the air conditioning for a room, to the cooler for power electronics. By solving the Navier Stockes equation, in addition to those of heat, we obtain the temperature at any point in the field, the speed and pressure of the fluid at any point. As with Flux 3D, the average temperature of the heating source is treated as a junction temperature and we get the total square resistance.

8.5.2.2.2. Advantages

The design of the Flotherm software provides, in our case, four advantages over the previous one:

– it allows for consideration of the fluid-wing convection: the h coefficient is not imposed by the user, but determined from the hydraulic and thermal equations;

– it takes into account the fluid mechanics: the problem can be solved in various situations, such as an established or not hydraulic system, a laminar or turbulent system;

– the software has libraries of materials, geometric shapes, and objects (fan, pump, etc.); and finally,

– other conditions such as heat radiation or natural convection can be treated.

8.5.2.2.3. Defects

Flotherm presents the following limitations:

– the parallel piped mesh does not permit the calculation of heat exchange on curved surfaces or ramps. It is therefore not possible, for example, to simulate coolers with trapezoidal or cylindrical channels;

– the software does not take into account the electro-thermal coupling;

– computing time is relatively short for simple applications, however, for the same reasons as those cited for Flux 3D, it remains too long to reach an optimization: the resolution time varies between one minute and ten hours

depending on the complexity of the problem (the calculation convergence difficulties arise mainly from the hydraulics).

8.5.2.3. *Simulation results*

We have now addressed the relevance of the two programs, namely knowledge of the junction temperature of a heating component according geometric and hydraulic parameters and a cooler.

Let us now examine what other results it is possible to obtain. As we said, Flux 3D solves the equation of heat along a wing. It is then possible to trace the isotherms in this wing, as seen in Figure 8.20. Given the different symmetries, and to gain calculation time, we simulate a part consisting of a channel and its two half-fins located on both sides.

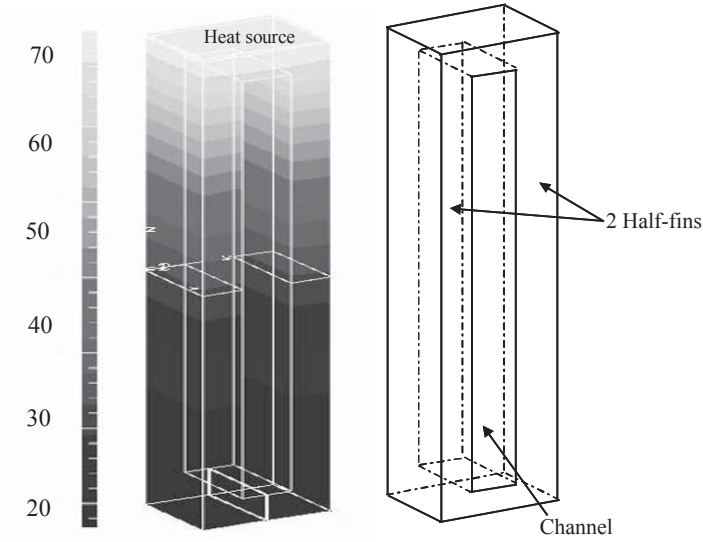


Figure 8.20. *Isotherms in two half-fins, data from Flux 3D: simulation of a channel and its two silicon half-fins*

In this figure, we see that the isotherms are all parallel to each other and perpendicular to the fins axis. The flow of heat is therefore unidirectional expressed by the vertical axis.

The Flotherm software also takes into account the fluid flow within the cooler. By simulating the entire structure, we gain access to the temperature map inside the

cooler (Figure 8.21), to the distribution of load losses (Figures 8.23 and 8.24) and to the velocity vector (Figure 8.22). Through these simulations, we have seen, for example: that the fluid is distributed uniformly in the channels when the holes are centred (which is the case of our coolers), see Figure 8.22 and 8.23; and a movement of fluid when the holes placed on the diagonal, which does not allow as good a distribution (Figure 8.24).

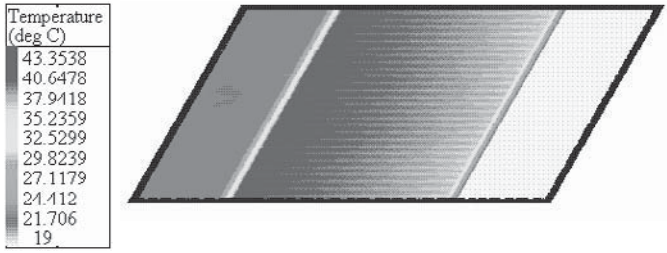


Figure 8.21. *Mapping the temperature of fluid in the cooler*

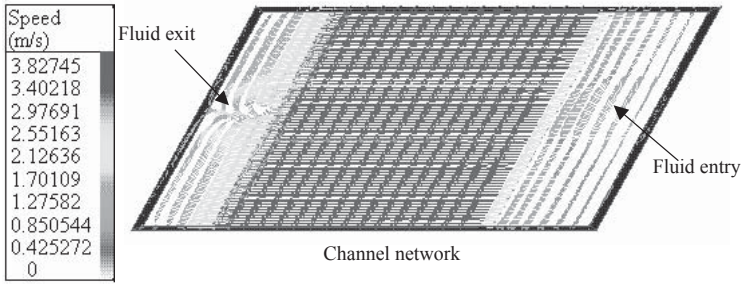


Figure 8.22. *Distribution of fluid velocity in the cooler*

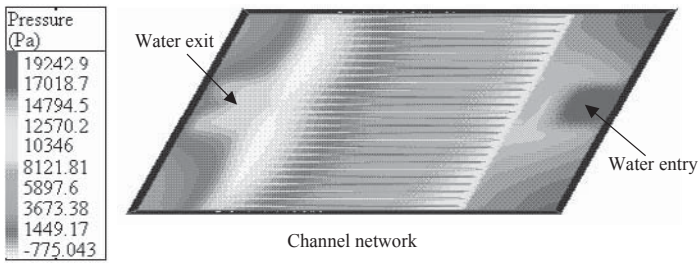


Figure 8.23 *Mapping the fluid pressure in the cooler whose holes are centred in relation to the collectors*

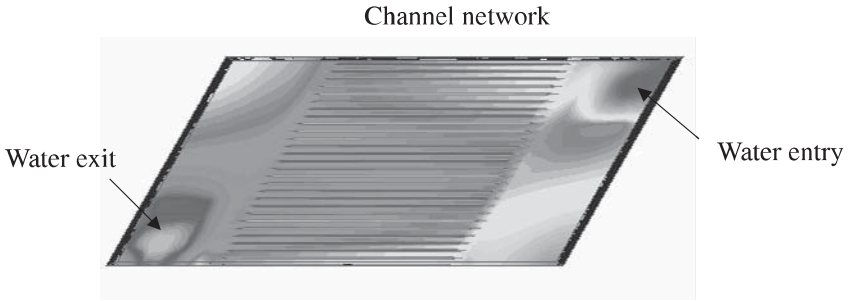


Figure 8.24. *Mapping the fluid pressure in the cooler whose holes are on a diagonal*

8.5.3. *Taking into account electro-thermal coupling*

In the power circuits for electrical energy conversion, power components act as switches with cycles from a state of high impedance (blocked-state), to a state of low-impedance (passing-state). If we analyze the power dissipation of such a component during a cycle of commutation, we can usually see that in the blocked-state the leakage current remains low enough to make the power dissipated by the component negligible. The component only accounts its power dissipation in the passing-state when its losses during commutation switching frequency becomes significant. As the electrical component characteristics, depend on temperature and as its commutation times are also influenced by temperature, there is interaction between the power dissipated in the component and its warm-up: this fact is called electro-thermal coupling. Figure 8.25 illustrates the concept of electrothermal coupling with a simplified functional diagram [BEL 97, HEF 93].

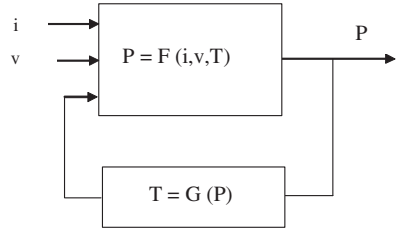


Figure 8.25. *Functional diagram representative of electro-thermal coupling*

Despite the apparent simplicity of the functional diagram in Figure 8.25, solving an electro-thermal coupling problem is not trivial. Indeed we must have software to

calculate the temperature (and/or its distribution) in electrically active areas of the component. We should also put into equations the power dissipation in active areas taking into account the fact that their temperature varies.

8.5.3.1. *Various possible approaches*

Given the level of sophistication expected in the modeling of the electro-thermal coupling, two types of approaches are possible.

8.5.3.1.1. Without taking into account the distributed power dissipation

This procedure is often used when we simulate the operation of a complex circuit with a circuit simulator or a behavioral simulator. In this case, we assume that the active area of the component is characterized by a single temperature. The thermal equations are introduced to assess the temperature of each active area and the electrical equations used to calculate the voltage and current through the active areas are dependent on temperature. This type of procedure is simple to use but it does not provide information on the intrinsic behavior of the component because it completely ignores the distributed nature of current lines in the active area of the component.

8.5.3.1.2. With consideration of distributed power dissipation

This procedure is more accurate because it takes into account that the current density is not uniform in the active area of a power component subject to heating. A distributed thermal simulation must be coupled with a procedure for calculating local power dissipation, taking into account distributions of voltage, current, and temperature in the active areas. Although the waveforms of voltage and current in the component are generally complex in converters, it is practically impossible to use a circuit simulator to calculate the local quantities i(t) and v(t) in the active areas. In order to achieve such a goal, the nature of the distributed component should considered; this requires the description of each elementary part of this component, by a complete electrical model. Given the practical difficulties that we encounter when we digitally simulate the operation of a circuit, with multiple components, whose electric models are usually non-linear; it is difficult to envisage this solution. Now, analytical simplified procedures may be developed for calculating the distribution of power dissipation based on reasonable assumptions. This procedure makes it possible to discover in greater detail, the electro-thermal behavior of a large component or group of components.

The electro-thermal modeling made in the context of section 8.5.3.1.1 is relatively common and one can find many examples in the literature. Electro-thermal modeling according the context of section 8.5.3.1.1 is rarer, however, and the following development will focus exclusively on this technique. With this

technique it is possible to determine whether the electro-thermal behavior of a large component, or of a power module is stable, and, if it would prove unstable, also whether there is an electro-thermal instability, locally or globally.

8.5.3.2. *Determining the power equation*

To simplify and maintain the brevity of the statement, it is limited to a static evaluation of the effect of electric and thermal coupling on large components or components mounted in parallel to achieve power modules. We assume further that the power dissipation in components is mainly due to losses resulting, during the passing-state, of a global current in components imposed by the external circuit.

For almost all the components used in the converters circuits, the calculation of power dissipation in the passing-state can be done without too much error by the approximation of a dropout linear voltage according to the passing current. If this component is isothermal, its direct voltage drop V_{on} can be written:

$$\begin{cases} V_{on} = V_S + R_{on} I_{on} \quad \forall \quad I_{on} \geq 0 \\ I_{on} = 0 \quad \forall \quad V_{on} \leq V_S \end{cases}$$

where I_{on} means the passing current imposed by the external circuit, V_S is a threshold voltage and R_{on} is a series resistance. These last two terms depend on the operating temperature of the component. The second condition is applied to prohibit any possibility of reversing the current I_{on} when the voltage V_{on} becomes less than the value of the V_S threshold voltage.

In practice, the expression above, describing a component approaching a direct voltage drop is all the more valuable when the component is subject to a passing current of strong intensity. The resistance R_{on} of controllable components (MOS and IGBT transistors) can be determined by the value of the voltage command applied to the command electrode of the component (e.g. grid-source voltage for a VDMOS transistor).

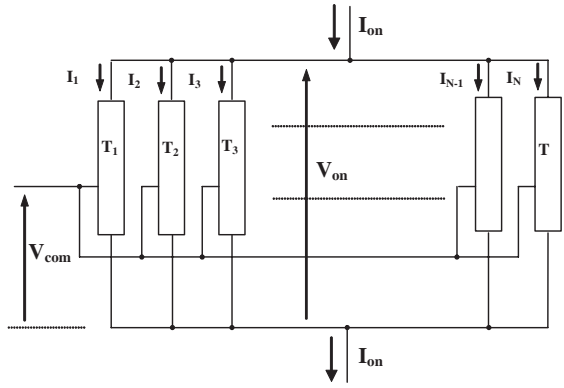


Figure 8.26. *Schematic spread of the active zone of a non-isotherm component*

When the component is no longer an isotherm, we should represent its active area as shown in Figure 8.26. The active zone should be treated as a parallel assembly of basic components, operating so that the direct voltage drop, V_{on}, is common, and sharing common current I_{on}, depending on the local temperature. Assuming that the common current I_{on} is imposed by the external circuit and that the distribution of temperatures in the active area is known, we can calculate the current I_i and common voltage drop V_{on} in solving the system of equations:

$$\begin{cases} I_i = \dfrac{S_i}{S} \dfrac{V_{on} - V_S(T_i)}{R_{on}(T_i)} & \forall\, 1 \le i \le N \\ \displaystyle\sum_{i=1}^{N} I_i = I_{on} \end{cases}$$

where S refers to the total surface of the active area and S_i to the surface of element i at temperature T_i of the active area [VAL 97]. This system of equations implicitly assumes that each element of the active area is still characterized by the law $V_{on}(I_{on}, T)$, which was defined for isotherm components.

To better meet the physical reality, we must prevent the emergence of negative currents I_i, when solving the system of equations. Under these conditions, numerical resolution can no longer be calculated analytically, but should be done only by looking for iterative values of V_{on}, which can verify that the sum of all currents I_i is equal to the current I_{on} imposed on the component by the outside circuit. When

appropriate allocation of the current I_i is obtained, we can simply calculate the distribution of dissipated power in the active area with the relationship:

$$P_i = \left[V_S(T_i) + \frac{S}{S_i} R_{on}(T_i) \right] \cdot I_i$$

Knowledge of the distribution of power can then revive the calculation of temperature distributions, and complete electro-thermal calculation can be achieved by implementing a numerical algorithm whose simplified process is given in Figure 8.27.

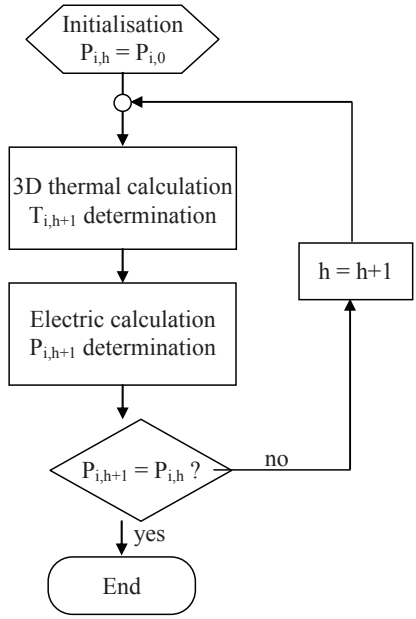


Figure 8.27. *Simplified electro-thermal calculation process*

8.5.3.3. *Examples of electro-thermal simulation*

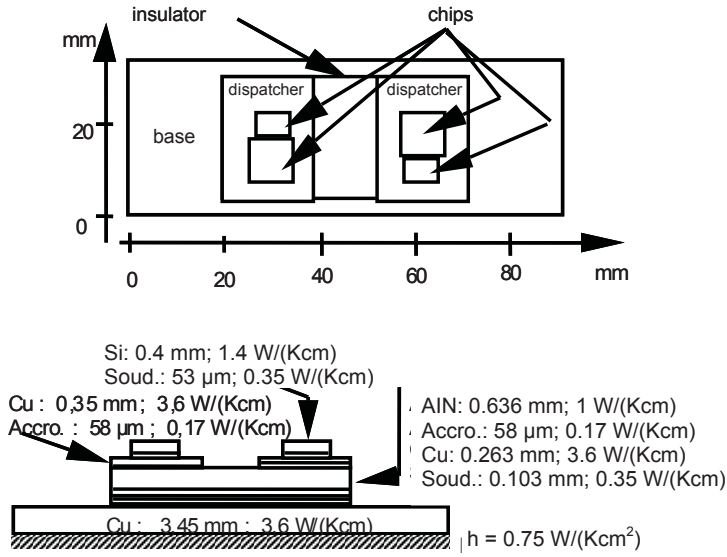
8.5.3.3.1. IGBT module

Figures 8.28a to 8.28c give examples of a simplified electro-thermal calculation conducted on a chip module IGBT MG75J2YS40, whose data on the geometric layout and thermal structure are recalled in Figure 8.28a. For purposes of electro-thermal calculation, the active area of an IGBT has been divided into 64 by 64

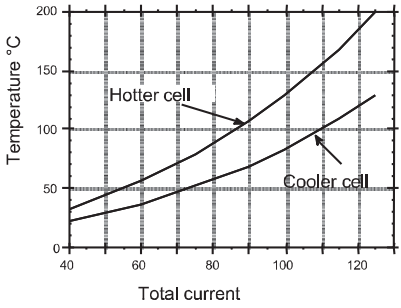
thermal cells. The direct voltage drop during the passing-state of the IGBT can be calculated from the threshold voltage, V_S, of the on-state resistance, r, whose values in relation to the temperature are:

$$V_S(T) = 1.7213 - 1.644\ 10^{-3}\ T - 1.229\ 10^{-5}\ T^2$$

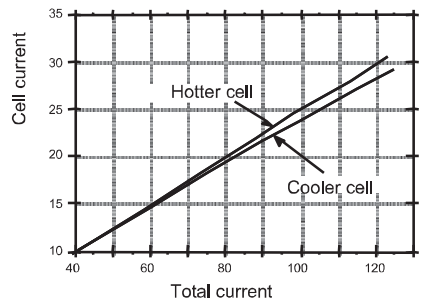
$$r(T) = 1.198\ 10^{-2} + 8.74\ 10^{-5}\ T$$



(a) Geometric behavior and thermal structure



(b) Temperatures calculated on the chip



(c) Current calculated in the cells

Figure 8.28. *Example of an electro-thermal simulation module IGBT MG75J2YS40*

Figure 8.28b shows the calculated evolution of the highest and lowest temperatures of the active area, depending on the external current imposed on the chip, while Figure 8.28c gives an indication of the distribution of this current in the different thermal cells which have been defined. It should be noted that in this case the local electro-thermal behavior of IGBT is stable, which makes in practice a very low dispersion between the minimum local current established in the hottest cells and the maximum local current established in the coldest cells.

8.5.3.3.2. MOS transistor module

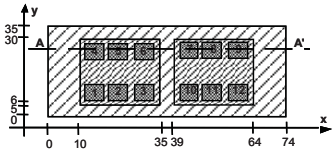
The following example focuses on the electro-thermal study of a hybrid module including MOS transistor reference MTM 8N60 mechanically mounted as shown in Figure 8.29a and assembled as a bypass, six by six, for the electrical operation. Figure 8.29b recalls data on the thermal structure of the module, and the direct voltage drop during the passing-state for a thermal cell of index, i, and temperature, T_i, of a MOS transistor is calculated from its resistance, r_{oni}, during the passing-state. This is given by the relation:

$$r_{oni}(T_i) = 0.432\ N\ (1 + 2.864\ 10^{-3}\ T_i + 1.371\ 10^{-5}\ T_i^2)$$

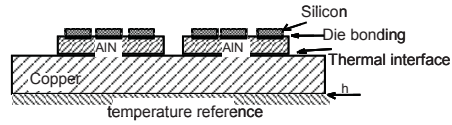
It is assumed for this study that only chips 1 to 6 are active and share a common current imposed by the external circuit.

Figure 8.29c shows the calculated evolution and the maximum temperature reached by chips no. 1 and 2 according to the total current imposed by the external circuit. Note first the good homogeneity of maximum temperatures which are very similar when the external current increases, thereby demonstrating that the power dissipated by each of MOS transistors remains well balanced and that the electro-thermal local stability of the MOS transistors module is very good.

Figure 8.29d shows a comparison of the maximum temperature evolution that can be achieved depending on the current; considering on the one hand a R_{on} independent of temperature, and on the other hand the full effects of the electrical and thermal interaction. We can see that taking into account the full electro-thermal interaction leads to a significantly lower current value at the limit of overall thermal stability. The latter is crossed when the power dissipation is no longer compatible with the power, which can be evacuated by the cooling device.



a) geometrical layout of the different blocks (all sizes expressed in mm)



Copper width = 2.5 mm ; k = 3.6W/(cm.K); D = 1.03 cm2/s

AlN width = 0.7 mm ; k = 1.1W/(cm.K); D = 0.48 cm2/s

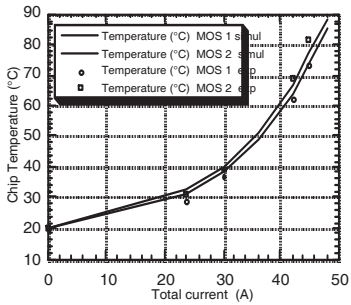
Die bonding = 0.08 mm ; k = 0.35W/(cm.K); D = 0.27 cm2/s

Silicon width = 0.3 mm ; k = 1.6W/(cm.K); D = 0.93 cm2/s

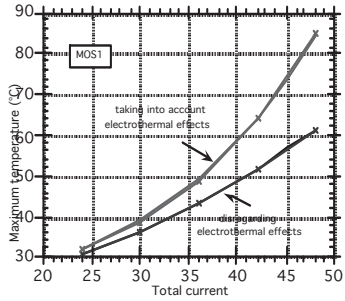
Convective exchange coefficient h = 0.5 W/(cm2.K)

Thermal interface: Rth = 0.06 cm2.K/W

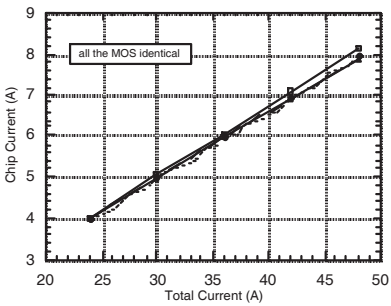
b) thermal structure along the line AA'



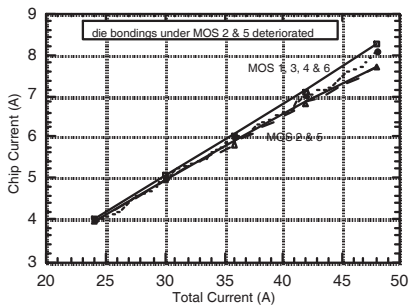
(*c) Evaluation of temperatures*



(d) Comparison of heat-up calculated with or without electro-thermal coupling



(e) Sharing of currents between the chips



(f) Influence of an imbalance between thermal resistances

Figure 8.29. *Example of electro-thermal simulation of a MOS transistor module*

Figure 8.29e shows the evolution of currents conducted by the various chips according to the total current imposed on the module. It should be noted that these currents are very similar for different chips, even when approaching the thermal limit imposed by the stability of cooling. By way of comparison, Figure 8.29f shows the impact of a degraded thermal contact under chips 2 and 5: it is assumed that the thermal resistance of the weld of chips 2 and 5 is increased by a ratio of one to three compared to welds of other chips. While this situation leads to a significant overheating of chips 2 and 5, the current conducted by these chips only decreases slightly. We can therefore say that in practice, if we observe, in a MOS transistor module whose chips are mounted in parallel, strong maximum inequalities of temperatures between chips, this disparity in temperatures is caused by the imperfections in the thermal environment near chips.

8.6. Experimental validation and results

In this section, we will present the experimental results obtained from two test benches. The first operates a direct measurement of temperature and the second an indirect method. Both methods are commonly used.

8.6.1. *Infrared thermography*

8.6.1.1. *Overview*

General principles of radiation physics teach us that, the surface of a body brought to an absolute temperature, T, radiates a power density p (expressed in $W \cdot m^{-2}$) into the surrounding space proportional to the fourth power of its temperature (Stefan-Boltzmann law). The radiated wavelengths and their relative intensity depend on the temperature provided by Planck's law. Conversely, we can use the radiated power, detected in an appropriate wavelength range to determine, under certain specified conditions, the temperature of the body under observation: this is the principle of infrared thermography which operates with electromagnetic radiation commonly in the wavelength range of 2 to 10 μm. There is no attempt here to rebrief on theoretical infrared thermography, which may be found in the above cited works, we simply to show how it is possible to operate in practice to measure the temperature of the active parts of hybrid integrated circuits when they are operating. Currently, infrared thermography is practiced with an infrared camera connected to an electronic monitor, whose role is to interpret the radiometric image directly in the form of a map of temperature, provided that the local emissivity of the surface on which the radiation is studied is known.

8.6.1.2. *Precautions*

It should be noted first that measuring the operating temperature of a component by infrared thermography requires direct observation of its surface and therefore requires the investigator to work on components whose environment has been altered to make this observation possible. In particular, the junction temperature of an encapsulated component cannot be accessed by thermography. At least the case must be opened and all the protective layers removed to give direct access to the optical surface to be observed.

Then take into account the fact that the surface to observe has multiple areas of a different nature (the semiconductor oxide or passivant, metal), characterized by very different emissivities that make it difficult to directly interpret the radiometric image under the form of a thermal map. In general, we get good results only if the surface emissivity is homogeneous. For this, the easiest method is to paint the surface with a thin layer (10 to 15 μm) of black paint to ensure a uniform emissivity value close to unity (≥ 0.95) with the wavelength range operated by the IR detector of the camera.

When dealing with the surface in order to standardize its emissivity, we should be vigilant of the paint deposit thickness. Figure 8.30 shows the problem of determining a constant temperature, T, from the temperature, T_M, measured by the infrared camera on the surface of the deposit of paint of thickness e, conductivity, k, and assuming that the heat was evacuated by convection (characterized by the coefficient h) from the surface of the deposit of paint. Under these conditions, we can easily show that the quantities

ΔT_M ($= T_M - T_A$) and ΔT ($= T - T_A$) are linked by the relationship:

$$\Delta T = \left(1 + \frac{he}{k}\right)\Delta T_M$$

This relationship clearly shows that the difference in measured temperature ΔT_M drops representative to the real temperature difference ΔT, as soon as the ratio he/k remains low compared to the unit. We conclude immediately that if the measured temperature must remain representative of the temperature sought, the filing of paint which is generally characterized by a low thermal conductivity (≤ 0.01 $W \cdot K^{-1} \cdot cm^{-1}$) must be much finer if it is to be associated with the large convective exchange ratio observed at the surface.

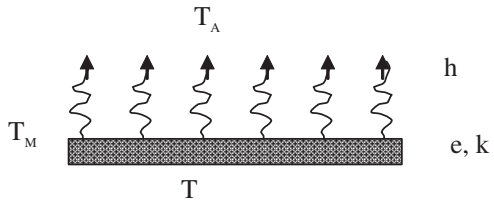


Figure 8.30. *Classic problem of measurement by infrared thermography*

The general purpose infrared cameras are made to provide the radiometric images at a rate of 30 to 100 images per second. In these circumstances, it is as if the thermal scene was observed sampled at a frequency of 30 to 100 Hz. Applying the classic rules (Shannon's theorem) on sampling, we should restrict this technique to observe static or at least slow phenomena, characterized by relatively long time constants (≥ 0.1 s). We may therefore observe the slow transitional heating resulting from the gradual heating of the housing, characterized by constant timespans of several seconds or even minutes. The rapid heating on chips in cases of accidental electrical overload, are often thermal transients characterized by time constants ranging from a few μs to the ms.

8.6.1.3. *Example of thermo-graphic survey*

Figure 8.31 shows a thermography record done on a power IGBT module (MG 200 JYS1 from Toshiba). For the purposes of experimentation, the module was mounted on a water cooler which helps maintain its underside in contact with water at a constant temperature. The upper part of the case has been removed, as well as the freezing filling, contributing to the electrical passivation of the components and their protection against corrosion. The surface of the module was covered with a black paint to make its emissivity uniform. A preliminary calibration was done by heating the module; by circulating a water at regulated temperature to verify that the emissivity of the surface is actually homogenous, and close to 0.9. This actually helps to interpret the radiometric image as a map of temperatures. For this experience, chips 1 (top) and 2 (bottom) are mounted in parallel and share a total current of 90 A under a common voltage drop equal to 2.94 V. The total power dissipated by the module is 265 W and is divided into 140 W for chip 1 and 125 W for chip 2, which explains why chip 1 seemed hotter according to the thermography.

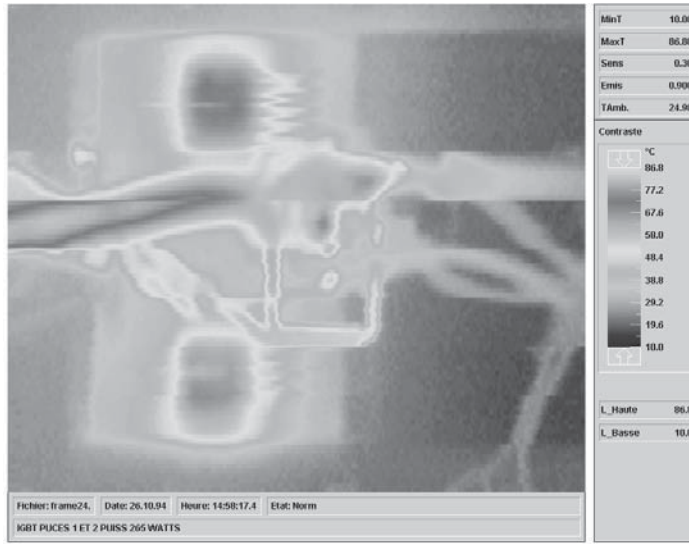


Figure 8.31. *Example of thermography statement for an IGBT power module*

The thermography also shows that the power dissipation is far from negligible in the connection wires that bring the current to the IGBT chips collectors. The distortions of the observed temperature distribution in the active areas of the IGBT chips are due to the local connection wires. A more detailed study and comparison calculated temperature distributions and those measured by infrared thermography determined with certainty that the cooling module is characterized by a convective coefficient exchange whose value is not constant but varies, depending on the position at the base of the module.

8.6.1.4. *Conclusions*

Due to the constraints applied to the sample under test, it is clear that the infrared thermography is not an appropriate technique for junction temperature measurement, for components operating in normal conditions. However, the fact that it is able to provide with good definition (an image is commonly made up of 100 lines with 256 pixels, and is even better for the most recent devices) information on the distribution of the surface temperature of the studied components, this technique can be an excellent tool for validation of thermal modeling results.

8.6.2. *Indirect measurement of temperature from a thermo-sensible parameter*

8.6.2.1. *Description of the measurement bench*

We present in this chapter measurements taken on an IGBT equipped with a cooler made of micro-channels flowed by the circulation of water.

The measurement bench, presented in Figure 8.32 consists of a hydraulic open-loop, a heating source and different systems for measuring temperature.

The hydraulic system itself is composed of a debimeter, a 10 μm filter limiting the risk of channel obstruction and a digital gauge measuring the loss of water pressure between the input and output of the cooler at collector limits, with an uncertainty of 10 mBar.

To characterize a cooler, we should apply a constant power P to its upper side – this is the role of the heating source – and have access to three temperatures: that of water at the input of cooler T_e, that of water at the output T_s and that of the upper surface of the cooler, which we called junction temperature T_j.

From these different measures, we deduct the thermal square resistance by the equation:

$$R_{cmestot} = \frac{T_j - T_e}{\varphi}$$, where φ is the heat flow

The water temperatures at the entrance and exit are measured through thermocouples inserted in the hydraulic pipes, and linked to an acquisition system using the Madena software. The uncertainty on the measures is around ± 0.5°C.

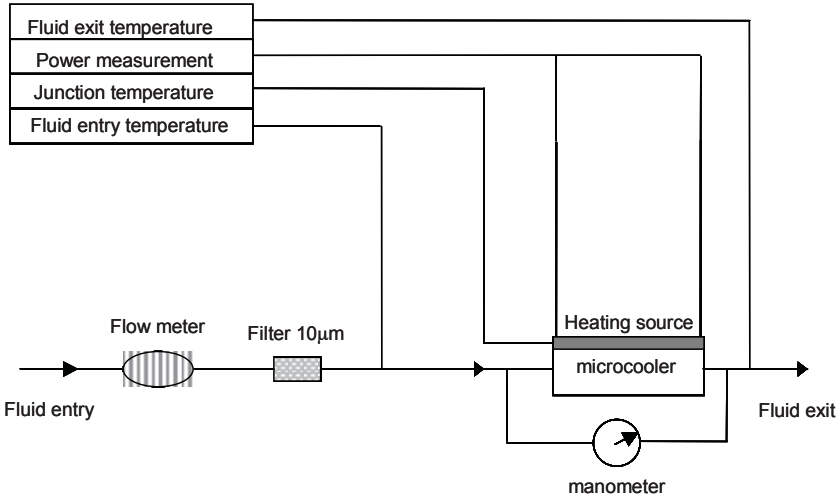


Figure 8.32. *Schematic of the measurement bench*

In the case of copper coolers, an IGBT without case is directly soldered onto the upper side of the cooler, which also plays the role of connector with the drain. The measures of current and voltage give the power value ($P = \varphi \cdot S_P = U \cdot I$). The temperature at the junction of IGBT in this case is equal to the temperature of the upper surface of the cooler, since the thermal resistance of the solder can be considered negligible (less than 1% of the total resistance) [LAF 96]. The measure of this junction temperature is made indirectly by measuring an easily accessible magnitude, called the thermo-sensitive parameter (TSP), whose value varies with temperature following a known law. The TSP usually chosen is the voltage drop when the device is flowed by a low measurement current I_e (10 mA) [GRA 85]. The circuit in Figure 8.33a allows us to make flow a current of the form given in Figure 8.33b. The current I_{ch} issued by the pilot switch, ensures the heating of the IGBT. The time of application must be sufficient to achieve a permanent heat operation (around 100 ms) [MEY 98]. For the measurements, this current is blocked by the pilot switch. The component under test, is then flowed by a calibration current supplied by an auxillary source. V_{sat} is measured on its terminals. The measurement time is about 100 µs.

The law V_{sat} (T_j) is linear and increasing with a slope close to 2 mV/K. This method has mainly been used for copper cooler characterization experiments. Some previous work has shown that this temperature is near the volume average temperature of the chip in steady state operation [FAR 94]. This is the definition that we gave to the junction temperature:

$$T_j = \frac{1}{V_p} \iiint_{v_p} T(x,y,z)\,dV_p$$

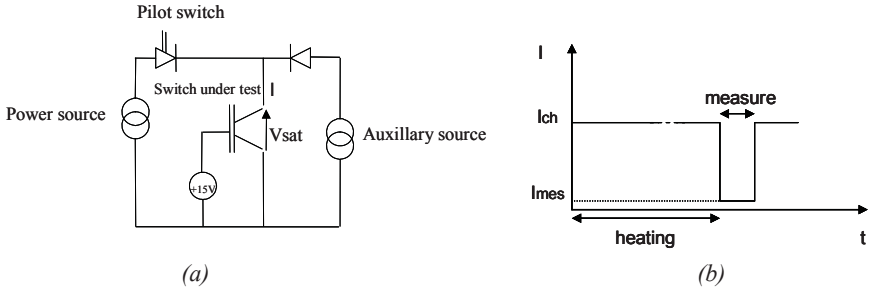


Figure 8.33. *a) Mounting allowing the measurement of the TSP of the test component, b) waveform of the current flowing through the device under test*

8.6.2.2. *Results of measurements*

The following results were obtained on copper coolers prototypes made by Luc Meysenc during his thesis [MEY 98]. Table 8.2 gives their main characteristics.

	channel depth D (µm)	**channel width** lc (µm)	**fin width** e (µm)	**thickness spreader** e_d (µm)	**channel no.** n	**size of red channels** $L_x = L_y$	**section**
Prototype Cu 1	3,040	311	288	1,800	27	1.6x1.6 cm²	rectangle
Prototype Cu 2	730	230	165	1,800	41	1.6x1.6 cm²	rectangle

Table 8.2. *Key geometrical parameters for two copper prototypes made by LEG*

Here, the thermo-sensitive parameter method measurement introduced in the first section was used.

In the best case, it is possible to dissipate, through these copper coolers, a power density of 300 W·cm^{-2} for a junction temperature rise of 60°C. Note that this cooler does not include electrical insulation between the chip and the fluid.

	Q ($l \cdot min^{-1}$)	φ ($W \cdot cm^{-2}$)	R_{cmes} ($K \cdot cm^2 \cdot W^{-1}$)
Proto Cu 1	0.63	156	0.27
	1.33	156	0.24
	1.75	156	0.23
	2	156	0.22
	3.5	156	0.2
Proto Cu 2	0.5	156	0.31
	0.7	156	0.26
	1	156	0.23
	1.3	156	0.22

Table 8.3. *Results of measurements on copper micro-coolers (Q is flow of water)*

8.7. Conclusion

Throughout this chapter, we examined the various aspects involved in cooling power electronic components. We recalled the basic rules for evaluating the losses. We have presented different heat exchanges involved in this type of devices. A substantial portion of the chapter was devoted to thermal modeling of modules on a few examples of software tested during national research operations. It is obvious that this presentation is not exhaustive and that there are other tools that can lead to comparable results.

These modeling approaches, especially those made from analytical equations (which are much faster) are required to design coolers well suited for this type of application.

Finally, we presented some measurement methods and experimental results that validate simulations with acceptable accuracy for this type of problem.

Acknowlegement: the authors thank Professor J.M. Dorkel (LAAS, Toulouse-France) for his great participation to the writing of several paragraphs of this chapter.

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Chapter 9

Towards Integrated Power Electronics

9.1. The integration

9.1.1. *Introduction*

Power electronics is a branch of electronics which uses semiconductor devices for making systems to transform the form, size and/or frequency of waves that carry electrical energy. These operations are carried out with powers far greater than those encountered in linear electronics. For reasons of efficiency, but also because they cannot safely remove a large fraction of the flowing power, these semiconductor devices work between two states, either with a current of the magnitude of the nominal current and a very low voltage at the terminals, or with a voltage close to the nominal voltage but with a current as low as possible. Furthermore, to achieve the necessary conversions, these components must move from one state to another during little dissipative transitions. All these constraints lead to a switching operation in which the role of the semiconductor components can be like that of an operating switch between two states: opened or closed. Thus, the important characteristics of these devices are blocking voltage (a few volts to a few thousand volts), the passing current (a few amps to a few hundred amps), the voltage drop during on-sate operation and switching times which set the losses of conduction and commutation.

Since the first devices, improving performances of power components is achieved in general by:

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– increased voltage and current ratings of devices;
– optimizing performances during the commutation;
– improved security areas;
– greater simplicity of command.

These improvements are the consequences of technological progress in the field of microelectronics, development of new structures and specific studies carried out in the field.

Although the performances to optimize for power components are different from those of integrated circuits, the explosion of microelectronics had a significant impact on the development of power components. In terms of power components, the first trend was mainly an increase in the ratio V.A/mm^2, while for integrated circuits, progress corresponds to an improvement in the ratio of the number of transistors/mm^2. Over the past twenty years, the microelectronics industry has developed significantly with major research effort towards reducing dimensions. Although evolution has taken place in different directions, a transfer of technological progress and means of production was made from the field of integrated circuits to the power components, as shown in Figure 9.1.

In terms of structures, a large number of power components are developed from devices used for the first time in the field of signal processing. 15 years elapsed between the first introduction by the FAIRCHILD Company in 1954 of a bipolar transistor with silicon planar technology and the arrival of the first transistor adapted for use in power. The penetration of MOS transistors in the field of power took place within the same time span as the development of the first VMOS power transistor in 1976. The first realization of a silicon-based MOS transistor was conducted in 1960. This time span saw the adaptation of electrical devices for the application of power requirements. This introduction of MOS technology in the field of power devices is the decisive step that marked a break in the evolution of power components in terms of both performances and structures. The reduction in size of VDMOS structures for low and medium voltage led to a significant reduction of resistance during the on - state operation. For the first time, reducing the size of a power component led to an improvement in its performances, thereby joining the mode of development of integrated circuits. This reduction in size has been made possible by improved manufacturing technology processes from microelectronics, such as double diffusion based on the creation of polycrystalline silicon grids. These devices have benefited from research progress in the field of microelectronics, and sometimes production lines used for older generations of integrated circuits. These works on MOS power components then allowed the rapid development of IGBT, which now constitutes the major axis of power components, and the study of new grid MOS devices such as

MCT, BRT, EST, etc. This has naturally led to the development of power integrated circuits.

These integrated power circuits are an extension of the integration of logic circuits by adding an element of power to signal processing circuits. As in any development in power semiconductor devices, the first achievements were applications with low voltage and low current.

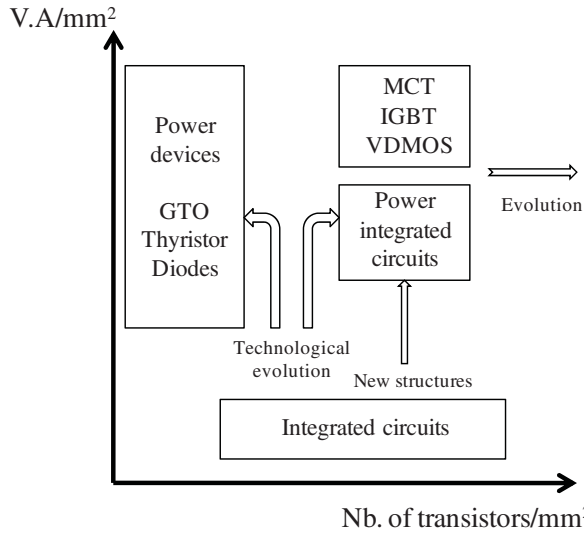


Figure 9.1. *Impact of technological advances in microelectronics on power components*

Currently, only a portion of applications in the domain of very low power (automotive electronics) use integrated power circuits. However, the majority of applications on the power grid can also enjoy the benefits of integration. We will present as a first step the main methods of monolithic integration, and we will then outline the best suited strategies for integration of new functions for the power electronics of the future.

9.1.2. *The different types of monolithic integration*

The strategy for integrating power functions can be handled in two ways: either by promoting the functionality compared to power elements, by promoting the optimization of the power part [CHA 95a, SAN 99a]. The "Smart Power" and HVIC (high voltage integrated circuit) devices are more relevant to the first approach and

are made from technologies of integrated circuits (CMOS or BiCMOS). The devices based on the functional integration of the second approach are based on power component technologies.

9.1.2.1. *Power integrated circuits*

Technological advances in the field of microelectronics have made it possible to integrate into a single chip, power components and logic and analog circuits to serve as command, diagnosis and protection. Thus, the first power integrated circuits for low voltage applications emerged in 1985, fifteen years after the initial integration of signal components.

These power integrated circuits were developed under two names, "Smart Power" circuits and HVIC circuits [RUM 85]. The difference between the two families is essentially linked to the power element and to the ranges of current and voltage addressed:

– for "Smart Power", the power component alone is generally vertical (VDMOS);

– for HVIC, power components are lateral and very often of MOS type (LDMOS).

HVIC are multi-output circuits able to support up to a few hundred volts but presenting very low current densities inherent to the lateral components used. In contrast, "Smart Power" components, more efficient in terms of current densities, and may pass currents of several amps.

The study of insulation techniques between the low voltage area and the power elements was one of the most important challenges of this family of components (Figure 9.2). The self-insulation, the junction insulation and the dielectric insulation are the main solutions used today. However, the dielectric insulation is still costly and, despite its effectiveness, it is still reserved for applications requiring a very strong insulation.

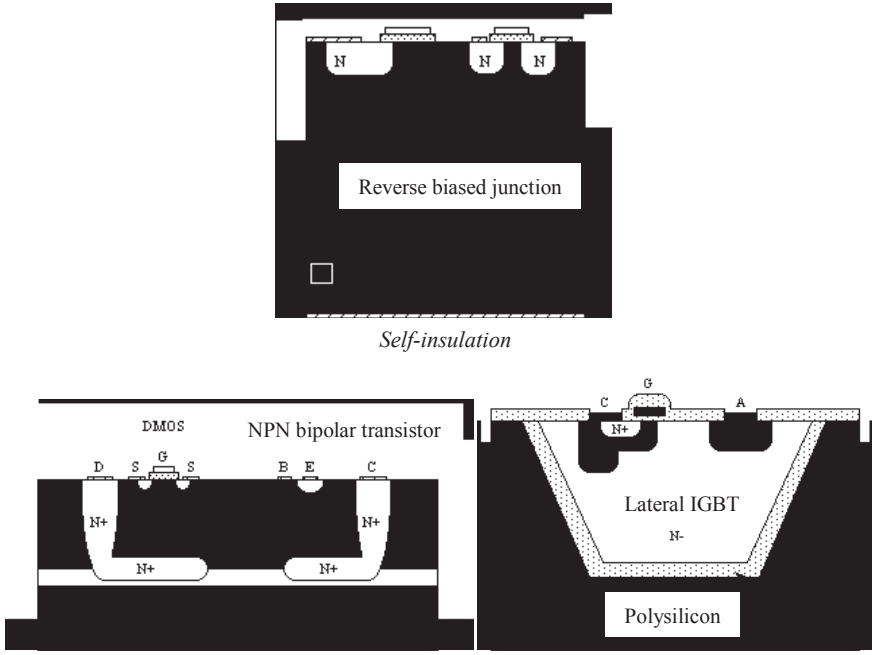


Figure 9.2. *Insulation techniques for vertical and lateral power components*

The first generations of power integrated devices *Smart Power* were carried out with a technology which does not allow very large densities of integration (Figure 9.3). The new generations of "Smart Power" components, Smartmos 5 (Motorola), BCD5 (ST-Microelectronics), SIPMOS (Siemens) are designed from VLSI technologies which must be able to allow for the design of power components able of support voltages in the order of 100 V, using insulation techniques developed in recent years (by junction insulation, dielectric insulation).

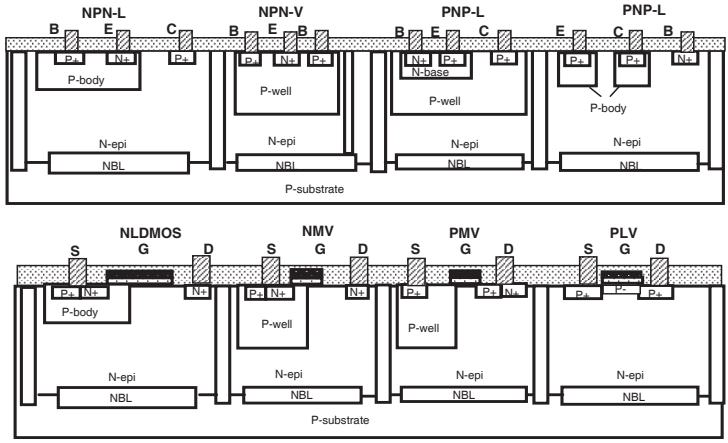


Figure 9.3. *Structures and standard elements on Smart Power Technology*

These technologies make it possible to integrate complex digital circuits (DSP) and micro-controllers. While in the first Smart Power circuits the surface of the power component was often greater than that of the integrated circuit, the trend is reversed in the new power integrated circuits, which are characterized by the integration of new functionalities. This trend is accompanied by a reduction of design rules and advanced technologies. Figure 9.4 shows a block diagram of this type of circuit that can be described as "new Smart Power". It is divided into three parts: the interface circuits, control circuits and signal processing, and the power element. In terms of interface circuits, the trend is to replace the bipolar circuits with BICMOS circuits, for more desirable performances. The signal processing circuit functions correspond to CMOS with low power consumption and high density of integration. The power devices are generally based on DMOS technologies to achieve lateral structures (LDMOS), or vertical structures (VDMOS). In view of increasing functionality, memory can also be integrated. The BCD technologies (Bipolar, CMOS and DMOS) allow considerable flexibility in order to achieve the different types of above mentioned circuits.

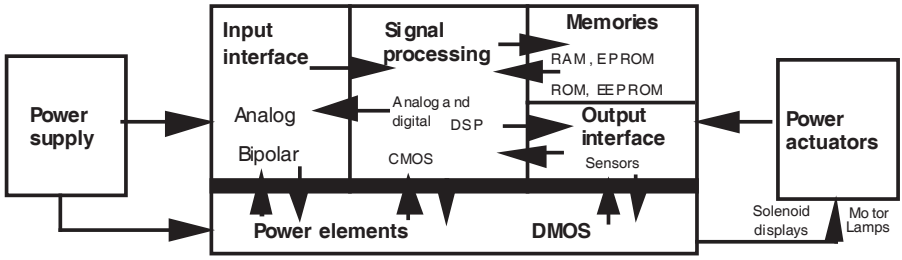


Figure 9.4. *Block diagram of a Smart Power circuit*

The main areas of application of these power integrated circuits are portable equipments telecommunications and automotive electronics. The development of these circuits is mainly supported by automotive applications such as ignition, injection, ABS, lighting, command of small motors (lift windows, air conditioning). The optional level of integration, the range of power and hence the power component are then functions of the proposed application.

The technologies developed for integrated logic and analog circuits with low voltages were utilized a few years after power integrated circuits (Figure 9.5). This different development is linked, on the one hand, to the important work in the field of integrated circuits supported by an important market, and on the other hand by the complexity of integrated circuit manufacture for larger power, where insulation and voltage strength aspects must be accounted for. Today, this gap is reduced to only one generation, while lengths of MOS transistors channels reach 0.6 μm for power integrated circuits, against 0.35 μm or 0.18 μm for VLSI *(very large scale integration)* electronics. This development can allow an estimation of trend for the future of integrated power circuits. This evolution towards an increased degree of integration leads to integrated systems on a single chip in the field of low power.

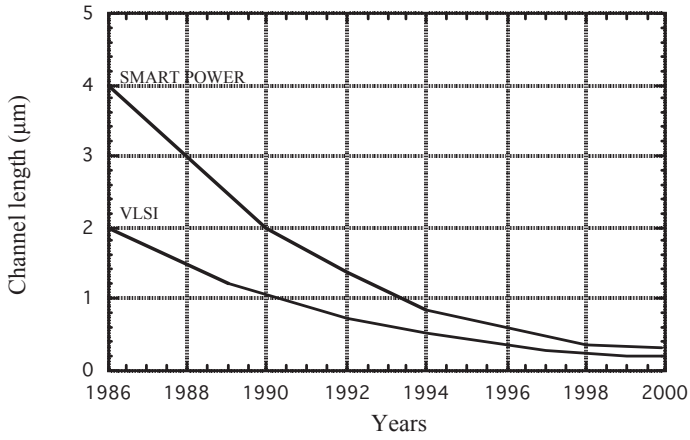


Figure 9.5. *Comparison between the evolutions of "Smart Power" and VLSI technologies*

9.1.2.2. *Functional integration*

The concept of functional integration in power electronics has emerged from the operating principle of the first power devices, such as thyristors and especially triacs [BOU 02, BOU 04, GEN 64a, GEN 64b, PEZ 97a] (see Figure 9.6). In this mode of monolithic integration, the function is made by surface interconnections but also by many electrical interactions between different semi-conductive areas which must be carefully designed and sized.

Without reaching the complexity of functions obtained with "Smart Power" components, devices made by functional integration can obtain specific features for applications of control and protection by combining several basic elements [CHA 95b, SAN 97, SAN 99b, MAR 00]. This mode of integration, based on the vertical power components ability to withstand voltages of several hundred volts, and transit currents of several amps, is better suited to the development of new functions for power applications of medium power connected on electrical energy distribution networks. At the moment, functional integration is evolving both in terms of designing new functions of monolithic power and on developing new technological solutions.

STMicroelectronics, for example, uses this concept of functional integration in the development of new power functions, under the name ASD™ (application specific discrete). The ASD™ is an approach responding quickly to the specifications imposed by a customer [PEZ 95a].

9.1.2.2.1. The AC Switch™ structure

The extension of functional integration enables the development of new command and switch protection functions [PEZ 95b, PEZ 96, PEZ 97b, PEZ 97c], with advantages over discrete components (volume reduction and performances). Figure 9.6 represents an AC Switch™ structure developed by STMicroelectronics in Tours. This structure is well suited for grid applications.

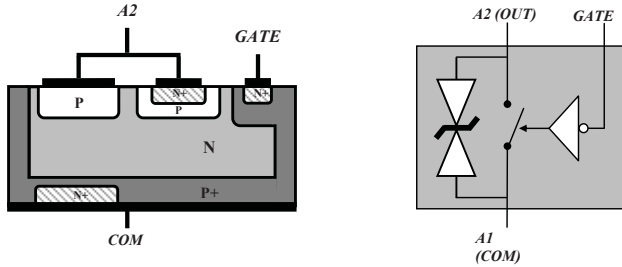


Figure 9.6. *Cross-section view of an ACS structure and electric symbol (patented structure)*

Unlike the triac, two thyristors with anode trigger are managed by a single command. This command, on top of the chip, is referenced in relation to the underside of the chip. This allows a decoupling of the two thyristors (improves *dV/dt* strength) and facilitates the use and mounting of chips onto a single base (such as a radiator).

The technology used is a planar technology with better reliability and lower manufacturing cost. Moreover, the use of suburb P+ areas ensures the robustness of the device in avalanche, and avoids the use of a varistor.

However, the operation under negative command confines the use of the AC Switch to two quadrants (Q2 and Q3 of triac). One of the main strengths of this structure is the design of its trigger which is isolated from the power part by the junction. The reaction of the trigger on the command circuit (called "kick back") becomes low enough to allow the direct command of the trigger by a micro-controller circuit.

9.1.2.2.2. AC Switch™ structures with a predetermined trigger [PEZ 95A] over a half period

The following power structure has a monolithic form in which we find an AC Switch™ with a predetermined trigger, on a half period, which remains automatically conductive on the next period. This device has a sensitive trigger, does

not require a strong boot current, and presents a good immunity against parasitic triggering in terms of dI/dt and dV/dt.

This AC Switch™ consists of a series mounting of two blocks. Each includes a thyristor and an antiparallel diode (Figure 9.7). The first block includes a thyristor with a trigger output. The second block includes a thyristor and a vertical diode in the same substrate. The electrical interaction between these two structures is very strong so that the charges stored during the blocking of the diode are used for triggering the second thyristor (Figure 9.8).

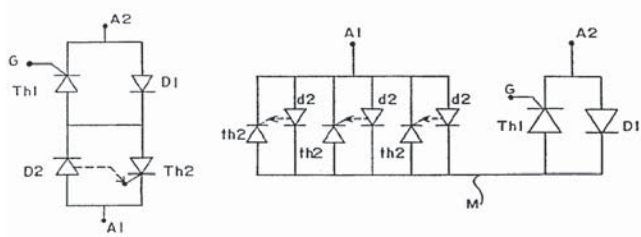


Figure 9.7. *Electric schematic and operating principle*

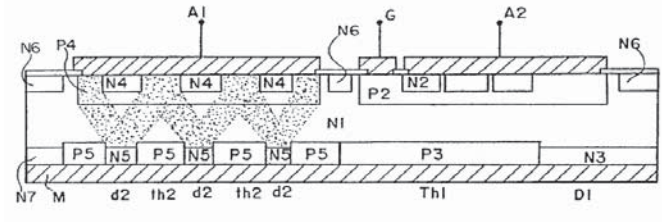


Figure 9.8. *Cross-section view of the AC switch device with a predetermined trigger*

This power device includes a conventional thyristor (*TH1*) with a trigger electrode (*G*), and a diode (*D1*) mounted in antiparallel. This diode *D1* is mounted in series with a second thyristor (*TH2*), which is mounted with a second antiparallel diode *D2*. The structure now has two main electrodes, *A1* and *A2* and a command electrode *G*. Thus, if the electrode *A1* is polarized positively compared to the electrode *A2*, the current passes between *A1* and *A2* through the diode *D2* and thyristor *TH1* after applying an order on the thyristor *TH1*. Then the thyristor *TH2* automatically becomes a conductor during the half period following the conduction phase of the diode *D2*.

The operating principle (see Figure 9.7) and the cross-section view of the structure (see Figure 9.8) highlight the strong electrical interaction between the different structures. This interaction is being used to develop a new feature, which illustrates the potential to create new functions, offered by the mode of functional integration.

9.2. Examples and development of functional integration

Functional integration is not confined to the bipolar structures and multi-layer interactions in silicon. It also applies strongly to other technologies and more particularly to the MOS technology. This gives new lines of components making better use of silicon. The best known state of the art is certainly IGBT. However, many variants have emerged through a process of functional integration. In this part we describe, by example, the functional integration process of a MOS-thyristor function. We then discuss specific functions. The dual thyristor example will be developed to show how, through a process of functional integration, a specific component can be fully established.

9.2.1. *The MOS thyristor structures*

The use of MOS technology for power devices offers a degree of freedom in designing the additional functions of integrated power because they can combine the advantages of both MOS transistors and electrical interactions in the volume. The MOS structures have a high input impedance (considerably simplifying command circuits). However, in standard configurations of vertical MOS structures adapted to power applications, the compromise between on-state resistance and voltage strength limits their use in the range of medium and low powers. To take advantage of this voltage command, research has been undertaken to combine MOS and bipolar structures for “high voltage” applications. The IGBT (insulated gate bipolar transistor) (see Chapter 2), based on this type of association, has undergone an important industrial growth in recent years. The device meets the advantage of a voltage command (via a grid of MOS transistor) and a low on-state resistance linked to the modulation of conductivity inherent to the injection of carriers by the anode structures in the low N- doped region. This approach was then extended to MOS-thyristor associations that are the integration foundation of new power switches.

9.2.1.1. *Ordering the closure of MOS thyristor structures*

In the case of devices such as classical thyristors with a large N-type base, the closure order is carried out through a N-channel MOS transistor that is connected between the cathode and the N base of the PNP structure [BAL 79, JAE 87]. Most of

these devices (known as MOS thyristors or MOS gated thyristors) presented in recent years in the literature are derived from power VDMOS transistors, in which the N^+ drain region is replaced by a P-type region strongly doped to obtain a vertical structure of four thyristor type layers, equipped with an isolated control (Figure 9.9). On this semi-conductive architecture, we can identify a PNP transistor coupled with a NPN transistor, as in a conventional thyristor, and a resistance under short circuit R_{CC} corresponding to the resistance of the P region under the N^+ cathode. In this configuration, the P-type substrate of the MOS transistor is connected to its source region (the thyristor cathode) through this resistance R_{CC} (see Figure 9.9).

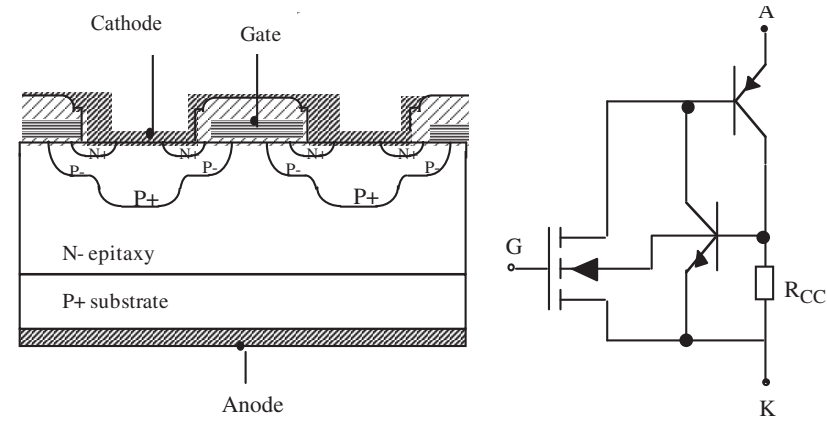


Figure 9.9. *Cross-section view and equivalent circuit of the thyristor MOS*

Most of the components that were developed derive from VDMOS power transistors or IGBT, and are multi-cellular type. But the concept can be applied to single components designed from thyristor structures, in which the trigger region is replaced by a MOS grid [DAR 86, SAN 90].

9.2.1.2. *Orders at the opening of MOS thyristor structures*

Several approaches have been proposed to achieve the opening of a thyristor through a MOS transistor. The latter may be placed:

– in series between the semi-conductive region of the cathode and the cathode contact in order to be able to interrupt the current flow;

– between the N- base region of PNP transistor and the N region of the NPN transistor collector to remove the coupling between the two transistors; or

– in parallel with short circuit resistance between the cathode and the base for value variation, thus changing the level of maintenance current in the thyristor.

9.2.1.2.1. MOS transistor placed in series between the semi-conductive cathode region and cathode contact

In the first option (see Figure 9.10), the EST (emitter switched thyristor) [BAL 90], the cathode region (called cathode floating) of the thyristor structure is linked to an outside contact by a MOS transistor, which plays the role of a short circuit. The passage of current between the anode and the external cathode contact occurs only when the MOS transistor is on; the process of opening happens when we block this transistor.

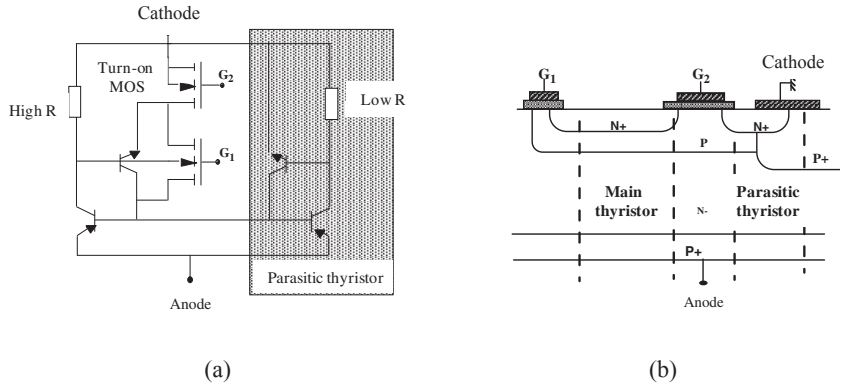


Figure 9.10. *An EST device: a)equivalent electrical schematic; and (b) a cross-section view*

The configuration of this structure places a MOS transistor in series with the thyristor. This contributes to increasing the on-state voltage drop of the device. Indeed, this additional voltage drop becomes a handicap when the current range of the structure is increased. This integration solution leads to the presence of a parasitic vertical thyristor located between the anode and the cathode contact. The device control by the MOS transistor is lost when the thyristor begins to take effect. The closure order is ensured by a MOS transistor placed in an identical pattern to that of the MOS thyristor described in the preceding section.

The solution of setting a MOS in series with a thyristor has also been proposed under the name FIBS (five layers bimos switch) [LIL 92]. This involves a five-layer structure and the integration of several MOS transistors within a single cell (see Figure 9.11). The structure is controlled by 3 integrated MOS transistors, one for the closure and two for the opening. At the opening, the first transistor (MOS A)

connects the cathode of the device to the emitter region of the thyristor. This transistor is therefore placed in series with the thyristor as in the EST structures. To achieve the opening process, we must block the MOS transistor A. From this point on, the device may be likened to a five-layer structure with two junctions to ensure blocking: the main junction (base P base N-) can withstand high voltages, while the other junction made of N- area and P^+ short circuit cannot support them. At this level, the MOS transistor B can eliminate the breakdown problem if it is passing at the time of deadlock. This MOS section also enables the movement of holes from the anode, via the P+ short circuit of cathode.

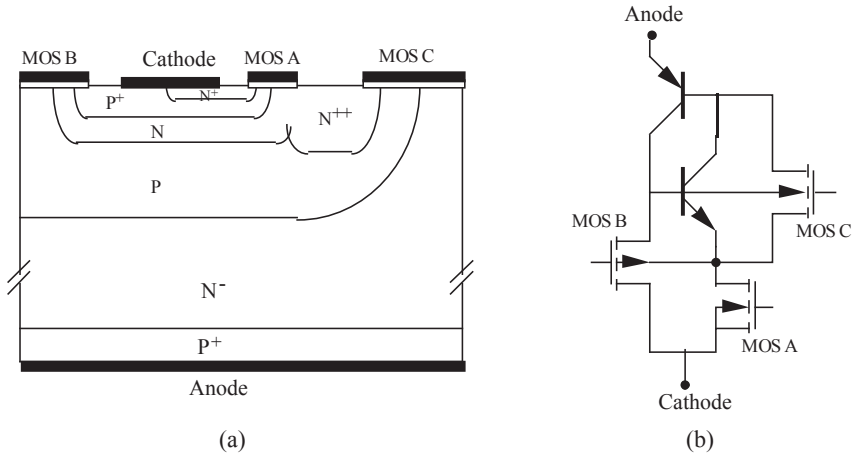


Figure 9.11. *FIBS device: (a) cross-section view; and (b) equivalent electrical schematic*

In another solution called DMT (depletion mode thyristor) [BAL 88], the MOS transistor is placed in series between the base of the PNP transistor and the NPN transistor collector (see Figure 9.12). Applying a negative voltage on the grid induces a depopulated layer in the region A, located under the base of the NPN and between the grids. The distance between these grids is optimized so that this region is entirely depopulated for grid voltages of 10 volts. Once this area is depopulated, the grid polarization produces a potential barrier, i.e. electrons, thus eliminating the coupling between bipolar PNP and NPN sections. The opening process is that of a PNP bipolar transistor with an open base. Thus, for these devices, the evolution of current during this period of openness presents a “tail current”, corresponding to the evacuation by recombination of charges stored in the base.

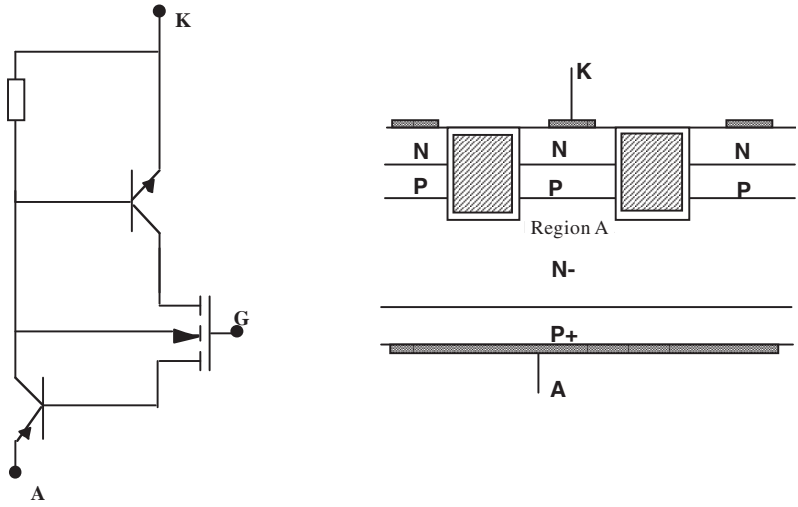


Figure 9.12. *Equivalent electrical schematic and cross-section view of a DMT structure*

9.2.1.2.2. Transistors placed in parallel with short circuit cathode base resistance

Regarding the latter solution, two different approaches using MOS transistors should be distinguished for integration: one is to directly link the two semi-conductive cathode regions and the P base region of the NPN transistor; the other is to connect them via an intermediate semi-conductive region.

Indeed, on the cross-section view of the device shown in Figure 9.13, we note the presence of an additional P^+ region outside of the thyristor section, and linked to the cathode. Applying a negative voltage on the MOS grid induces the formation of a channel on the surface of the N^- region, which connects the P base to the intermediate P^+ region. This helps to reduce the value of the short circuit cathode-base resistance, and will momentarily increase the constant current value of the thyristor section. Opening occurs as soon as this value is higher than its flowed current. This arrangement proposed by BALIGA is known as the BRT (base resistance thyristor) [NAD 91].

It is possible to directly link the P base and the cathode through a MOS transistor acting as an ordered short circuit, thus reducing the value of short circuit resistance between the cathode and base (see Figure 9.14). This decline in resistance increases the value of the constant current, i.e. the nominal current, and allows the device to open for currents less than this maintenance current. This mode of openness is used in devices known as MCT [ART 93, BAU 91, TEM 86].

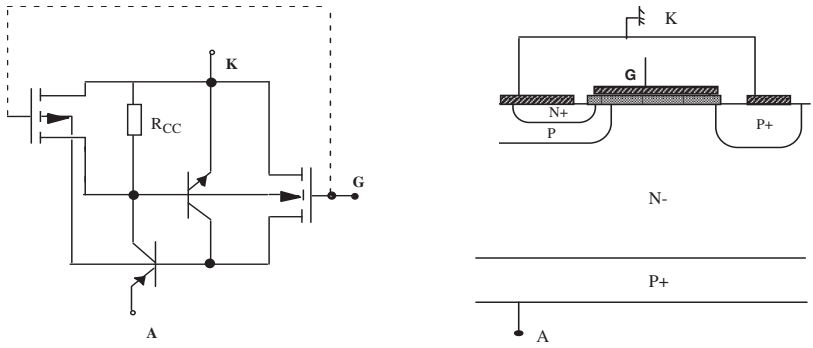


Figure 9.13. *Equivalent electrical schematic and cross-section view of a BRT structure*

The effectiveness of opening these devices is directly linked to the performance of the MOS structures. It is convenient to make small cells in order to get the highest Z/L ratio (width divided by the length of the MOS channel), thus leading to a lowest possible on-state resistance and to an effective emitter-base short circuit. The constraints imposed for these MOS structures, in terms of optimizing the Z/L ratio, are similar to those encountered in the low-voltage VDMOS devices, and as for the latter, the optimization of electrical characteristics are made through deeper integration.

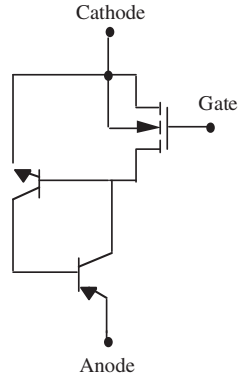


Figure 9.14. *Equivalent circuit of an opening command by emitter-base short circuit*

In the case of the DGMOT structure (dual gate mos thyristor), a lateral MOS structure in a P box allows for short circuiting of the P base with the N^+ emitter (see Figure 9.15). At this level, opening occurs when the maintenance current becomes

greater than the nominal current. Note the adopted technology is similar to that of IGBT because we have a vertical structure with four layers.

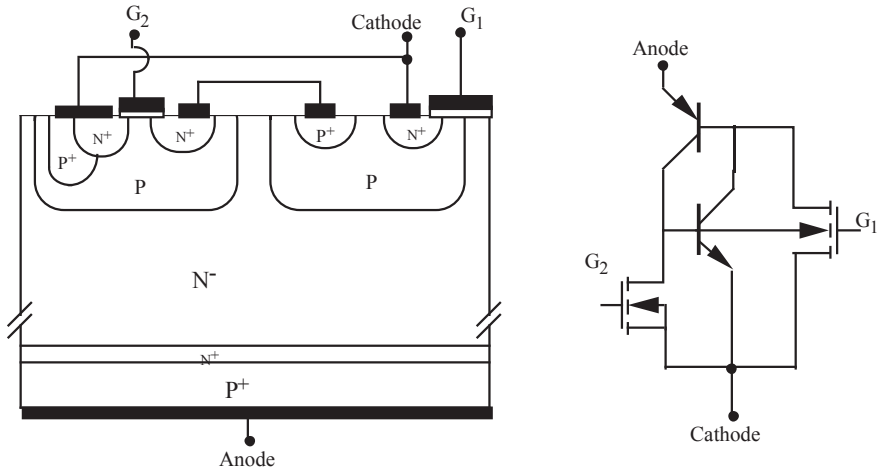


Figure 9.15. *Cross-section view and electrical equivalent diagram of a DGMOT device*

In the case of five layers structures, one should distinguish two types of devices: the NMCT [ART 93] and the PMCT. The principles for closing and opening are the same but the type of MOS transistors used for opening and closing is reversed because the successive layers of the thyristor structure are also reversed. The N or P qualification refers to the type of the thyristors lowest doped base thyristor. In the case of a N base, the integration mode imposes an N-channel MOS transistor for setting conduction and a P-channel for the opening (see Figure 9.16); while in the case of a PMCT with a P base, we have a P-channel MOS for setting conduction and a N-channel for the opening.

As the relationship between the mobility of electrons and holes is clearly favorable to electrons, the PMCT solution displays an improved performance at the opening from that of its counterpart NMCT. However, the real difficulty of manufacturing P-type low-doped substrates in a reproducible way, and the difficulty of growing thicker layers (thicker than 150 μm) by epitaxy, put the PMCT devices out of competition for immediate applications where the voltage required is greater than or equal to 1,200 volts.

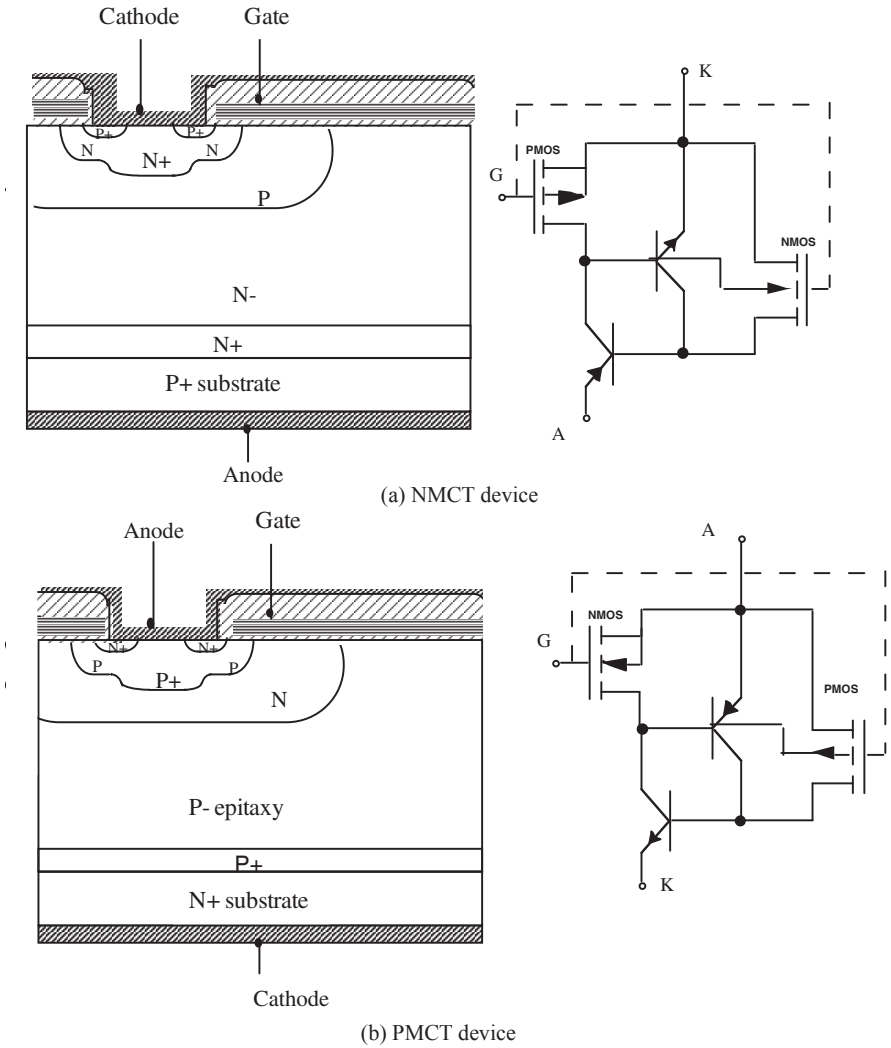


Figure 9.16. *Cross-section view and equivalent circuit of (a) a NMCT structure and (b) a PMCT structure*

9.2.2. *Evolution towards the integration of specific functions*

Currently, the concept of functional integration can be used to obtain, on the one hand, originals ways of switching which are not exploited in the usual components; and on the other hand, ways to perform new functions including in a monolithic

device where the power components are together with protection elements, amplification and validation of the command. This must ultimately lead to improved performances, better adaptation to requirements (manufacturing can be made for a given application), and greater simplicity of design equipment. Firstly we will present the integration strategy adopted for the dual thyristor function; and secondly the integration of a switch-breaker function. These examples will enable us to highlight the generic nature of this mode of integration before outlining the possible developments for the integration of power functions.

9.2.2.1. *The dual thyristor*

The static switches involved in the conversion must possess static characteristics directly related to the reversibility of the energy conversion. It is possible to consider four different types of switches:

– non-reversible (e.g. the bipolar transistor, the diode);

– only reverse voltage (e.g. the thyristor);

– only reverse current (e.g. the dual-thyristor, the MOSFET); and

– reversible voltage and current (e.g. triac).

The dynamic characteristics of components – their way of switching and therefore way of command – must be linked both to the structure of the converter and its strategy of control. These components must either have orders for blocking or triggering, or present spontaneous commutations.

So far, only diodes, transistors, thyristors, and triacs devices have been monolithic. However, it is possible to obtain new integrated switches such as dual thyristors based on the method of functional integration.

The properties of the dual thyristor can be established from those of the thyristor in applying the rules of duality [FOC 78]. Indeed, as the thyristor is blocked during the passage of zero current (or, more accurately, below the keeping current value) the dual thyristor switches on with the passage of the zero voltage (by increasing values). The blocking is obtained by order if the switch is flowed by a positive current, as a thyristor is turned on by the order if a positive voltage is applied on its terminals. All properties of thyristor and dual thyristor are summarized in Figure 9.17 [CHE 88]. If the thyristor function is available as a monolithic device for a long time, dual thyristor function is achieved by combining the basic power components (bipolar transistor, MOST, IGBT, and diode) with a logic command (see Figure 9.18). The integration of these discrete solutions into silicon offers even less benefit as it does not exclude the major handicap of these circuits, namely the need for bulky, costly and potential EMC disturbance vector auxiliary power supplies. In the following sections, we will show that the functional integration

[BRE 98a] is able to achieve global function beyond the constraints described above.

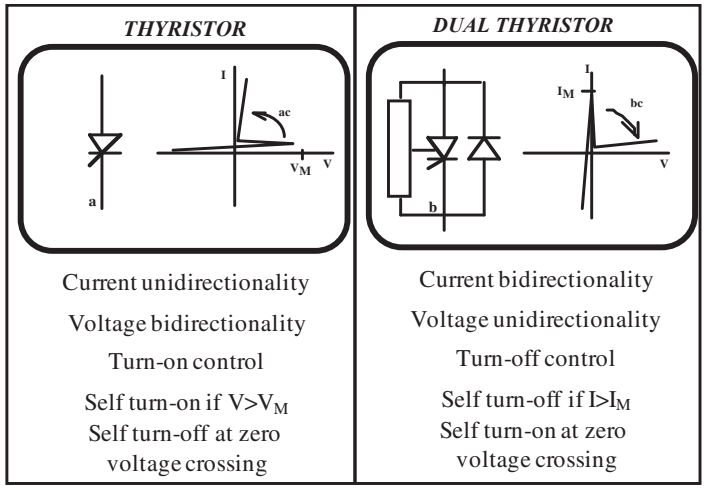


Figure 9.17. *Symbols, characteristics and comparative properties of the thyristor and dual thyristor*

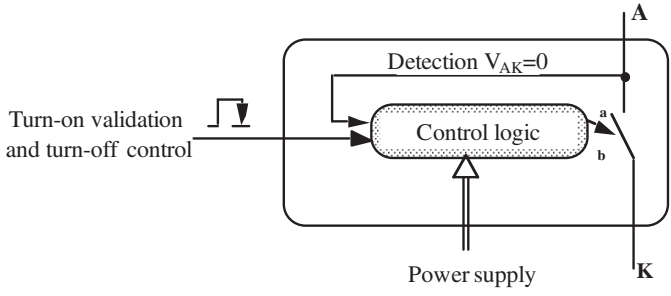


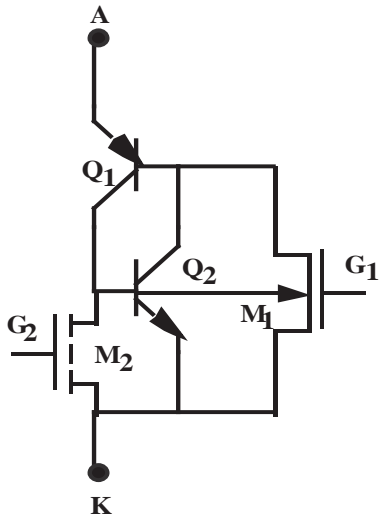
Figure 9.18. *Discrete solution making the dual thyristor function*

The dual thyristor function is a three segment switch, reversible in current. In the family of power semiconductors, the thyristor is the only one to present, under positive bias, a bi-stable blocked-conductive behavior, and to remain started after the abolition of the command order . The basic power device ensuring the "dual thyristor" consists of a thyristor structure. The static characteristic can be obtained by a thyristor structure associated with a diode placed in antiparallel. In terms of

dynamic characteristics, this function must exhibit a spontaneous switch-on at zero voltage and a switch-off ordered by a pulse. Thus, the full functionality can be obtained by completing the thyristor-diode association of two adapted cells for self switch-on and switch-off made with two MOS.

Thus, the heart of the function is constituted by a thyristor with self switch-on and switch-off ability. Figure 9.19 shows the equivalent electrical circuit of the power component for this function and the associated status table. At the closing, the thyristor switches on spontaneously when the anode voltage becomes positive through the current supplied by the MOS transistor with preformed M_1 channel, whose drain current feeds the base of the PNP section and acts as a triggering current for the thyristor. The switch-off is then made by applying a positive voltage to the transistor M_2 grid, to bypass the emitter base junction of the NPN transistor, as is the case in MCT structures. If we analyze the electrical diagram of this function, it is clear that the MOS transistor with preformed channel M_1 must include a N-channel since it is in parallel with the NPN transistor. As M_2 can be either N-channel or P-channel, we can consider two very different structure types for the monolithic integration of the switch function: a four layer structure (where M_2 is a N channel), and a five layer structure (where M_2 is a P channel). As the integration strategy is based on the main component, and as the achievement of auxiliary components must be done by adding a minimum of technological steps, we opted for a four-layer technology type thyristor. In order to make the drain of the opening NMOS, it is necessary to add an additional N^+ box. The main role of this transistor is to short circuit the P base with the N^+ cathode of the thyristor element. For this, a P^+ region is added and linked to the drain. To obtain the NMOS closure, a preformed channel area is added to link the N^- base (drain) to the N^+ cathode (source). The P base serves as a substrate for both MOS transistors. Figure 9.20 shows a schematic cross section of the four layer structure.

This integration is therefore based on the device being able to switch-on and switch-off by itself. The thyristor block can be provided by a pulse command [BRE 96, BRE 98a]. A diode placed in antiparallel ensures the reverse conduction of the device as provided in the dual thyristor. This structure nevertheless has the disadvantage of a boot transistor leakage current prevalent when the device is on hold status. Some developments have been made to reduce these problems, and several references are available on this subject [BRE 97, BRE 98b, BRE 98c, BRE 99, BRE 01, MAR 99, SAN 99c].



V_{G2}	V_{G1}	
0	-1	blocked state
0	0	energizing
1	-1	blocked
1	0	leakage current

Figure 9.19 *Electrical equivalent schematic and functional table of a thyristor able to switch on and off by itself*

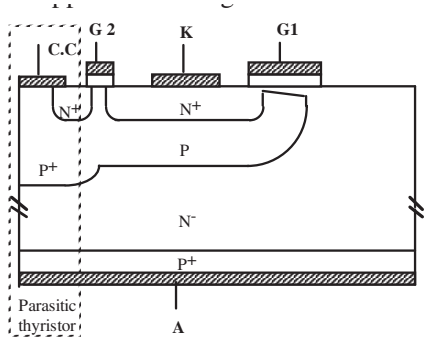
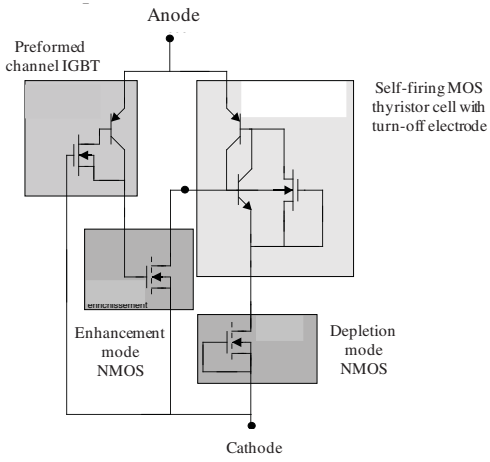


Figure 9.20. *Schematic cross-section view of the four layer structure*

9.2.2.2. *Evolution towards new switch functions*

The functional integration of the design and implementation of monolithic specific functions can also be applied to other types of functions [MAR 00]. One example is the power micro circuit-breaker [SAN 99e] or self switch-on and self switch-off structures [LAU 99]. The development of a bi-stable feature becomes an essential basic sub-assembly for more complex functions. Figure 9.21 below shows the schematic diagram of a micro circuit-breaker structure based on the integration

of several building blocks. The associated table on its right summarizes the function of each brick.



TMA cell:
Self-switch-on of I_{AK} during zero transition of V_{AK}

IGBT cell with preformed channel:
Current generator for blocking order

Enrichment NMOS cell:
Blocking cell, receives order for blocking and short circuit from trigger-cathode junction of thyristor-MOS

Depletion NMOS cell:
Set maximum current and creates the voltage rise which drives the switch-off

Figure 9.21. *Structural schematic of a micro circuit-breaker function*

This basic structure may also be implemented to synthesize a self switch-on and self-blocking component. In this case, the device incorporates a sensitivity or a threshold detection of one or two electrical quantities (current and voltage). Depending on the nature of the component, it can block or become a by-pass. Furthermore, through a process of functional integration, this type of specific function can be designed and implemented by association and cohabitation of building blocks. Figure 9.22 shows the principle schematic of such a function.

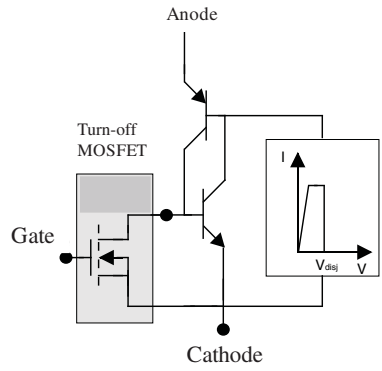


Figure 9.22. *Structural schematic of a self switch-on and self-blocking function*

9.3. Integration of functions within the power component

The monolithic integration of functions within a power component is an important aspect, which comes as additional to functional integration. It is based close to or within the power component, on integration of electrical functions to facilitate the implementation but also to improve the characteristics of the integrated component. This process must be completed to limit the additional associated technological costs, without penalizing the characteristics of the main function, namely the power switch. There are command and associated type functions (closely implemented command, supply of the command, mono or two-way communication interface, etc.) and so-called protection functions [ALK 04, LAU 99, MIT 04a]. Other functions, such as state observers or sensors can also be considered. In this chapter we will discuss two examples of function integration to illustrate this theme.

In addition, other types of functions can be integrated. These functions are mainly about the electrical and physical environment of the component, but this time on the power side. As such, we can consider monolithic integration of CALC (circuit aid to the commutation), based on passive components, but also among other thermal functions for the development and/or the evacuation of the heat flow created by the chips. To illustrate this section, we discuss the case of two cooling solutions, integrated within the silicon chip.

9.3.1. *Monolithic integration of electrical functions*

The reliability and availability of power systems are a concern of current research in power electronics. This requires semiconductor power performances not

only in normal but also in extreme systems. An extreme system is unusual conditions of power component operation: transitional overload, accidental short circuit, wrong operation of the application system, high dI/dt and dV/dt, high dissipated energy, special application, etc.

In such conditions, components are at their ability limits, leading to failure of operation, which can, in turn, lead to the destruction of components, and in the most serious cases, destruction of the system. The integration of specific protection circuits in the heart of the component, protecting it from failures of the external circuit, is therefore a valuable contribution for increasing the "reliability" and the availability of power systems [ALK 04, LAU 99].

In order to utilize more powerful devices receiving a close and self-protected command, it is necessary to associate with power component protection and control functions. These functions should not require the implementation of complex circuits. In this case, the power component occupies the largest area and fixes the technology.

Given that polysilicon is used in MOS technology for the manufacture of grids of power components (VDMOS or IGBT), this material can also be used to define the active areas in which we can use a number of protection components (resistors, diodes, MOS transistors). For example, it is possible to produce a layer of polysilicon on the field oxide of power components, this insulates against the power part, and receives the low voltage components (NMOS, diodes, resistors) (see Figure 9.23).

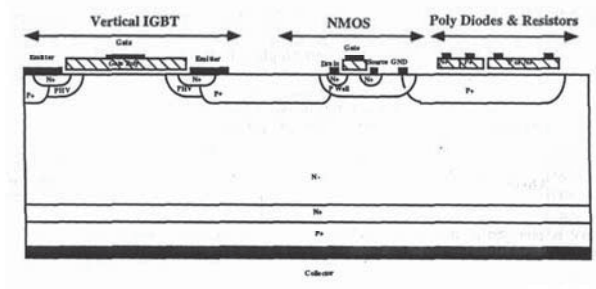


Figure 9.23. *IGBT integrating protection circuits made from a polysilicon layer*

9.3.1.1. *Short circuit protection function*

Within this general framework, we are interested in the IGBT protection against short circuits. At the onset of a short circuit, the power switch delivers an important

current with full voltage to its terminals. The dissipated power in the power structure is very high and its destruction is almost inevitable, because the temperature exceeds the allowable temperature for the junction. There are two types of short circuits: the first is already present at the of the power switch-on (type 1) and the second (type 2) appears when the power switch is already in conduction. Monolithic integrated solutions allow IGBT protection against short circuits in both type 1 and type 2.

9.3.1.1.1. Monolithic integrated detection and protection circuit

The short circuit state is detected if two conditions are met simultaneously:

– a switch-on command is applied to the switch grid; and

– power voltage is present on the anode.

The schematic of the electrical circuit protection principle is given in Figure 9.24. The main elements of this design include a power supply, a load resistance Rc, the IGBT, a circuit of grid command (synthesized by a resistance Rg and a voltage source Eg) and the detection and protection circuit against short circuits. This detection and protection circuit consists of an anode voltage sensor, a delay MOS (Md), a delay resistance (Rdelay) and a cut-off MOS (Mc).

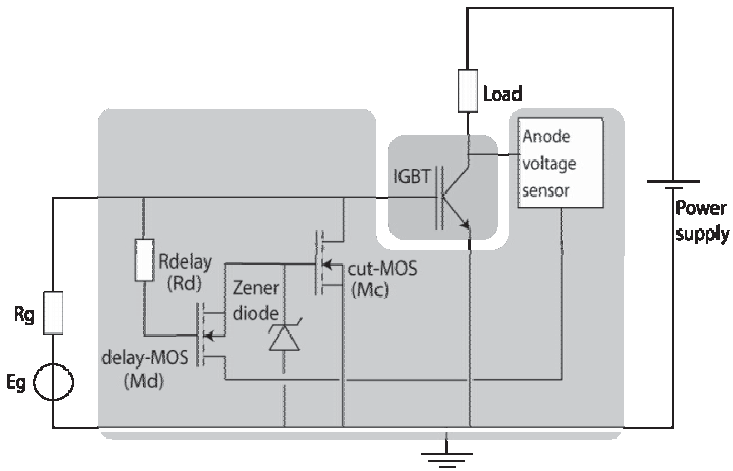


Figure 9.24. *Schematic of the detection and protection circuit against short circuits*

9.3.1.1.2. Operation principle of the anode voltage sensor

If the detection of grid command does not make a major problem, it is not the same for the detection of anode voltage. Indeed, on the one hand the anode is on the back side of the plate and on the other hand, this voltage can be of very high value (from a few to a few hundred kV). The anode voltage sensor must overcome these two problems.

Figure 9.25 shows a schematic cross-section view of the vertical structure of the anode voltage sensor. It is materialized with the help of two P^+ wells referenced to ground, of a deep and low-doped N^- base (which is naturally present in a power switch and allows the voltage strength) and a P^+ or N^+ implantation on the rear. A heavily N^+ doped region is located between the two P^+ regions, and allows an ohmic contact. This contact can detect a voltage V_{sensor}, which is an image of the voltage applied to the anode. There is no particular technological difficulty in producing this sensor. It may be easily integrated into any process of power technology [LAU 99].

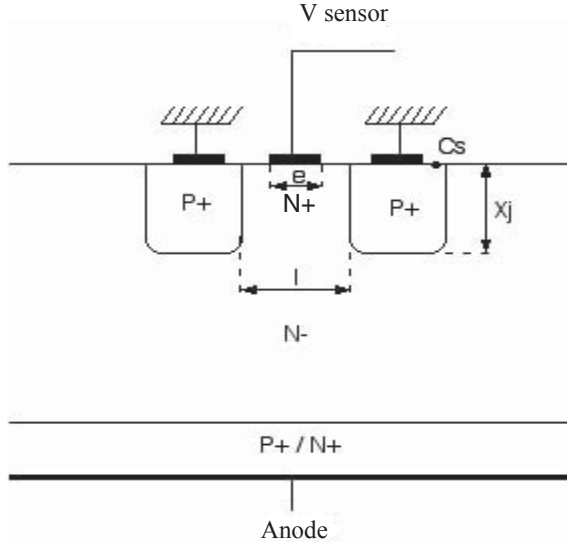


Figure 9.25. *Vertical cross-section view of anode voltage sensor*

For a given thickness of plate, voltage V_{sensor} depends on the physical characteristics of the P^+ wells (C_s = surface concentration of P^+wells; X_j = junction depth of P^+ wells); thickness of the plate W; length l, between wells; length of metallization "e" of ohmic contact, V_{sensor} (its influence remains modest and is

especially significant for high values of anode voltage); and, of course, the voltage applied to the anode. The parameters for optimization of the sensor are thus: e, X_j, C_s and l.

Figure 9.26 illustrates the behavior of the electrical voltage sensor, the change in voltage V_{sensor}, depending on the voltage applied to the anode for different lengths, "l". The technological parameter values used for this example are: W = 300 µm, X_j = 6 µm, $C_s = 2.10^{19}$ cm^{-3} and e = 4 µm.

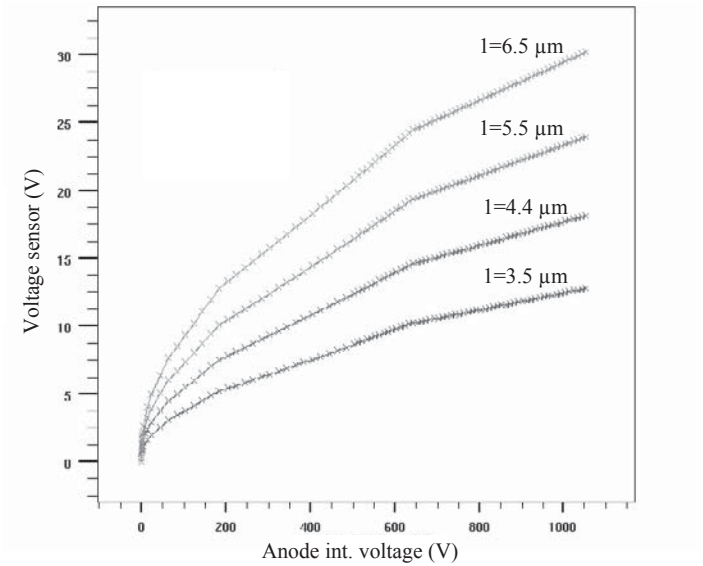


Figure 9.26. *Voltage V_{sensor}, depending on the anode polarization and the distance l between the two P^+ wells (X_j = 6 µm, $C_s = 2.10^{19}$ cm^{-3}, e = 4 µm, W_{plate} = 300 µm)*

V_{sensor} increases with the voltage applied to the anode but within a much lower range (between 5 and 25 V for a voltage anode up to 1,000 V). This voltage range can be directly used by a signal processing and information circuit. In fact, V_{sensor} is an image of the anode voltage. The optimization of this sensor shows that for a given anode voltage and a thickness W of plate, the increase in technology parameter values X_j and C_s, leads to a decrease in the value of V_{sensor}. Similarly, for identical conditions, a reduction in length will decrease the value V_{sensor}.

These findings on the electrical behavior of the sensor can be explained by the recovery of the potential lines between the two P^+ wells. Indeed, shorter length

and/or deeper P^+ wells (large X_j and/or C_s), leads to a more effective recovery. Thus, the high potential line values cannot reach the ohmic contact issuing the V_{sensor} value.

9.3.1.1.3. Principle of operation of detection and protection circuit

The integrated structure corresponding to the circuit layout of detection and protection against short circuits (Figure 9.24) is shown in Figure 9.27. Around the IGBT, the elements are integrated in order to obtain a recovery of potential lines between each P^+ area. There are two possibilities for integration of the delay resistance (Rdelay). The first is to achieve a diffused layer, the second is to materialize resistance on the surface of the structure with a layer of polycrystalline silicon, deposited on the field oxide.

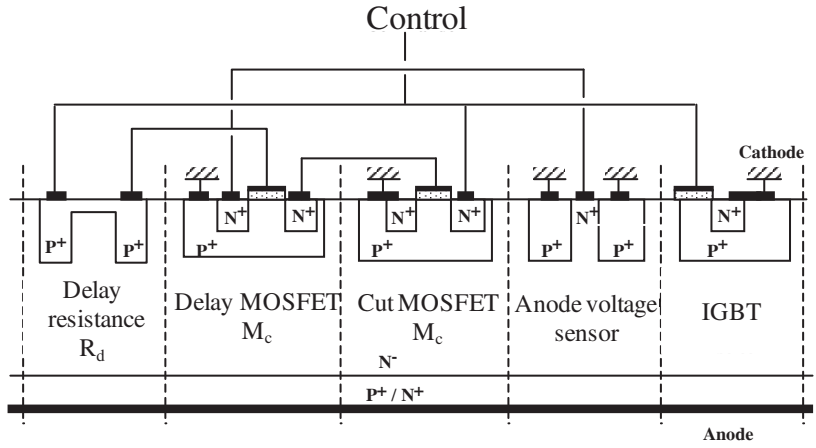


Figure 9.27. *Integrated structure corresponding to the electrical diagram of Figure 9.24*

At the onset of a short circuit, the anode sensor voltage delivers a continuous V_{sensor} image of the supply voltage. This voltage will trigger the command of the cut-off MOS (Mc) via the delay MOS (Md). The latter must be calibrated so as to obtain a voltage on the cut-off MOS grid that exceedes its threshold voltage (V_{TC}) when a short circuit appears. In normal operation, V_{sensor} must be significantly lower than the threshold voltage of the cut-off MOS ($V_{sensor} < V_{TC}$).

In the case of a short circuit of type 1, the delay MOS can load the grid of the cut-off MOS with a delay determined by the time constant RC formed by its grid capacity and the delay resistance (Figures 9.24 and 9.27). Thus, during a normal commutation (transition from state OFF to state ON of the switch without the

presence of a short circuit). This time period allows the grid of the switch to take charge while the anode voltage drops down to a value equivalent to that of the on-state (a few volts). Indeed, without this delay time, the cut-off MOS would immediately be (active) and the switch could not operate. Once active (validation of the presence of a type 1 short circuit), the cut-off MOS discharges the grid for the power switch, making a (controlled) short circuit from the power switch to the ground. Switching to the on-state of the switch is then impossible.

If the phenomenon of short circuit occurs while the power switch is already in the on-state (type 2), anode voltage moves from a low value (voltage drop of the on-state) to full voltage. The anode voltage sensor then delivers a voltage above the threshold voltage of the cut-off MOS, which then discharge the gate of the IGBT. In this case, there is no delay time since the grid command of the delay MOS is already established. Note the introduction of the short circuit detection and protection circuit to the centre of the isolated grid power switch does not change its behavior under static and dynamic operation.

Figure 9.28 shows simulation results showing both the changes in command voltage (Eg) and voltage on the grid of IGBT without the presence of a short circuit, and for a type 1 short circuit. The change in grid voltage without short circuit shows that the presence of the detection and protection circuit does not alter the electrical behavior of the IGBT for a commutation from the on-state to the off-state. In contrast, the grid voltage of the IGBT in case of a type 1 short circuit, goes under its threshold voltage (≈4 V) within 300 ns, despite the grid command Eg.

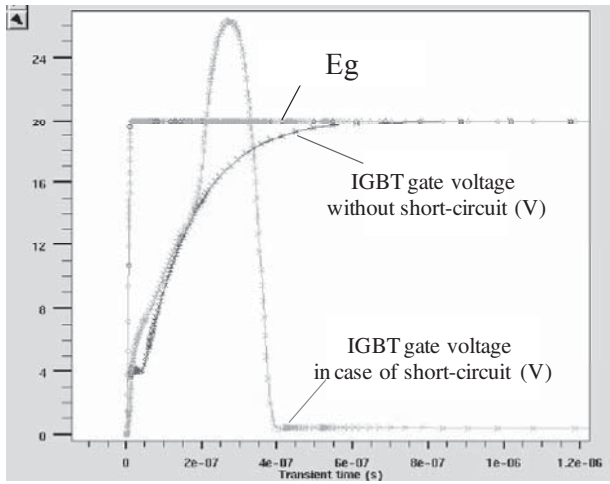


Figure 9.28. *Two-dimension electrical simulation of detection and protection circuit with an isolated grid power IBGT in the case of a type 1 short circuit*

9.3.1.2. *The self-supply of the close command of an isolated grid switch*

In power electronics, supplying the close command of a grid switch is a "basic" brick for its implementation. It helps to provide energy to the close command, usually via a galvanic isolation to ensure the adaptation of voltages. Its integration within the power component has several advantages:

– simplification of the implementation of the component;

– reduction of the connections and increased reliability;

– reduction of conducted type EMC propagation paths; and

– creating a board to supply auxiliary functions.

However, to be "viable" economically and technically speaking, the integration of this type of supply must remain simple, without additional major technological and especially generic cost. To meet these functional but also technology requirements, the best choice is not always the most obvious. International research has shown several ways to supply the command of a grid switch, it now remains to identify those that can be integrated within a VDMOS type power chip.

One of these is to take the energy on the terminals of the component when it is available [MIT 04a]. Its originality lies in the fact that all the active components can be integrated within the power chip through its own technological process. Based on the very simple and general principle of the linear regulator, this solution helps to overcome the problems of galvanic isolation and monolithic integration, while providing a solution for high efficiency conversion. Its electric schematic is given in Figure 9.29.

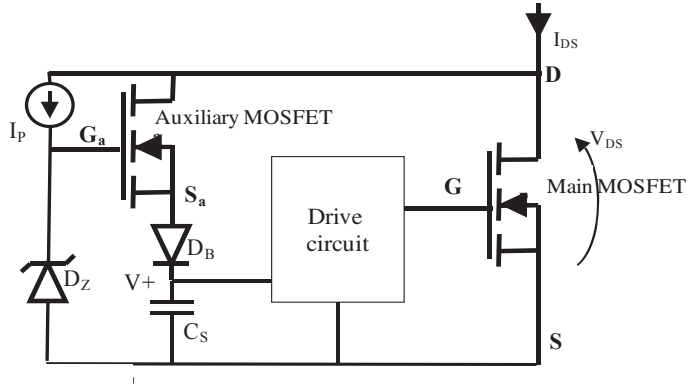


Figure 9.29. *Electrical schematic of an integrated function for supplying the close command of a power switch*

9.3.1.2.1. Principle of operation

The operating principle is based on a "pulsed" linear regulator placed in parallel with the power transistor. When the main transistor is blocked, the circuit in parallel regulates the voltage of a capacitor storage via an auxiliary power transistor and a branch of polarization. When the transistor enters the on-state, blocking diode Db prevents the capacitor discharge. The energy stored in the capacitor is then used to supply the close command of the switch during its conduction phase. It is important that the main switch be regularly blocked to enable the self-supply system to store renewed energy.

9.3.1.2.2. Realization

The power components all share the same constraints in voltage, which greatly facilitates their monolithic integration. In addition, they all have as a common electrode, the rear side of the component. The low-voltage components can be made on the surface via the technological process of the main transistor. A cross-section view of the whole is given in Figure 9.30. It should be noted that a VDMOS process can, with approximate flexibility, create all the functions. The various elements of the self-supply must be properly designed in order to obtain the desired functional or electrical interface characteristics.

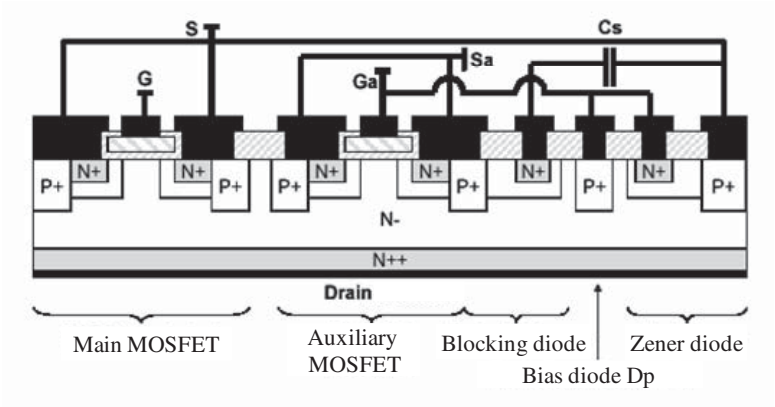


Figure 9.30. *Cross-section view of all elements of the supply system as a monolithic integration compatible with the main switch (except the element of storage)*

Such a solution is based on a system approach closely coupled with a desire for monolithic integration (Figure 9.31). If it is not universal, it has some advantages as being simple, efficient and very easy to implement [MIT 04c]. Figure 9.32 shows the result of a practical implementation where we can observe the proper operation

of a power transistor via the evolution of its drain source voltage. We can also see that the function regulates (more or less effective following the specification and characteristics of components) the close command voltage.

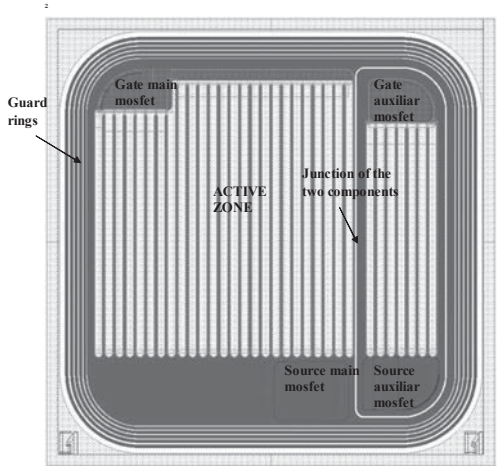


Figure 9.31. *Top view of the main and auxiliary components*

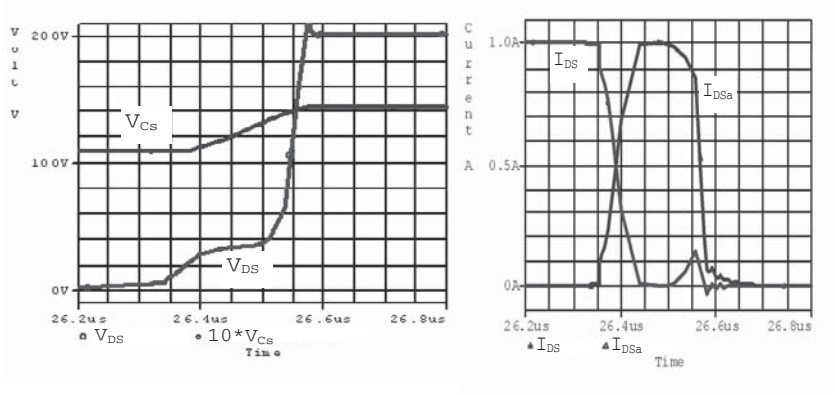


Figure 9.32. S*imulation results showing the evolution of waveforms during storage capacitor recharge*

Evolution of the close command supply technique can be considered, implementing a JFET type power switch instead of the auxiliary transistor and its

branch of polarization (see Figure 9.33) [MIT 04b]. This component can be fully integrated within the power component, thus providing a simplified solution with similar but different characteristics from the previous solution.

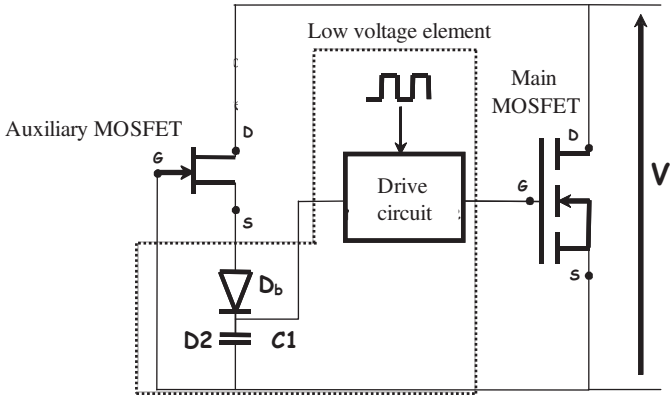


Figure 9.33. *Electric schematic of another technical solution (with a JFET transistor) for integration and compatible for supplying the close command*

9.3.2. *Extensions of integration*

9.3.2.1. *The passive elements*

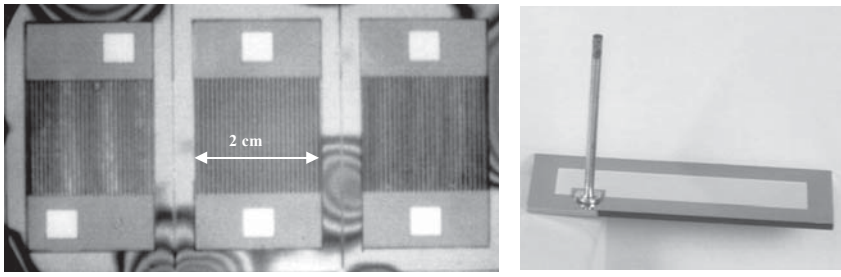
The reductions in the size and weight of portable equipments (telephones, micro-computers, electronic diaries) are linked to a reduction of power dissipation. This strategic niche has led to development of works related to the development of passive components on silicon, in the prospect of moving towards monolithic converters. This approach should reduce the number of components, their connections and lead to more reliable and less expensive products. Many filtering applications based on RL networks are also involved.

Recent developments in the field of micro-technologies have profoundly changed the microstructure manufacturing possibilities. These new techniques are particularly well suited for the manufacture of windings on silicon. The achievement of resin elements and the electrochemistry of magnetic or conductive materials supports the creation of magnetic cores and windings with a thickness of several tens of microns. Generally, the so-called "cold" technological process is able to operate *post-processing* and therefore consider integration with semiconductor devices. First prototypes with a value of inductance of 35 nH/mm^2 at 1 Mhz were made. The manufacturing process used is fully compatible with the standard CMOS process and micro-converters with an output power of 1 to 2 W may be

incorporated. The other major passive element that would be good to integrate on silicon is the capacitor. Note, the deep etching technology, which uses the volume of silicon to maximize energy storage per area unit.

9.3.2.2. *The integrated cooling*

The thermal environment of power components determines their proper operation and their electrical performances. On the one hand, it is important to facilitate the evacuation of losses generated by the component and on the other hand, it is interesting to maintain a temperature as homogeneous as possible within the component. For this reason, research is undertaken to integrate within the power chip, a thermal function playing the role of heat distribution, ensuring an isothermic operation of the chip (in case of non-uniform loss). Figure 9.34 shows two possible solutions for silicon: one of them is based on the integration of a single phase micro-channel exchanger, the other is based on the integration of a heat pipe dispatch. Figure 9.35 shows the schematic diagram of a heat pipe for heat dispatching [AVE 02a].



(a) (b)

Figure 9.34. *(a) All silicon single phase exchangers; (b) all silicon heat pipe*

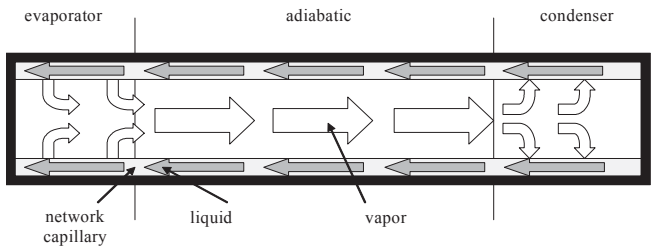


Figure 9.35. *Principle schematic of exchanger*

The distribution of heat increases the exchange surface with the rear and thus making the flow a more important heat flux. This helps to maximize the current rating of the semiconductor components. For example, for a MOSFET transistor, the current rating may be greater than the conventional specifications if the exchange on the back side is particularly powerful.

The evacuation of heat can also ensure greater uniformity of temperature within the chip. Thus, when hotspots appear locally, the integrated heat dispatcher can limit the local heating; which often makes a thermal runaway, and the destruction of the component possible.

9.3.2.2.1. Realization

The heat dispatcher is created within the crystalline structure of the component. This limits the adverse effect of the interfaces and thus maximizes the performance of the exchanger or the dispatcher. Its integration also helps to spread the flow of heat before the first critical thermal resistance, that of the electrical insulator (usually a ceramic type AlN, Al_2O_3, etc.).

The dispatcher is made using the techniques of deep etching and pasting of plates (silicon wafer bonding). The plates are engraved to create an important exchange surface, a capillary network. The assembly by plate pasting integrates the thermal function into the silicon. The diagram below (Figure 9.36) presents this assembly.

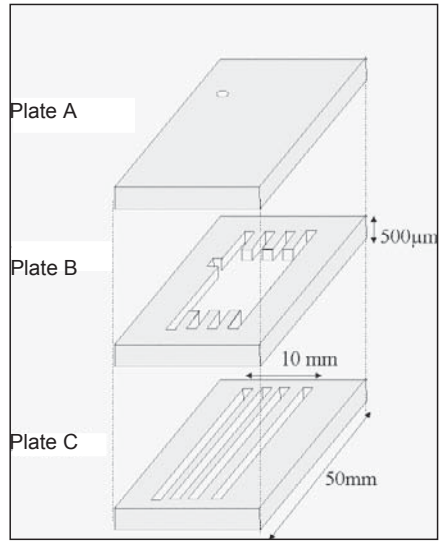
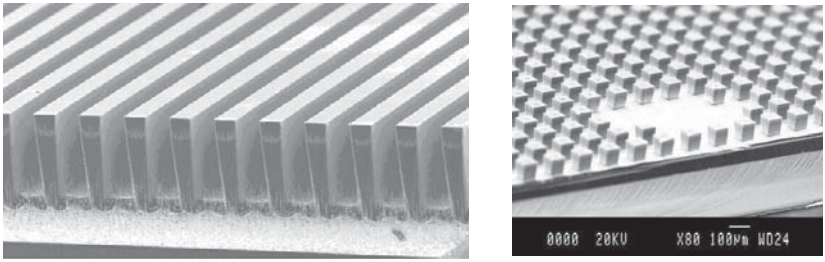


Figure 9.36. *Pasting of three layers to produce the thermal function*

The photos in Figure 9.37 present some views by using microscope to electronically scan a micro-channel network and a capillary network. The resolution sought is the micrometer [AVE 02b, AVE 04].



(a) (b)

Figure 9.37. *(a) Micro-channels network for a single phase heat exchanger; (b) capillary network for heat pipe structure*

9.3.2.2.2. The exchanger

The integrated single phase exchanger evacuates the losses generated by the device via a circulating fluid in a network of micro-channels. The large exchange surface associated with a phenomenon of forced convection helps to maximize the exchanges between the chip and the ambient. The groove size is a major parameter resulting from compromise between the exchange surface and loss of charge and dirt. Indeed, if the achievement of a silicon micro-channel technology poses no particular problem, optimization of such an exchanger does not automatically lead to a very dense network of micro-channels. Studies have been conducted in this way to simplify the design of this type of function but the theory of heat at a micro level does not clearly identify the possible optimum.

In the figure, this type of exchanger can extract a significant amount of heat per unit area. Table 9.1 gives some experimental values for a laboratory prototype.

Q l /min	ΔP: pressure drop	P: electric power delivered Watt	ΔT_j °C	R_{conv} measured K/cm²·W	R_{conv} calculated
0.5	0.066	50	33	0.56	0.85
		100	63	0.53	0.85
1	0.22	50	26.6	0.48	0.4
		100	50.2	0.45	0.4

Table 9.1. *Figures for an all silicon single phase exchanger*

9.3.2.2.3. The dispatcher

The monolithic integrated dispatcher enables increase of the exchange surface and therefore the flow of exhaust heat per unit area, while promoting the thermal balance within the chip. This last feature is based on the creation of a particularly powerful heat sink. This is achieved by a heat pipe that helps maintain an equivalent resistivity near zero within the thermal function. The hot areas, called evaporators are then linked to the cold areas, known as condensers, by a capillary network (Figure 9.35). The liquid trapped in the heat pipe is sprayed on one side, and transferred to the condenser, where it becomes a liquid. The way back is through a capillary network, a real pump of the integrated thermal function. The operating principle is described by the diagram in Figure 9.38.

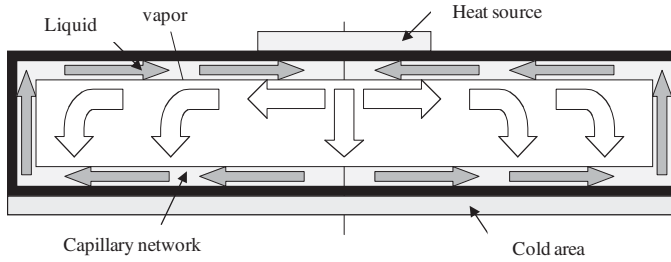


Figure 9.38. *Schematic of the heat pipe with heat dispersal*

For the heat dispersal function, the evaporator is on the front and the condenser is on the back side. For the heat dispatcher function, evaporators and condensers are both on the front, with only the condenser at the rear.

Figure 9.39 is an illustration of the isotherm and heat transfer effects obtained with the use of a heat pipe in silicon technology.

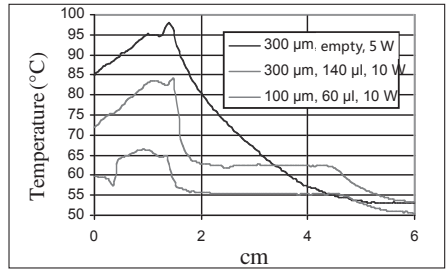


Figure 9.39. *Changes of temperatures on surface of an all silicon heat pipe for several filling conditions*

This process of thermal integration has the potential to affect power components as has been mentioned, but can also affect other applications of microelectronics, and more particularly the very important market of computers and microprocessors.

9.4. Design method and technologies

9.4.1 *Evolution of methods and design tools for functional integration*

In the past, the design of power discrete devices (diodes, bipolar transistors, MOS, IGBT, thyristors, triacs) was made for a given range of power and frequency. Regardless of the precise characteristics of the future application, electronic power application designers were choosing in a catalog the best-suited devices meeting their specifications. This approach, separating the activities of device designers from those of power systems engineers, is no longer adapted to the design of integrated power functions. A new approach is to develop specific functions knowing as *a priori* the specifications of the functionality, the electrical characteristics of the function, and the constraints imposed by its environment. These specific functions result in a de facto system approach.

As we have previously demonstrated, a device based on the mode of functional integration results from the association of basic cells in the silicon. These associations are the topology, layout and physical characteristics of the different semiconductor layers of a cell that determine its electrical functionality. From this point of view, 2D simulation tools based on solving physical equations of a structure described by the physical characteristics of layers (doping profiles, oxide thicknesses, etc.) and their design, can obtain the mode of operation, and the electrical characteristics of the device, at the cost, however, of a careful description in terms of networking and use of appropriate models and physical parameters. The mode of description, based on the topology of the integrated structure, is at a level too far from the functionality and even electrical characteristics. The exclusive use of 2D simulation tools is not particularly well suited to the design of such functions, even if their development constitutes an essential link in the chain of design.

As the function design is closely linked to the surrounding system, the electrical schematic, as a first step, remains the best suited symbolic representation for designers, even if all the subtleties in terms of electrical interactions cannot always be translated. Thus, each cell must be defined by its electrical equivalent, associated models and surface topologies (drawings of masks).

Several phases lead to the design of an integrated device fulfilling the functions defined by a specification. The first phase is to define the function from an electric viewpoint, the second concerns the design of the integrated structure providing this function. During these two phases, designers do not have the same objective, and

indeed do not have the same approach, nor the same culture. Tools and specific methods of design are therefore needed to obtain a coherent approach taking into account the technological and system components of the problem. In this case, the common denominator is made up of a library of basic elements taking into account: the technological aspects through schematic cross-section views of the cells and surface topology; the electrical aspects represented by the equivalent electrical schematic, and the associated models. These models are based either on a more electrical description for the first phase, or a more physical for second, while generally taking into account both aspects in each case.

The problem in the first phase is to define the electric schematic that ensures the functionality required by the specifications. The designer must have a tool enabling a "functional" approach to the problem, based on purely electric considerations, both in terms of output characteristics, and input parameters. These requirements are consistent with the characteristics and specificities offered by the behavioral models. These are based on a description of the behavior of electrical characteristics corresponding to an operation of the component. These behavioral models are mathematical forms.

The other phase involves the design of the integrated structure, i.e. the determination of technological and geometrical parameters. In this perspective, we need to develop analytical models to highlight the influence of physical and geometrical parameters on the electrical characteristics of the function (or behavior in the application sought). At this stage, a library should allow us to make a quick first design of the structure to be integrated, including the number of cells to integrate (requested surface), and values of technological parameters. With this approach, 2D simulation tools can then be used to validate the results of this design phase before committing to the manufacturing stage. The organizational structure of Figure 9.40 illustrates this design strategy.

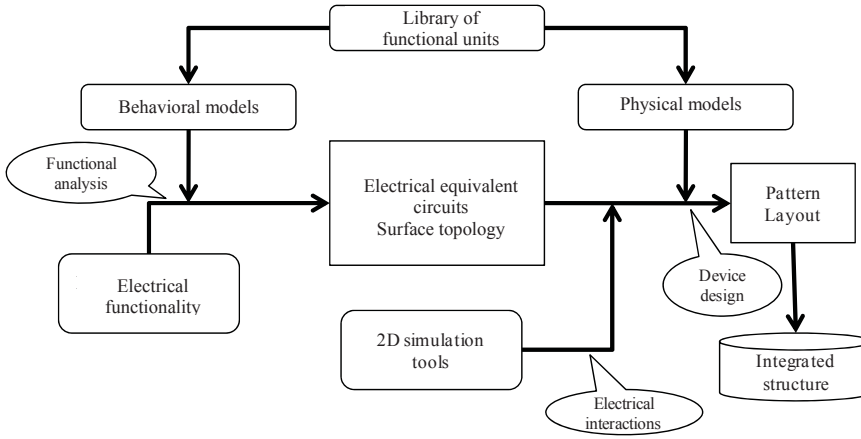


Figure 9.40. *Organization chart describing the design methodology for functional integration*

The following table (Table 9.2) presents an inventory of the major basic cells listed for a 4-layer N/P/N/P thyristor type technology integrating the four types of MOS transistors, channel N and P, with enrichment and with depletion.

9.4.2. *The technologies*

The functionality and electrical characteristics of devices based on this method of functional integration depend not only on the arrangement of semi-conductive layers and surface topology but also on the physical characteristics of different regions.

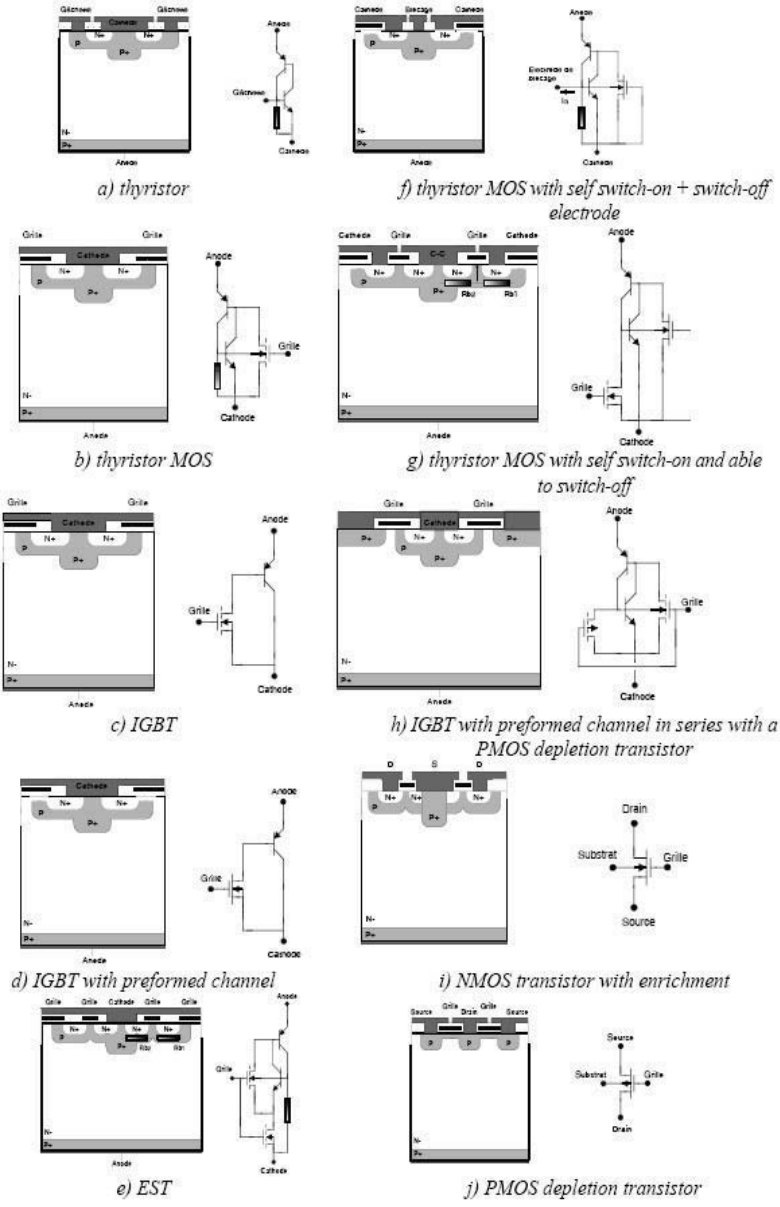


Table 9.2. *Major cells used for functional power integration*

The technology used in functional integration must therefore be composed of optimized stages, which are compatible with each other. The technological process of producing a structure for an electrical function will be established from the association of all or part of the optimized steps of this sector. This pipeline can be established around an "in-line" process with polysilicon grids in order to achieve basic power devices of the MOS/bipolar family (IGBT, MOS-Thyristor) and supplemented by specific technological steps achieving:

– integrated elements on the rear side;

– the possibility of introducing the four types of MOS;

– the possibility of carrying out two types of P cells;

– P– peripheries;

– P+ cells; and

– the introduction of specific technological steps.

The step sequence must be in accordance with the final heat balance of each step. Figure 9.1 shows the technological step sequence of a flexible chain.

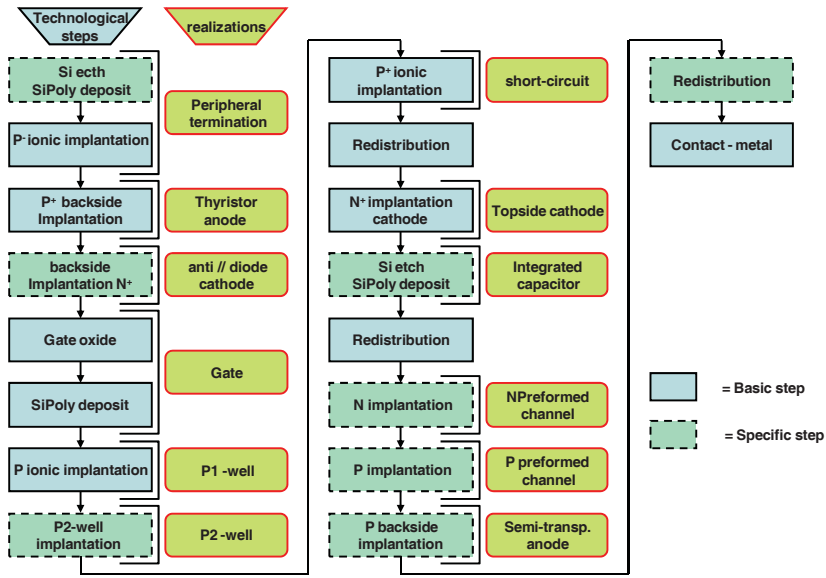


Figure 9.41. *Linking technological steps*

9.4.2.1. *A sequence example*

The main building blocks of this technology are made in the following way: implementation of P^+ cells front and rear, producing the N^+ cathode on the rear side, creating the N doped polysilicon grid, leading to P cells and N^+ cathode aligned with the grid and production of preformed N and P channels.

The starting substrate is N-type silicon. P^+, P and N^+ regions are made by ion implantation (boron for the P type and arsenic for the N^+ type). The redistribution of the P^+ regions (front and rear) and the N^+ rear cathode is done, during the creation of the gate oxide made at 1,100°C, and during redistributions of P cells and N^+ cathodes on the front side at 1,150°C. The gate polysilicon is deposited by LPCVD from the decomposition of silane (SiH4). This is doped by N dissemination of phosphorus. The preformed channels are achieved through the polysilicon by ion implantation of boron for P-type channels and phosphorus for N-type channels. They are then redistributed at a temperature of 950°C. Figure 9.42 shows the sequence of technological steps for the creation of the polysilicon grid, P and N^+ cells.

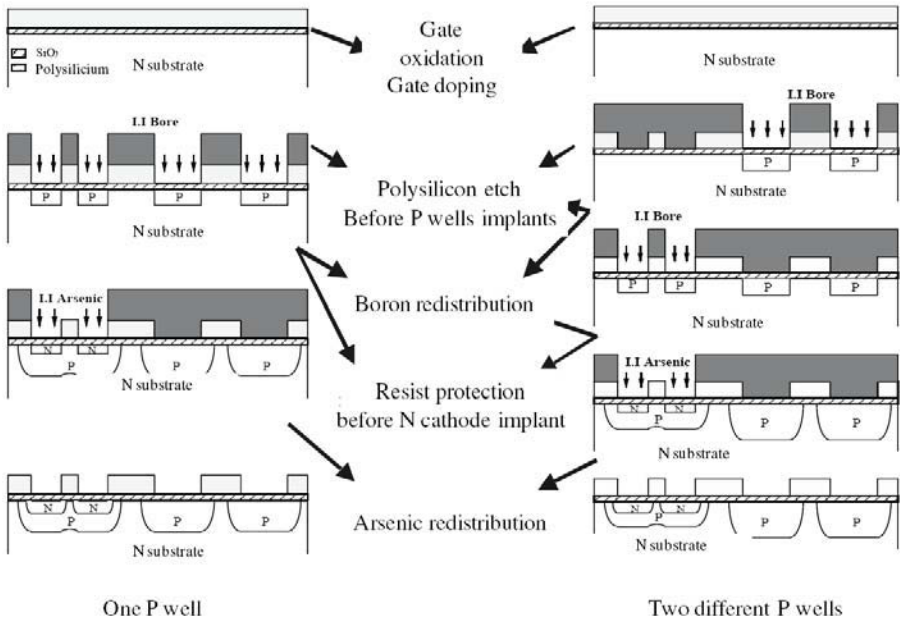


Figure 9.42. *Different sequences of technological steps*

9.4.2.2. *Specific technological steps*

Increasing the complexity of the integrating power functions leads to the development of specific technological steps compatible with the flexible basic industry process. These developments are attributed to progress made in recent years in the techniques used in the field of micro-technology. The reactive ion etching (RIE), the deep etching of silicon by KOH or EIR, the chemical deposits under high pressure vapor (CVD) or low pressure (LPCVD), the deposits of thick resins, the electrochemical deposition, the thermo migration of aluminum, the report of layer and new techniques of assembling being the main examples. The mastery of these techniques will achieve, over time, variable integrated capacities, micro-windings, micro-transformers, micro-converters, micro-coolers, etc.

The control and integration of these technologies into flexible technology will ultimately allow, the foundations of power structure design to incorporate active and passive elements, and also develop new features.

9.5. Conclusion

Power electronics was developed in parallel with microelectronics, although it has different objectives: increasing controlled powers, and increasing signal processing capacity.

Major technological advances have been made in the field of microelectronics, that over the past 30 years have had interesting consequences for power electronics. In this chapter, we discussed examples of monolithic integration based on silicon technology (hybrid-type integration of circuits is also possible). Two methods stand out: one emphasizes functionality, while the other relies instead on optimizing the operation and related characteristics.

Initially, achievements using the *Smart Power* technology were made in the low voltage field, corresponding to automobile applications. However, the main success of these techniques of integration comes from the conjoining of bipolar and MOS technologies, which has provided many power component prototypes, but also to the IGBT which is today the best component for great power.

The success of the IGBT is a great springboard for promoting the integration of power and it seems likely, as we showed in the last parts of this chapter, that we will evolve to silicon chips, incorporating many features, and achieving a self-contained device ready to use, reliable and compact (integration of auxiliary power supplies, controls, safeguards, cooling, etc.).

It also seems that by adding the integration of some passive components, we can in the next decade, develop autonomous micro-systems performing the switching function for high power and packaging of electrical energy, which is so widespread.

9.6. References

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